Advanced PCB design and layout for EMC.

Part 1 – Saving time and cost overall

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This is the first in a series of eight articles on good-practice EMC design techniques for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances, commercial and industrial equipment, through automotive to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time to market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues

A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” included a section on PCB design and layout [1], but only set out to
cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. This series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles by this author (e.g. [3] [4]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not bother with why these techniques work, they will simply describe the techniques and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1 Reasons for using these EMC techniques

Most professional circuit and PCB designers would love to employ all of the good EMC techniques described in [1] - [4] and this series, but are often prevented from doing so by project managers and other managers who only see these techniques as wasted time and added cost.

Sometimes it is the manager of the PCB layout department who prevents the use of good EMC techniques, usually claiming that the product cost-to-make will increase, but often really because they have become familiar with their existing PCB design rules and bare-board manufacturers and don't want to make the effort to change.

This section will show that such management approaches are completely the opposite of what is really required these days for success in the design and manufacture of electronic products of any type, in any volume.

PCBs have continually been getting more high-tech and costly ever since they were first invented, and they will continue along this path for ever. In a few years time microvia PCBs with more than 8 layers and embedded capacitance will be the norm. It is a tough commercial world for everyone these days, and companies that don't keep up with PCB technology will be left in the dust of those that do.
1.1 Development – reducing costs and getting to market on time

Even if a PCB has no nearby wireless datacommunications antennas, and even if it does not use high-speed devices or signals, these PCB techniques can save time and money by reducing the number of iterations it takes to get the circuit working with its full performance specification. This is because many EMC techniques are also signal integrity techniques. In fact, good PCB design for EMC goes beyond the requirements for signal integrity; so a PCB that is designed using good EMC techniques generally has excellent signal integrity.

The author originally developed the PCB design techniques described in [1] - [4] over ten years and three companies in the 1980s to enable powerful digital processing, sensitive high-specification analogue circuits, and switch-mode power converters to share the same enclosure, even the same PCB, without compromising the analogue performance at all.

Projects that used to require 10 or more design iterations could use these techniques to meet their performance specifications on the first PCB prototype. During the 1990s it was found that these techniques also achieved excellent compliance with EMC Directive test standards, without requiring high-specification enclosure shielding, sometimes without any shielding at all.

Good EMC design techniques are good signal integrity techniques, for both analogue and digital circuits. This means more predictable project timescales with fewer three-cornered arguments between the circuit, PCB and software designers as to whose fault it is that the performance falls short of its specification.

However, there are still very many companies that do not employ the techniques described in [1] - [4], never mind the advanced PCB techniques described here. This appears to be because they don’t realise that the true cost of a design modification increases rapidly as a project progresses. People only tend to see the obvious costs of the modification (the hours
spent, the cost of another prototype PCB, etc.) which are the same whatever stage the project is at, but Figure 1A gives an idea of how the real cost of a modification varies during the project timescale.

![Figure 1A](image)

Of course, once a design iteration causes a delay in the market introduction the true costs of that modification can be astronomical. This issue is much more important than it was even ten years ago, due to the very short product lifetimes now being experienced for almost every application area. Some cellphone and computer industries already have product lifetimes of 90 days or less, but it is increasingly likely that for even quite ordinary products and equipment, being 6 months late to market can mean no market at all – with the consequent loss of all the investment in the project. For some debt-financed companies, the loss of investor confidence caused by a late market introduction can lead to the loss of the company.

So it is not too exaggerated a claim to say that good PCB design and layout techniques are a valuable financial tool and competitive weapon. The section below on ‘trends’ should make this claim even more clear.

1.2 Reducing unit manufacturing costs
1.1 above dealt with project costs, but unit manufacturing costs also benefit from the use of good EMC techniques at the level of PCB design and layout.

A general rule of thumb is that the true costs, in manufacture, of controlling EMC increases tenfold for each higher level of assembly. So the lowest-cost place to control EMC is in the design of the ICs and semiconductors. Achieving the same EMC performance at PCB level costs about ten times more than if it could be done in the IC. And if implemented at product enclosure level the true costs of achieving the same EMC performance are ten times higher again, as shown by figure 1B.

![Figure 1B](image)

Few designers have as much control over the EMC characteristics of their ICs as they would like. Most are stuck with using commodity ICs with no EMC controls at all (in fact, some of them seem to have been designed to maximise EMC problems). FPGA designers, and especially ASIC designers, have a greater degree of control of the EMC characteristics of their devices – but even so there are limits to what current technology can achieve.

However, as subsequent parts of this series will show, it is possible to completely control all aspects of EMC (except for direct lightning strike) at the level of the PCB, the lowest-possible-cost solution after IC design techniques.
A common project management perception in too many companies is the idea that the product made with the lowest-cost components will be the most profitable. So designers are constrained to achieving the lowest possible ‘BOM cost’ (BOM = Bill Of Materials) for their circuits and PCBs, which means that numerous good EMC design techniques (such as PCBs with at least 8 layers) are not permitted because the designers cannot prove that they are essential. (This was the very management technique that led directly to the demise of the Challenger space shuttle, because the engineers could not prove to their managers that the booster O-ring seals would malfunction at the low temperatures present at the launch site).

This management philosophy leads to the idea that EMC measures are best ‘bolted on’ at the end of a project, once it is known what is really required. But these EMC measures will have a unit manufacturing cost of around 10 times what they would have cost if implemented at PCB level (see figure 1B). And since almost all modern circuits of all types now suffer from EMC problems, whether emissions or immunity (and all future ones will, see later) the typical result of the ‘lowest-possible BOM cost’ approach is that the unit manufacturing costs of the products are actually increased by considerably more than they need be.

Also, implementing EMC measures near the end of a project suffers greatly from the very high cost of modifications at this stage, see 1.1 and figure 1A, and it is not at all unusual for market introduction to be delayed by one or more months due to problems with achieving EMC compliance. Late market introduction is a very serious commercial and financial issue these days, much more so than it was even 10 years ago.

This article is not the place to discuss product costing issues. But it is worth mentioning here that, except for a very few types of products (high-performance PC motherboards and graphics cards, some specialist instruments, etc.), the profitable selling price of a product bears no relationship at all to the total cost of its components. Apart from some special
application areas, anyone who thinks there is a direct relationship between a product’s BOM cost and its selling price really needs to understand his or her business a lot better.

It is not at all an exaggerated claim to say that although using good EMC techniques in PCB design and layout usually increases the BOM cost for the PCB assemblies in a product, the unit manufacturing cost will usually be reduced, making more profitable products. The section below on ‘trends’ will show that in the near future the word ‘usually’ in the previous sentence will need to be replaced by ‘almost always’.

1.3 Enabling wireless datacommunications

A product that fully complies with the EMC Directive, FCC or VCCI emissions specifications can still have quite powerful radio-frequency (RF) fields nearby. Radiated emissions are measured with antennas at a distance of 3m or 10m (although some military and automotive standards use 1m), and the general rule of thumb is that the field strength emitted by the product increases proportionally to the reciprocal of the distance. So 37dBµV/m at 10m (a CISPR 22 limit) becomes 57dBµV/m at 1m and 77dBµV/m at 100mm – nearly 10 milliVolts/metre!

Also, the standard radiated emissions tests measure in the far field and so don’t detect the near-field emissions from the product at all. Near-field effects can be thought of as electrical coupling due to stray capacitance and stray mutual inductance. Near-fields fall off with the reciprocal of the square or cube of the distance, so are quite insignificant at 3m distance or more, but within 100mm of an electronic circuit they can be much more intense than the fields predicted from the far-field measurements.

When a wireless receiver is added to a product (e.g. when GSM, Wi-Fi or other IEEE 802.11 variants, Bluetooth, Zigbee, etc., datacomms are added) the receiver’s antenna is closer to the product than 100mm, and so can pick up some very strong fields. The chances of the
product's radiated frequencies actually coinciding with the RF signal to be received is small, but the RF receivers used do not have perfect selectivity and their gain is very high, so it is often the case that the product interferes with its own datacommunications. This is usually seen as a reduction in the range achieved by the wireless link, and ranges which are ten times less than required are not uncommon.

Many manufacturers have had range problems for the above reasons when they have tried to add wireless datacomms to an existing design, even though it passed its standard emissions test with a good margin. Often, very costly EMC modifications are found necessary to reduce the RF fields around the antenna. These are usually costly both in the development time required and in the unit manufacturing costs.

The PCB EMC techniques described in this series will help add wireless datacomms with good range, most easily and with the lowest additional costs.

This is especially so where an internal antenna is required. Products with internal antennas cannot use their external enclosures for shielding, so must employ PCB-level shielding as described in the part 2 of this series.

1.4 Enabling the use of the latest ICs and IC packages

Huge benefits can be achieved for some products by using the latest 130 or 90nm chip-manufacturing processes to create ‘systems on a chip’, and/or by using chip-on-board or ‘chip-scale’ packaging, both of which save a great deal of PCB area. These new technologies can even enable new application areas which had always been considered impossible, or at least impractical.

However, these state-of-the-art (at the time of writing) silicon processes are associated with increased levels of increased frequencies, and the chip-on-board and chip-scale packages have much lower interconnection inductance (they have no lead frame) and so allow more
high-frequency noise to 'leak out' of their IC's silicon chips into the PCB's conductors, where they find more efficient 'accidental antennas'.

The higher levels and higher frequencies associated with these new and very desirable technologies cause problems for signal integrity, and the situation is made worse by the fact that these ICs typically operate on much less than 5V d.c. power (1.8V is not untypical) so their logic thresholds are lower and they are more vulnerable to interference.

Figure 1C shows an example of this issue causing a signal integrity problem, where acceptable noise levels in an existing design of PCB can result in unreliable digital operation if the ICs are replaced with otherwise identical equivalents that operate on a lower power supply voltage. Many designers have been surprised at how difficult it can be to simply convert an existing design to employ lower-voltage ICs.

The EMC techniques described in this series are often required for signal integrity reasons, just so that these types of ICs and IC packages can be made to function at all with any reliability.
To pass EMC compliance tests when these ICs are used may require all of the techniques described in this series plus shielding of the overall enclosure. However, the performance specifications for the enclosure-level shielding (and filtering) required will be much less, making the products less costly in manufacture, if these PCB EMC techniques are used in full.

1.5 Easier compliance for high-power DSP

Another situation that sometimes arises is very powerful digital signal processing, where numbers of ICs pass large quantities of data between themselves. The clock rates and signal edge speeds might not come within a decade of what is achieved in the core logic of a 130nm ‘system-on-a-chip’, but the relatively large distances the signals have to travel in their PCB traces can make their signal integrity difficult and their EMC compliance a significant challenge.

The PCB techniques described in this series help deal with both the signal integrity and EMC compliance of powerful DSPs in the easiest and lowest-cost manner.

1.6 Improving the immunity of analogue circuits

Analogue designers working with low frequencies (e.g. d.c. to 10MHz) might assume that all the fuss is about digital ICs and circuits and needn’t bother them. But all analogue semiconductors and ICs contain non-linearities (that is why they are called semiconductors, after all) and the small silicon feature sizes they use mean that they will happily demodulate and intermodulate RF ‘noises’ to frequencies well over 1GHz.

In the early 1990s the author tested a product that was little more than an LM324 on a small PCB for its immunity to RF under the EMC Directive’s generic immunity standard for the industrial environment, EN 50082-2:1995 (now replaced by EN 61000-6-2), and found that it gave much higher error voltages when subjected to 1GHz than it did when subjected to 500MHz. The author has tested many all-analogue products for immunity and they all showed
significant problems up to several hundred MHz, until fixed by applying EMC remedial measures to their circuit design, PCBs and enclosures, basically as described in all six parts of [2].

Now that all analogue electronics exists in an environment that is very polluted with man-made electromagnetic noise up to at least 2.5GHz, whether that pollution comes from external devices such as cellphones, or internal devices such as switch-mode power converters or digital processing, PCB EMC techniques are now necessary to achieve their desired levels of immunity (and hence their signal-to-noise ratios) most easily and with the lowest cost.

2 What do we mean by “high speed”

‘High speed’ is hard to define exactly, but in the context of digital PCB design and layout it usually means signals with edge-rates that are so short that the dimensions of the PCB start to have a significant effect on the signal voltages and currents.

Another way to look at it is to say that the PCB dimensions are so large compared with the propagation time of the signal’s edge that the PCB’s traces and planes start to behave as resonant transmission lines instead of ‘lumped’ constants (e.g. milliohms, picofarads, nanohenries).

The velocity of electromagnetic propagation is limited by the laws of nature, and in an FR4 PCB it is approximately 50% of the free-space velocity of $3.10^8$ m/s, say 660ns per metre (2ns per foot). So we can associate an ‘edge length’ in millimetres or inches with each rising or falling edge of a signal. So a 1ns edge has an ‘edge length’ in an FR4 PCB of approximately 75mm (3 inches).

The rule of thumb is that we usually need to design the PCB using transmission-line techniques when the edge length is shorter than three times the longest dimension of a PCB.
So for a PCB that has a longest dimension of 150mm (6 inches) we would categorise edge rates of 3ns and less as “high-speed”. Figure 1D shows this relationship.

The above sounds quite straightforward – all we have to do is look in the devices’ data sheets for their rise and fall times to see whether we need to use advanced PCB techniques. But, as usual, real life is not so obliging – notice that figure 1D refers to the actual transition time. Rise and fall times may not even be given in the data sheets for some ICs, and in any case they only specify the maximum values. Actual transition times experienced in real life can be much less than what is specified on a data sheet, and will often be somewhere between a half and one-eighth. This allows the semiconductor manufacturers to shrink their silicon processes so as to squeeze more chips onto a wafer, improve yields, and make more money without the expense of updating their data sheets every time they do one of these ‘die shrinks’.

So a venerable glue logic device with a specified maximum rise and fall time of 6ns might nowadays be made on a silicon process that is ten times smaller than when it was first introduced to grateful designers, and might switch in under 1ns. Since some estimates have it that 30% of the USA’s gross national product depends on silicon feature sizes shrinking year-on-year in accordance with Moore’s law, for ever, we can see that it won’t be long before
all devices are “high speed” and all PCBs need to be designed using advanced techniques that take full account of the transmission line behaviour of traces and planes.

Figure 1E shows the measured noise emissions from a basic HCMOS glue logic IC, showing that it is generating frequencies on its outputs and power pins that go far beyond what would be expected from its data sheet specification.

Another issue is that many VLSI ICs have ‘core logic’ processes that use much smaller devices than their output drivers, and operate at much higher frequencies than the overall system clock, with much faster signal edges. These cause transient signals to be injected into the PCB’s 0V and power distribution systems, and common-mode noises on all the I/Os (often referred to as ‘ground bounce’ or ‘rail collapse’). The edge rates of these power transients and common-mode noises can be under 100 picoseconds, which we would categorise as “high speed “ for a PCB with longest dimension of only 5mm.

For analogue circuits, the “edge length is shorter than three times the longest dimension of a PCB” rule of thumb becomes the “tenth of the wavelength at the highest frequency of concern” rule, usually written as $\lambda_{\text{MIN}}/10$ (since the minimum wavelength, $\lambda$, of concern is associated with the maximum frequency or concern).
Note that the wavelengths that matter are the ones that occur inside the PCB, and due to the slower velocity or propagation in a PCB (about 50% of the velocity in air) they are about 50% shorter than the wavelengths associated with the same frequency in air. So instead of the $\lambda_{\text{MIN}}/10$ guide, some designers prefer to use a $\lambda_{\text{MIN}}/20$ rule of thumb, where the wavelength is calculated as if the signal concerned was in air instead of in a PCB. The relationship between highest frequency of concern and PCB dimension is also shown in figure 1D.

3 Electronic trends, and their implications for PCBs

3.1 Shrinking silicon

Section 2.1 above said that some estimates have it that 30% of the USA’s gross national product depends on silicon feature sizes shrinking year-on-year in accordance with Moore’s law, for ever. This trend is published as a an ‘official roadmap’ by the Semiconductor Industry Association, which is a major multinational organisation. Figures 1F and 1G are derived from the roadmap they published in 2001.
IC trends are driven by higher speed of operation, increasing complexity (more transistors per IC), improving wafer yield, and the cost to make each ‘chip’. All of these aims are what is driving the electronics industry to create more advanced products at lower costs, and even to address markets that were previously impossible, and they are all achieved by shrinking the feature sizes on the silicon wafer.

The established state of the art in silicon feature size is (at the time of writing) 0.13 microns (130nm) with a number of companies developing 90nm processes and research progressing on 65nm. Some semiconductor companies are already claiming to have 90nm or 65nm products in production, but these processes are not yet sufficiently well-developed to be in widespread use. There is an unstoppable trend towards smaller feature sizes and this is very good news for the future applications of electronic technologies.

But all this silicon high-technology has an inevitable downside for EMC and signal integrity.

The EMC effects of shrinking feature size include…

- ICs that are more vulnerable to over-voltage damage (insulation layers are thinner)
- Data ‘bits’ are more vulnerable to data corruption (due to wider bandwidth and lower capacitance)
- Increasing emissions

The increasing emissions occurs because smaller silicon feature sizes means…
It is important to note that it is not the clock frequency that is important here – it is the switching transition time. Even if the clock frequency doesn’t increase, using smaller silicon processes increases the emissions significantly. Figure 1H shows the effects of changing the switching edge speed on the harmonics of a 100MHz clock.

The shrinking silicon feature size issue applies to all digital ICs including ‘glue logic’, not just VLSI and high-speed devices. It also applies to some analogue ICs. ICs are being made using silicon fabrication processes that employ ever-smaller feature sizes simply to improve the yield from the silicon wafers to make more money for the semiconductor companies.

So even buying the same old devices doesn’t protect a manufacturer from ‘die shrinks’, and a new batch of ICs can make a previously EMC-compliant product non-compliant, or even make its operation unreliable by compromising signal integrity. The needs of the semiconductor companies to earn more money for their shareholders has been known to cost some of their customers many millions of dollars in having to redesign their entire existing portfolio of products. Of course, while you are busy redesigning all your existing products, you have no
resources to spare for designing new ones, and this can have the most serious financial implications for a manufacturing company.

3.2 Shrinking packaging

Smaller packages have lower inductances in their bond wires and lead frames, which can increase the levels of very high-speed core noise that 'leaks out' via the I/O and power/reference pins, and also allows the true ‘sharpness’ of an output driver’s transitions to be applied to the PCB’s conductors. Designers have often been surprised at the signal integrity and EMC problems caused by simply replacing a device with the same type in a smaller package. One designer used a chip-scale IC in 2000, operating at the very low clock frequency of 1kHz, and was amazed to find that his product was failing emissions tests at 1GHz, due to the 1 millionth harmonic of the clock.

‘Chip-scale’ packages which are hardly any larger than the silicon chip itself are the ultimate expression of this packaging trend, and generally require the use of microvia PCB construction (see part 7 of this series). Chip-scale devices allow enormous improvements in miniaturisation, so there will be great pressure to use them.

Smaller packages can in fact help to improve EMC, but only if advanced PCB techniques are applied early in a project.

3.3 Shrinking supply voltages

To reach higher speeds (and reduce thermal dissipation) ICs and communications are using increasingly lower voltages, and the problems that the resulting lower logic threshold voltages can cause were briefly discussed in 1.4 above and Figure 1C. Because of the ever-increasing numbers of semiconductors integrated in modern ICs, the amount of power required is increasing, so the supply voltages are continually decreasing to
try to stop ICs from failing due to overtemperature, and (in battery-powered products) to extend battery life.

The result is that power supplies need a lower source impedance and a higher accuracy (tighter voltage tolerances). And since the IC loads operate at ever-higher frequencies they need their low source impedance to be maintained to ever-higher frequencies. Figure 1J shows an example of the trend that has occurred over the past few years.

![Figure 1J: Example of PCB power supply trends](image)

<table>
<thead>
<tr>
<th>Year</th>
<th>Supply (Volts)</th>
<th>Supply (Watts)</th>
<th>Supply (Amps)</th>
<th>Supply impedance target (milliOhms)</th>
<th>Supply impedance to be maintained up to (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990</td>
<td>5.0</td>
<td>5</td>
<td>1</td>
<td>250</td>
<td>16</td>
</tr>
<tr>
<td>1993</td>
<td>3.3</td>
<td>10</td>
<td>3</td>
<td>54</td>
<td>66</td>
</tr>
<tr>
<td>1996</td>
<td>2.5</td>
<td>30</td>
<td>12</td>
<td>10</td>
<td>200</td>
</tr>
<tr>
<td>1999</td>
<td>1.8</td>
<td>90</td>
<td>50</td>
<td>1.8</td>
<td>600</td>
</tr>
<tr>
<td>2002</td>
<td>1.2</td>
<td>180</td>
<td>150</td>
<td>0.4</td>
<td>1200</td>
</tr>
</tbody>
</table>

The achievement of such low supply impedances (e.g. 0.4 milliOhms) at up to such high frequencies (e.g. 1200MHz) requires very advanced PCB design techniques, and these are discussed in parts 4 and 5 of this series. A great deal of noise is emitted by ICs into their d.c. supplies, as shown in figure 1E. At some frequencies the supply noise currents can be higher than the output currents, and as a result the ‘accidental antenna’ behaviour of the d.c. supply distribution on a PCB can sometimes contribute more to a PCB’s electromagnetic emissions than the actual signals. So d.c. supply impedance is an important EMC issue.

Of course the trend shown in figure 1J is continuing, although there seems little possibility in decreasing the supply voltage below, say, 0.8V due to the silicon band-gap voltage being around 0.6V. Increased power requires higher efficiency and more sophisticated cooling
techniques are needed, and with the higher frequencies being used the heat-removal devices (e.g. heatsinks, heat pipes, etc.) now need to be designed for EMC too, so that they do not behave as resonant structures (accidental antennas).

3.4 PCBs are becoming as important as hardware and software

To cope with IC trends, the typical PCB of the future will be a very high-technology component indeed. It will be a network of microwave transmission lines, not simply a convenient way to interconnect devices (no longer simply a 'printed wiring board') – and it will need to be designed in parallel with a sophisticated cooling system.

At the time of writing, more than 50% of the volume of global PCB manufacture uses 6 - 12 layers, and 4 layers or less are only used for the simplest circuits. More than 50% of the volume of global PCB manufacture is also “controlled-impedance” using transmission-line design techniques.

PCB design and layout is becoming just as vital to the product’s function as all of the hardware and all of the software. PCB designers may once have been little more than draughtsmen, but increasingly they are having to actually design their PCBs according to electrical specifications, as described later, and need an understanding of wave propagation and the ability to drive sophisticated field solvers.

3.5 EMC testing trends

The FCC in the USA already require testing of emissions at 5 times the highest clock frequency, or 40GHz, whichever is the lower. And the latest draft of IEC 61000-4-3 which describes basic immunity testing method for radiated RF fields will cover up to 6GHz.

There is no sign of any end to this trend, because the radio spectrum between 1 and 60GHz is increasingly being used for communications and so needs protecting from ‘unintentional transmitters’. High-volume low-cost motor cars are just beginning to be fitted with anti-collision...
systems that fit each vehicle with a radar operating at 77GHz. The future for electronics
design and manufacture is very exciting, but EMC is going to become a truly major headache.

4 Managing designing to reduce timescale risk and warranty costs

4.1 Guidelines, maths formulae, and field solvers

The difficulty of designing PCBs so that circuits will function at all, let alone meet EMC
requirements, is increasing at a much faster rate than silicon processes are shrinking and
clock speeds increasing. But we need to reduce time-to-market, not increase it, so we need to
use methods of designing PCBs so that they achieve functionality and EMC without
time-consuming iterations, preferably without any iterations at all – ‘correct by design’. Two
design methodologies help here: virtual design; and experimental verification.

Desirable skills for PCB designers, just to cope with modern signal integrity problems in
high-speed PCBs (see 2 above), never mind EMC, which is harder, include familiarity with
both 2-D and 3-D field solvers (which now run on PCs), and the ability to design PCBs to meet
electrical specifications such as…

- skew limits
- maximum crosstalk (% or dB) for each trace
- maximum inductances for some traces
- minimum rise/fall times, etc., etc.

There will need to be some iteration between PCB layout and circuit design (e.g. terminating
traces which are found to need to be transmission lines due to their length) – to save having to
iterate the design of the physical PCB when it is found to suffer signal integrity and/or EMC
problems later in the project (see figure 1A for the cost benefits of fixing problems early in the
design and development cycle).
General guides (“rules of thumb”) such as those given in [1] - [4] and this series of articles should be used from the very first to estimate orders of magnitude, and used throughout a project to ‘sanity check’ calculations and the outputs of computer-based simulators.

All practical mathematical formulae that can be used by a practising design engineer are based on simplifications and assumptions that result in inaccuracies, and may not even be true in some instances. As a result they are only appropriate for analytical approximations, quick estimates, and early design tradeoffs. However, it is getting easier to use field solver and circuit simulator software packages running on PCs instead of hand-cranked sums.

Field solvers are the only method that will confirm the signal integrity of an actual design before it is constructed and tested for the first time. Field solvers are getting better and costing less all the time, so one day we will be able to simulate the EMC of our completed designs – but we are still some way from that desirable situation at the time of writing.

4.2 Virtual design

It was mentioned earlier that some electronics industries have very short product lifetimes. These include PC motherboards, PC hard disc drives, PC graphics cards, cellphones, etc., and they often use ICs that have only just been released and for which no experience has been gained. With product lifetimes of 90 days or so, such companies must be confident that they can avoid PCB iterations that would cause them to be late to market. They use virtual design techniques based on circuit simulators and field solvers which interact so as to allow numerous design iterations that prove the PCB layout before the first PCB is even photoplotted.

Circuit simulators come in two main flavours: IBIS [5] and SPICE. It is claimed that IBIS handles complexity more easily than SPICE, and that more IBIS models exist. It is also easier and quicker to generate an IBIS model for a new IC.
Field solvers include 2-dimensional and 3-dimensional types based on a variety of modelling techniques, such as...

- FDTD (Finite Difference Time Domain)
- FEM (Finite Element Model)
- TL (Transmission Line)
- MOM (Method of Moments)

To reduce calculation time to what is achievable with today’s computers (including supercomputers) field solvers use a form of finite element analysis. They divide the structure to be simulated into very small cells, which must be much smaller than the shortest wavelength that can be created by the devices and circuit. They then solve simplified versions of Maxwell’s equations for each small cell in turn. Fields solvers can be used to optimise precise trace widths, dielectric thicknesses, and board stack-up for a target characteristic impedance, determine crosstalk, ground bounce and rail collapse, and many other signal integrity specifications. Some solvers also have limited EMC analysis tools.

There are also field solvers that are aimed at solving EMC problems rather than signal integrity (e.g.[6]) but at the time of writing they are limited to ‘what if’ investigations on simplified versions of the final design, and cannot be integrated with the virtual design flow described below.

In a virtual design and test methodology the circuit is first simulated using IBIS or SPICE, using appropriate models for the active and passive devices, including any wires and connectors. When the circuit simulates correctly, automatic netlisting sends a ‘rats nest’ to the PCB designer’s software application to prevents logical errors in PCB layout. The circuit designer will have a noise budget for each net (Figure 1K shows an example noise budget) and will communicate the following electrical requirements to the PCB designer...

- Segregation issues and critical component placement, shielding cans, etc. (see part 2 of this series)
- Characteristic impedances for some or all nets.
- Maximum values for ringing and reflections for each net
- Maximum values of impedance discontinuities for some or all nets
- Maximum values of cross talk for each net
- Maximum values of ground bounce for each net
- Maximum values of rail collapse for each net
- Flight times for some or all nets
- Maximum inductances for power supply decoupler traces
- Skew limits between nets

The PCB designer performs ‘what if’ simulations on critical parts of PCB’s physical structure (trace width, stack-up, etc.) using the appropriate in 2-D or 3-D field solvers, using appropriate parameters for final manufacture (e.g. PCB dielectric constant, copper lossiness, etc.), to meet the electrical design criteria for the PCB, and comes up with a first pass at the layout. The field solver then automatically extracts the draft PCB layout’s parasitics (partial and mutual inductances, stray capacitances, flight times, etc..) and sends them to the circuit simulator. The circuit simulator adds the PCB’s electrical characteristics to the circuit the designer captured, and re-simulates it to see if it still functions within specification. The designer then makes the appropriate modifications, where necessary, to make the circuit simulate correctly again.
The PCB’s electrical characteristics are an important part of the ‘hidden schematic’, which also includes the complex behaviour of the active and passive devices at high frequencies (which should have already been entered in to the circuit simulator). The hidden schematic for even a simple circuit is at least an order of magnitude more complex than the circuit that is drawn on a typical schematic or circuit diagram. For a complex circuit it can be two orders of magnitude larger.

When a PCB electrical parameter is out of specification, there are often a great many possible contributors. The task of discovering which ones to vary to achieve the specification can seem daunting, but ‘sensitivity analysis’ comes to the designer’s rescue. Circuit simulators and field solvers permit complex ‘what if’ investigations, and these can be used to discover the sensitivity of the chosen parameter (e.g. overshoot height, trace impedance, crosstalk, decoupling inductance) to the various physical design issues. Sensitivity analyses helps to avoid wasting time over insignificant issues, setting overly tough PCB fabrication tolerances, or having to do multiple ‘trace tuning’ PCB iterations.

The virtual design is iterated between the circuit simulator and the PCB field solver until both designers are happy with the result. This iterative process usually only applies the field solver to the critical areas, because at the time of writing it takes too long to run a full solver analysis on a typical PCB. But before the PCB’s layout is released for its first prototype manufacture it is fully simulated in the field solver and all of its parasitics fed back to the circuit simulator to prove that the circuit still simulates correctly. Now the first prototype of the PCB is virtually guaranteed to have no errors and to function correctly without signal integrity problems, for nominal specification components.

Of course, devices with nominal specifications hardly ever occur, and all device parameters vary with temperature (e.g. switching rise and fall times are shorter at lower temperatures). So
to prove that the design will give an acceptable yield in volume manufacture, and be reliable enough when exposed to temperature variations in real life operation – the circuit simulator performs Monte-Carlo analysis or parametric sweeps on the components' tolerances, plus temperature analyses on the components' temperature coefficients, on the final design.

Figure 1L shows an example of a virtual PCB design project flow.

The virtual design process as described above can really only ensure signal integrity and assist the achievement of reliability and lower warranty costs (at the time of writing). It cannot (yet) be used to ensure EMC compliance. But because high-frequency signal integrity issues are also EMC issues, it is possible to use this methodology to help ensure adequate EMC performance.

There is, of course, a learning curve associated with these circuit simulators and field solvers, and of course there is the business of developing a model library that includes not only the 3-dimensional attributes but also all the high-frequency behaviour of the components, the tolerances of their various parameters, and their temperature coefficients. And, of course, suppliers can be late delivering the latest version and there can be bugs in the software, and nothing ever goes as smoothly as we would like (Murphy's Law applies to all human
endeavours). So, if it intended to use virtual design on a new project, sufficient time must be
allowed for the acquisition of the software, development of the models and training of the staff,
and to allow for the normal operation of Murphy’s Law.

Virtual design as described above is now possible with relatively easy-to-use packages that run on a modern PC. Of course, they are not cheap, but they are very reasonable when compared with the true cost of even a single iteration of all the schematics and PCBs on a single product, especially if that design iteration could occur at a late stage in a project. Compared with the true cost of being late to market, most companies could afford the very best simulators and field solvers, high-power workstations to run them on, and training courses for the staff that will use them.

4.3 Experimental verification

Models are never 100% accurate, and they don’t model everything. Simulators are never 100% accurate and the assumptions they have made in order to achieve reasonable computation times might not be appropriate in all circumstances. And of course virtual design methodology cannot yet be fully applied to EMC due to the complexity involved in simulating the EMC of a real PCB with its cables and enclosure.

Considering figure 1A, we can see that we really must not leave any technical risks beyond a certain point in a project – so experimental verification is recommended for all risky design issues (which we might call potential “show-stoppers”). The risky circuit areas and their PCB layouts should be physically created and tested, as early in a project as possible.

Ideally, impedance analysers, network analysers, and time domain reflectometers would be used to prove the design of the risky area, and some very commercial companies are equipped with many hundreds of thousands of dollars worth of such equipment, plus sophisticated probing devices that can operate to many GHz, just for this purpose.
But even if the only equipment that is available is fast oscilloscopes (with suitable high-frequency probing techniques), bit error rate testers, and other equipment likely to be found in the typical electronics company, quite a lot of useful de-risking information can be obtained from an experimental PCB. Specialist instruments such as network analysers can be hired, but getting useful results from them may require a learning curve.

To improve reliability in the field, experimental circuits can be tested with forced cooling and heating of the experimental PCB. To improve yields in volume production is more difficult, as a wide variety of components with different tolerances are usually not available, and if they were, substituting them would take too long. But testing experimental circuits whilst cooling and heating individual devices considerably beyond their anticipated ambient range (e.g. from -40 to +120 degrees Celsius, taking care to avoid damage to scarce samples) will vary some of their parameters over a wide range and can help achieve a good yield in volume production.

5 References


I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than the series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named in a magazine article like this, but the following names stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to all of the excellent people and companies that I have left out.

Some useful textbooks and other references are:


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Advanced PCB design and layout for EMC.

Part 2 – Segregation and Interface Suppression

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the second in a series of eight articles on good-practice EMC design techniques for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time to market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (”Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. This series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not bother with why these techniques work, they will simply describe the techniques and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

Part of this article is very similar to the paper: “GHz Shielding at PCB level” presented by the author at the IEE’s event: “New EMC Issues in Design”, held at Qinetiq, Farnborough, on the 28th of April 2004.

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2.1 Reasons for shielding on the PCB

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1 Introduction to advanced segregation

Segregation is one of the most cost-effective PCB techniques, and was described in Part 5 of [1]; Part 5 of [2]; [3] and Volume 3 of [5]. The advanced segregation techniques described in this article employ the same analyses of the interface between the \textquote{inside} and \textquote{outside worlds},
and between the ‘noisy’ and ‘sensitive’ zones on the PCB, but employ more attention to the
details of the shielding and filtering.

It is always a good idea to plan for the worst case shielding and filtering that might be required
around each segregated circuit zone, in case it is required. Equipment can be
‘pre-compliance’ EMC tested without it’s shielding and with minimal PCB filtering fitted, with
the extra shielding and filtering parts (that it is hoped will not be required) readily available in
case they are needed to pass the tests. If the EMC test is failed, the shielding and filtering can
quickly be upgraded with the aid of a soldering iron, and the equipment retested without
significant delay, to find the minimum configuration that passes the test or at least to help
identify where the problem area lies. This can save months of time compared with the usual
scenario, in which PCB ‘respins’ are required each time it is suspected that additional
shielding and/or filtering is required to pass an EMC test.

Shielding and filtering work together to create high-performance segregation. High levels of
shielding will not be achieved without filtering, and high levels of filtering will not be achieved
without shielding, especially at frequencies above 100MHz.

2 PCB-level shielding

General shielding issues are described in Part 4 of [1]; Part 4 of [2]; Volume 2 of [5] and
Chapter 8 of [21]. PCB shielding employs the same general design, but issues and design
details more relevant to advanced PCB segregation are described in this section, and in
sections 3, 4 and 5 below.

2.1 Reasons for shielding on the PCB

There are many good reasons for using shielding techniques at PCB level. The most obvious
one is that shielding at the lowest level of assembly – the PCB – costs the least and adds the
least weight. Shielding at the level of the module or enclosure costs at least ten times more
than shielding at PCB level, refer to Figure 1B of [22].

![Figure 2A  Example of PCB-level shielding in a cellphone](image)

The continued miniaturisation of surface-mounted devices (SMDs) and the increasing density
of PCBs, are making it more necessary to shield different zones of a product from each other,
to achieve the desired levels of functional performance in the product.

The continued shrinking of the silicon features in ICs is making them more susceptible to
signal degradation. PCB-level shielding is a low-cost way to enable modern ICs to operate
reliably in the noisy environment inside a typical modern electronic product.

When integrating wireless (radio) communications with a product, the close proximity of very
‘noisy’ transmitting antennae tends to cause interference with sensitive circuits elsewhere in
the product (analogue and digital devices can both be susceptible). The close proximity of
very sensitive receiving antennae to ‘noisy’ circuits such as switch-mode converters and
digital processing can reduce the range over which the wireless communication will work.

PCB-level shielding is a valuable technique for wireless communications.

Many modern portable computing devices are equipped with a variety of wireless data
communications (such as Bluetooth, IEEE 802.11) but have no visible antennas because they
are mounted inside the product’s enclosure. The enclosure clearly cannot be shielded, and PCB shielding techniques are used instead.

Regulatory issues are also significant. As ICs’ silicon feature sizes decrease, digital and switch-mode power devices switch faster. Digital processing speeds are also continually increasing. The result is that modern electronic products are increasingly emitting significant levels at frequencies exceeding 1GHz. But the spectrum above 1GHz is increasingly being employed for personal communications, so regulatory emissions standards are moving to protect the radio spectrum up to 2.7GHz (in Europe) and beyond.

Modern product enclosures are perforated with increasingly large visual displays, connectors for numerous kinds of cables, slots for a wide variety of removable storage media, apertures for ventilation, and must be constructed with a number of joints for ease of assembly. At higher frequencies, constructional issues that were once negligible can seriously compromise shielding effectiveness (SE). PCB-level shielding-can be used to reduce the SE requirements for the overall enclosure, possibly even completely removing the need for enclosure-level shielding.

2.2 Overview of shielding at PCB level

Figures 2B and 2C provide an overview of the issues associated with PCB shielding. A five-sided conductive ‘shielding-can’ is placed over a circuit zone on a PCB, and electrically bonded by via holes in the PCB at multiple points around its perimeter to a plane layer inside the PCB (or on its bottom layer). The result is a six-sided conductive enclosure, part of which is embedded in the PCB itself.
The plane layer used is usually at 0V potential, but could be at any potential. Traces that enter or leave the shielding-can must be either shielded or filtered (Figure 2B only shows filtered traces). If the plane is on an inner layer of the PCB, the traces and devices on the other side from the shielding-can are not shielded. If a circuit to be shielded has devices fitted on both the top and bottom of a PCB, both sides can be fitted with shielding-cans (and PCB plane layer may not always be required). But double-sided shielding-cans are more awkward for automated assembly.

Where the devices on the top and bottom of a PCB are associated with different circuits, they can be isolated from each other (to some degree) by using an internal PCB plane layer. It is also possible to fit shielding-cans over both of these circuit zones, each one using the same plane layer as its sixth side.
Unfortunately, when using through-hole-plate (THP) PCB construction, the plated-through holes associated with the circuits on one side of the plane layer will protrude into the shielded volume on the other side of the plane layer, where they will ‘crosstalk’ into its circuits. Also, the perforations in the common plane layer due to the clearance holes around the through-holes will reduce the SE between the top and bottom shielded volumes.

Microvia PCB technology allows the achievement of much better isolation between two shielded volumes on opposite sides of a PCB, because it uses ‘blind’ and ‘buried’ plated holes that do not pass completely through the PCB. The use of microvia PCB construction (also known as high density interconnect [6], or sequential build-up) makes it possible for plane layers not to be perforated at all. Figure 2D shows the general principle.

PCBs constructed using microvia technology can achieve very high levels of isolation between circuits assembled on opposite sides of a PCB with an unbroken internal plane layer between them.

2.3 Types of PCB shielding-can

Traditionally, PCB shielding-cans have been made of sheet metal, such as tin-plated steel, brass or beryllium copper. They had multiple pins around their perimeter for soldering into plated through-holes, and they usually had clip-on lids so that the devices inside could be
accessed. The clip-on lids used multiple spring fingers around their perimeters to help minimise the resulting ‘leaky’ shield gaps. They were also available with internal dividers that could shield two or more zones of circuitry from each other.

Surface-mounted metal shielding-cans have become readily available in recent years, and cans of up to 50mm square are successfully assembled automatically at the same time as other SMD parts. A number of alternative designs are now available (or are being developed) to reduce weight and cost. Also, shielding-cans with reduced ‘environmental impact’ are becoming available.

Metal shielding-cans without removable lids cost and weigh less, and have better SE because they have fewer apertures. Laird Technologies has a design that allows the top of the shielding-can to be removed with a ‘key’, just like opening a traditional oblong tin of sardines.

To repair the shielding-can, a new metal lid with conductive adhesive is pressed onto its body. A variation on the shielding-can made from sheet metal is the die-cast metal ‘maze’ base that is soldered or press-fitted to the PCB and has metal spikes along its top edge. A flat metal lid with holes at appropriate places is pressed onto the base. An example of a PCB using this technique is shown in Figure 2E.
Plastic moulding techniques have recently become a vigorous area for research and developments. Formed plastic shielding cans have for years been painted with conductive adhesive, or had metal layers applied by vacuum deposition (such as sputtering) or electro-plating. But the tooling costs for the automated conductive coating of such parts can be high, or they can require costly manual processing.

One alternative is to print a flat sheet of plastic with a mesh or solid layer of conductive ink, usually silver [7] [8], or to plate it with metal [9] [10]. The conductively coated sheet is then cut and thermo-formed into the desired shape. The difficulty is in designing the ink or metal film so that it can stretch enough to make a wide range of PCB-level shielding shapes without cracking, since this creates apertures and reduces the SE.

Conductively coated plastic parts can be used just as they are, if stiff enough, but some types will need mechanical assistance, such as being clipped into a plastic or metal support (often created by the internal shaping of the product’s enclosure). An alternative is to use the thermo-forms made from the conductively coated plastic sheets as ‘preforms’ for a plastic moulding process. This is sometimes called “in-mould shielding”, with the shielding preform being moulded into the finished component, thereby avoiding the need for manual assembly.

Instead of using conductively coated plastic sheets as preforms, some companies [11] are using metal plated carbon fibres in in-mould shielding processes. (Note that loading the plastic material used for the injection moulding process with conductive material is not very successful, as the resulting parts have non-conductive resin-rich surfaces.

**2.4 Attaching shielding-cans to PCBs**

Traditional through-hole metal shielding-cans are often soldered to their ‘sixth side’ plane in the PCB using manual methods. Wave soldering can be used in volume manufacture, but the thermal inertia of the metal shielding-cans add to the difficulties of setting up the process.
Surface-mounted metal shielding-cans are intended for automated assembly using reflow soldering methods, and usually have patterns of small holes to aid temperature equalisation [12].

High-performance metal shielding-cans are often required to be ‘seam-soldered’ to a plane layer (or guard trace) on the top of the PCB [13]. Like other types of surface-mounted shielding-cans, larger sizes would usually employ two or more pins to locate them with appropriate through-holes in the PCB.

Soldered metal cans require holes to prevent ‘popcorning’ – thermally induced changes in their shape that weaken the solder joints. But these holes affect the SE that can be achieved, so there are performance benefits to be had by not using soldered-in metal shielding boxes.

Conductive gaskets can be used with metal or shielded plastic shielding-cans. Die-cut gaskets with double-sided conductive adhesive, or formed-in-place conductive gasket glue (usually based on silicones or epoxy resin), can be used to retain shielding-cans to the PCB – as well as electrically bonding them to the PCB plane layer used for their sixth side.

Non-adhesive conductive gaskets require some other means of retaining the shielding-can, such as a plastic clip. Some PCB shields are held in place by features in the product’s enclosure (either base or cover), and fall off when the enclosure is removed. Of course, gaskets do not always need to provide a continuous bond around the perimeter of a shielding-can wall, and dots of gasket can often be used instead.

An interesting recent development in conductive gaskets is the “Gore-Shield GS5200 thermal and electrical grounding pads” [14]. These are surface-mounted soldered components with a compliant layer of thermally and electrically conductive gasket material on their upper side. Arranged around the perimeter of a shielding-can, they not only provide electrical bonding to the sixth side’ plane layer, they also help remove heat from devices inside the shielding-can.
Another method of electrically bonding plastic shielding-cans to a PCB is to design the plastic part so that it has ‘bumps’ in its conductive surface that are individually compliant enough to ensure that each one will reliably press against appropriate traces and pads on the surface of the PCB [15]. The bumps could be the sites for form-in-place gasket dots, or they could be designed as ‘spring fingers’ requiring no gaskets. This technique needs no soldering or conductive gaskets, but requires some means of holding the part in place, as for the non-adhesive gaskets described earlier.

By using plastic materials that will withstand soldering temperatures, plastic shielding-cans can be soldered onto PCBs just like surface-mounted metal cans. They have the advantage of not requiring ‘anti-popcorning’ holes; so can be designed to provide higher SE levels.

Gore have developed what they call the “snapshot shield™” [15] [16] that uses a thermoformed plastic part post-metallised on its outside. Where it meets the PCB it has a small flange with holes in it. To assemble it to the PCB, standard ball-grid-array (BGA) solder balls are deposited on the PCB at the locations of the holes, and during soldering capillary action makes the balls ‘snap’ through the holes and make contact with the outer metal layer, whilst also retaining the shield in place. The advantage of this over regular surface mounting appears to be that since the inside of the shielding-can is insulating, it is less likely to short out components and traces by accident.

2.5 PCB shielding-can materials

PCB shielding-cans have traditionally been made from stamped, drawn or folded sheet metal, but a wide variety of alternative materials are now available (or are being developed) to reduce costs, ease assembly, or reduce environmental impact. Shielding-cans can now also be made using conductive ink printed onto a variety of substrates (e.g. plastic), meshed
patterns of conductive ink on substrates, metal meshes (with or without substrates), metal films deposited onto plastic substrates, etc.

Where meshes are employed the SE will degrade above a frequency governed by the size of the apertures in the mesh. There is a complex relationship between mesh size and shape, SE and frequency [17] with larger mesh sizes giving poorer SE. Meshes for GHz shielding will almost always be less than 3mm on a side.

At frequencies above 100MHz, even metal films 1 micron thick can give high values of shielding [18], so the conductive material used is usually not important for SE. However, all practical shielding-cans have their SE limited by apertures and interconnections. These issues are described below.

2.6 Apertures and gaps in shielding-cans

Apertures in shielding-cans include seams in folded metal constructions; holes for adjusting components; holes that help prevent ‘popcorning’ during automated soldering (that would weaken the soldered joints); and the spacings between the electrical bonds between the main body of the can and the PCB plane layer on its sixth side. The apertures in the plane layer caused by the clearance holes around plated through-holes have already been mentioned. Apertures in shields must be much smaller than the wavelength of the highest frequency for which shielding performance is required. A shield with a single aperture, that has a diagonal size of one-hundredth of a wavelength, can be expected to achieve an SE of no more than 34dB at the corresponding frequency, as shown by Figure 2F.
The wavelength ($\lambda$) in air of a frequency, $f$, is $300/f$ mm (when $f$ is in GHz). The wavelength inside a PCB is about half of this, due to the dielectric constant of the PCB substrate (e.g. FR4) slowing the velocity of electromagnetic propagation to about half that of free space, within the PCB itself.

Every time the number of apertures on one face of a shielding doubles, the SE in the direction perpendicular to that face falls by up to 6dB. So if there were 8 identical apertures on one face of a shielding-can, each one having its longest dimension equal to $\lambda/100$ at the highest frequency of concern, the SE perpendicular to that face, at that frequency, should not be expected to be any higher than 16dB at the corresponding frequency.

The apertures created in the shielding-can by its electrical bonds to the inner plane layer partly lie in the air above the surface of the PCB, and partly lie inside the PCB, where the wavelength at a given frequency is about half of what it is in air. So to determine the spacing of these bonds, it is best to assume that the whole of each aperture is in the PCB material, and use a bond spacing that is half of what we would assume for apertures that were wholly in the air.

For example, if it were required to achieve 20dB of SE at 3GHz in any direction around a 50mm square shielding-can, we would firstly note that the wavelength at this frequency is
100mm in air and 50mm inside the PCB material. A single aperture of 1mm diameter in air, or 0.5mm inside the PCB, would limit the maximum achievable SE of one face of the shielding-can to 34dB, so 7 apertures should result in 20dB.

Since the shielding-can is 50mm along each side, using an electrical bond spacing to the plane layer of 0.5mm would result in 100 apertures along that edge – many more than the maximum of 7 permitted by our 20dB specification. This situation is dealt with by using a plane layer (or wide ‘guard trace’) on the same surface of the PCB that the shielding-can is to be fitted, and electrically bonding the wall of the shielding-can to that layer (or trace) along its whole length. “Seam-soldering” is the traditional way of doing this for metal cans, but conductive gaskets or conductive glue can be just as good.

Now the electrical bonds to the inner plane layer do not create apertures in the air above the surface of the PCB. But we still have a problem with the apertures created by the spacings of the via holes between the guard trace and the plane layer inside the PCB. Using normal THP PCB techniques it is difficult to space them much closer than 1mm, but waveguide-below-cutoff techniques (see below) can be used to improve their SE considerably.

2.7 Waveguide-below-cutoff methods

So far, the apertures that have been discussed were assumed to be of negligible material thickness compared with their length or width. But where an aperture’s length or width is less than one-tenth of a wavelength, increasing its thickness will reduce its ‘leakage’, improving the SE of its shielding-can.

Real benefits for SE begin to occur when the thickness of the aperture (the distance the electromagnetic fields must travel to get from the inside of the shielding-can to the outside) is comparable with the diagonal or diameter of the aperture. The cut-off frequency of a
waveguide in GHz is given by \(150/g\) where \(g\) is the longest dimension of the gap (diagonal, or diameter) in millimetres. The attenuation of a waveguide below cutoff, at a frequency below 60% of the cutoff frequency, is estimated by \(27d/g\) dB where \(d\) is the depth of the waveguide.

Figure 2G gives a few examples.

![Figure 2G: Some estimated waveguides below cutoff](image)

When the frequency to be shielded is above 1GHz, the apertures in the shield will usually need to be less than 3mm in air, or 1.5mm inside the PCB, and waveguide-below-cutoff techniques can be used without sacrificing too much PCB area.

In the above example of a shielding-can with an SE specification of 20dB at 3GHz, we had a problem with the spacing of the through-holes that provide the electrical bonds between the plane layer (or guard trace) on the top surface of the PCB and the plane layer that provides the sixth side of the shielding-can. If the vertical spacing between the planes (or guard trace and plane) was 1.6mm and we used a 1mm spacing laterally between the via holes, the diagonal of the resulting apertures would be about 2mm, giving a cutoff frequency around 37.5GHz (assuming a 50% velocity of propagation inside the PCB) – well beyond the 3GHz we are concerned about.

A 6mm overlap between the top plane (or guard trace) and the inner plane would achieve an SE of about 81dB for each aperture at 3GHz. The 50mm side of the shielding-can requires 50
of these 1mm wide apertures, and this quantity would reduce their overall SE by about 34dB to about 47dB. Compared with the 20dB SE specification this is a very good figure, showing how effective the waveguide-below-cutoff technique is.

Note that the waveguide-below-cutoff created by the plane (or guard trace) on the top surface plus the layer providing the sixth side of the shielding-can, can extend inside or outside its wall, or lie partially inside or outside.

As well as the waveguide-below-cutoff technique being used inside the PCB, it can be used to reduce the effects of apertures in the rest of the shield can. It is important to note that no conductor should be routed through a waveguide-below-cutoff aperture – to do so would reduce its SE to zero.

2.8 Near field effects on shielding

The above discussions and Figures assumed that the fields to be shielded from were all ‘far fields’ (sometimes called plane waves) – and this is usually the case when designing a shielding can for protection against the RF fields generated during an immunity test (e.g. when testing according to IEC 61000-4-3).

But when the apertures are in the ‘near field’ regions of the sources (are within one-sixth of a wavelength at the frequencies of concern) the SE is very much less that that calculated assuming far field conditions [25]. The near field is the normal situation when using a PCB mounted shielding can to reduce the emissions from devices or the traces associated with them.

Determining the SE of a shielding can with apertures that are in the near field requires sophisticated computer simulation using modelling software that has been calibrated for such purposes (tested and proved against real-life measurements). Alternatively, simple test
set-ups can be created and tested in a laboratory well in advance of PCB layout (e.g. using simple loop and wire antennas driven from a signal generator).

However, the results in [25] point to three design guides:

a) If the SE for a device or trace is to be 40dB or more, keep the spacing between the device/trace and the shielding can’s apertures >> 2L, where L is the longest dimension of the apertures.

b) Minimise all aperture dimensions

c) Space the apertures as far apart from each other as possible

When using THP PCB technology, the PCB plane that generally forms one side of a shielded enclosure on a PCB is almost always perforated with ‘antipads’ (clearance holes) around numerous via holes. These antipads are typically 1mm or so in diameter, and of course are very close to other traces and PCB-mounted devices, so will limit the maximum attainable SE as far as emissions are concerned, even when the shielding can has no apertures and is seam-soldered to a top-side plane.

For the best PCB shielding, unperforated planes are required, and this means using HDI (microvia) PCB technology instead of THP, and this is discussed in Part 7 of this series.

### 2.9 Cavity resonances

Resonances (standing waves) can occur within the cavity formed by a shielding-can at frequencies at which whole numbers of half-wavelengths will fit between its sides. They can be calculated (in GHz) by:

\[
f = 150 \sqrt{(l/L)^2 + (m/W)^2 + (n/H)^2}
\]

– where: \(l, m, n\) are integers (0, 1, 2, 3, etc.) and \(L, W, H\) are the box’s length, width, height (in millimetres) respectively. Usually we are most interested in the lowest resonant frequencies of the longest dimensions, when \(l = 1, m = 0, n = 0\) (when the general equation simplifies to: \(f =\)
150/L), or when \( l = 0, m = 1, n = 0 \) (when the general equation simplifies to: \( f = 150/W \)). For example, a 50mm by 30mm box will have its lowest resonant frequencies at 3GHz and 5GHz, in its length (L) and width (W) directions respectively.

Resonances inside shielding-cans cause local amplification of their internal electric and magnetic fields at ‘hot spots’ within the shielding-can, and these increase the coupling between circuits covered by the same shielding-can. Figure 2H shows the coupling measured inside one example of PCB shielding-can [15] [16].

![Figure 2H](Image)

Also, the SE of a shielding-can is reduced at its internal resonant frequencies, with 20dB reduction being recorded by [15] [16]. This reduction in SE appears to be due to locally intense fields (hot spots) being near to apertures and conductor penetrations, causing them to leak more. Figure 2J shows the SE of the same PCB shielding-can that was measured for Figure 2H.
So it is best to use shielding-cans that have length and width dimensions much smaller than half a wavelength at the highest frequency of concern, to prevent internal resonances from occurring in the frequency range concerned. Multiple shielding compartments can be formed in one shielding-can component to increase resonant frequencies, and also to help reduce interaction (crosstalk) between circuits [16].

If it is not practical to avoid shielding-cans that are resonant within the frequency range of concern, then square (and cube) shaped structures should be avoided – as should structures with simple relationships between length, width and height (for example: 3:2:1). This is because at some frequencies such shapes will suffer from resonances due to their length and width together (or any two or three of the dimensions L, W and H). The amplification of internal fields at hot spots at these frequencies will be especially intense, and more likely to lead to undesirable results.

Ratios between L, W and H should ideally be irrational numbers, such as \( \pi \) (1.414….etc.) or the ‘Golden Mean’ (1.618….etc.), to help prevent coincidence of resonances. It will also help if the opposing sides of the shielding-cans are not parallel, but this technique is not often used, maybe because it does not result in a very pleasing appearance for a PCB assembly.
Another useful technique where cavity resonances in a shielding-can are potential problems is to use microwave-absorbing materials, such as Q-Zorb from Laird Technologies [18]. These are elastomers loaded with ferrite particles, usually a millimetre or two thick, glued to the inside of the lid of a shielding-can. These convert magnetic fields into heat, thereby damping down both the electric and magnetic field resonances within the shielding-can.

3 Interconnections and shielding

If the SE of a shielded volume is not to be degraded, all of the conductors penetrating its boundaries must either be shielded or filtered.

Where a conductor is shielded, their shield must bond along the full perimeter of its interpenetration with the shielded volume. Since we are discussing shielding on a PCB – traces are shielded if they run between two plane layers that bond to all of the via holes around the perimeter of the shielding-can. These two plane layers must be electrically bonded together with plated-through via holes, and it is recommended that these vias should be no more than λ/30 apart (for example, no more than 10mm for frequencies less than 1GHz), preferably much closer.

Where a shielded cable enters or leaves a PCB shielding-can, its connector or gland must make a direct electrical connection all around the perimeter of its aperture in the shielding-can, and also all around the perimeter of the cable’s shield. This is sometimes known as 360° shield bonding. Shielding is best thought of like plumbing with copper pipes – joints must either be 360° soldered or use compression joints that achieve 360° metal-to-metal contact. Plumbing that falls short of this will leak water, and shielding that falls short of this will leak radio frequency energy and so reduce SE.

It is possible to make a fully shielded PCB assembly, using plane layers on the top and bottom of the PCB, stitched together with a ‘via wall’ all around the perimeter of the PCB, plus fitting
shielding-cans over all the exposed devices and traces. Of course, such a PCB will only employ 360° shielded off-board interconnections.

3.1 Combining PCB shielding with filtering

Where a conductor is filtered, its filter must be located with its midpoint aligned with the point of the conductor’s penetration of the shielded volume, so that its input and output terminals lie either side of the shield – one terminal inside the shielding-can, and one outside.

Also, the radio frequency reference voltage (often called the ‘ground’) of the filter must be the shield’s surface at the point of the conductor’s penetration. So-called ‘feedthrough’, or ‘through-bulkhead’ filters are required. Leaded feedthrough filters are traditionally used, but require manual assembly. Modern automated assembly requires the use of surface-mounted devices (SMDs), such as those shown in Figure 2K.

![Leaded screw-in feedthrough filter (Requires manual assembly) Surface mounted feedthrough capacitor filter (Suitable for automated assembly)](image)

Leaded feedthrough filters are screwed or soldered into appropriately dimensioned holes in the shielding-can. But SMD types lie flat on the PCB and protrude through small apertures in the bottom edge of the shielding-can’s wall, as shown in Figure 2B. The holes for the filters are known as ‘mouseholes’, for reasons that are obvious to anyone familiar with ‘Tom and Jerry’ cartoons.
Figure 2L shows that the filters’ centre terminals must be soldered to the guard trace that follows the perimeter of the shielding-can. Each feedthrough filter must be symmetrically placed with respect to the via holes on each side of it (the vias link the guard trace and the wall of the shielding-can to its sixth side PCB plane).

Figure 2M shows the very beneficial effect of the shielding-can on the filtering performance of an SMD feedthrough filter. Such filters need to be combined with a shielding-can to achieve any significant filtering performance at frequencies above 1GHz.

Figure 2N shows how a device (such as an A/D converter, opto-coupler, CM choke or filter array) might cross the boundary of a shielded zone. Of course, as sketched, the device is of the type that has all of its input pins along one side, and all of its output pins along the other,
so that it can be placed so as to 'straddle' the 0V guard trace (and have a mousehole cut in
the shielding-can to go over it).

Devices for which the pins are not so conveniently arranged can be more difficult to employ
successfully on high-performance PCBs or PCBs with advanced EMC characteristics – so the
pinout of such ‘zone interconnecting’ devices should be made an important consideration
when selecting devices early in a project.

Figure 2N sketches the construction of a PCB assembly that is shielded and filtered. In some
circumstances such an assembly might not need any further EMC measures, apart from a
plastic box or other means to prevent electro-static discharges occurring directly to its
unshielded components.

Figure 2P sketches the construction of a PCB assembly that is shielded and filtered. In some
circumstances such an assembly might not need any further EMC measures, apart from a
plastic box or other means to prevent electro-static discharges occurring directly to its
unshielded components.
Sometimes adequate EMC performance can be achieved solely by the use of the filters or shielding-cans. It may be worthwhile experimenting, during EMC testing [19], with lower-cost three-terminal filters, feedthrough capacitors, ferrite beads, or even zero-ohm links – so it helps to ensure that the pad patterns for the filters will accommodate a variety of such devices.

4 Combining shielding with heatsinking

Some modern ICs dissipate significant amounts of heat, and require heatsinking. Where PCB-level shielding is also required, shielding-cans are combined with heatsinks. The metal base of the heatsink becomes the lid of the shielding-can, so the shielding-can on its own is little more than a four-sided shielding wall – with its bottom face completed by a PCB plane layer – and its top face completed by the base of the heatsink. Figure 2R shows a cross-section of an example based on a spring-finger type of ‘picture frame’ shield that is simply held in place by the heatsink (it will probably need a couple of locating pins with matching holes in the PCB). The clip or other construction that holds the heatsink in place is not shown.

![Figure 2R Example of heatsink combined with shielding](image)

The base of the heatsink must have a highly conductive surface using metals chosen so that they will not corrode after years of contact with the shielding wall. The heatsink is usually not
soldered to the shielding wall (although this could be done under certain circumstances).

Normally, all the various ‘pressure sensitive’ techniques that can be used for attaching shielding-can walls to PCBs can also be used to electrically bond the walls to the base of the heatsink. The spacing rules for the electrical bonds between the shield wall and the base of the heatsink are the same as those (above) for bonds between the shield wall and the PCB’s 0V guard ring and internal unbroken plane, the 6th side of the shielding volume.

5 Environmental issues

Two European Directives concerning the protection of the environment (known as WEEE and RoHS) will come into force in the European Union in 2006, with at least one other (known as EuPD) planned before 2010. The RoHS Directive will ban the use of tin-lead solder, and most people will go for tin soldering instead which may effect the choice of components available for use in filtering. But both of these directives will influence the type of shielding used, and the materials used in shielding-can construction.

The volatile chemicals used in some conductive coating and electro-plating processes have a negative environmental impact, and these processes tend to make the coated materials difficult to recycle [20]. Vacuum metallisation is claimed to be more ‘eco-friendly’, and tin and aluminium are non-toxic and easy to recycle. So vacuum metallised plastic shielding-cans (employing tin or aluminium) that are pressed, clipped or soldered into place, may have fewer environmental disadvantages than some other plastic shielding techniques. Thermo-formed shielding inserts aid the recycling of plastic enclosures [8]. Surface-mounted metal cans are easy to remove and recycle [12].

6 PCB-level filtering

6.1 Reasons for filtering on the PCB
The reasons for filtering at PCB level are very similar to those described in section 2.1 for shielding at PCB level, and will not be repeated here.

Section 1 above said that shielding and filtering work together to create high-performance segregation. High levels of shielding will not be achieved without filtering, and high levels of filtering will not be achieved without shielding, especially at frequencies above 100MHz (made especially clear by Figure 2L above). So it is important to note that as problem emissions and immunity frequencies continue to increase and go beyond 1GHz, and as pressure on costs and timescales continues to increase, careful design of PCB filtering will increasingly be required.

6.2 Overview of PCB filtering

General filtering issues are described in Part 3 of [1]; Part 3 of [2]; Volume 2 of [5] and Chapter 8 of [21]. PCB filtering employs the same general design, but issues and design details more relevant to advanced PCB segregation are described in this section, and section 7 below.

A number of basic single-line single-stage filter types are available...

- series resistor (R) or series inductor (L)
- shunt capacitor (C)
- resistor-capacitor (RC) or inductor-capacitor (LC)
- resistive Tee (RCR) or inductive Tee (LCL)
- capacitor-resistor (CR) or capacitor-inductor (CL)
- resistive Pi or π (CRC) or inductive Pi (CLC)

When filtering frequencies above a few MHz, soft ferrite 'supresser' ferrites are generally used instead of inductors, although they are shown on schematics by the same symbol.

Common-mode (CM) noise is usually the major cause of high emissions and poor immunity between 1MHz and 1GHz. When filtering more than one conductor, CM chokes wound on a
soft-ferrite cores generally provide better attenuation of RF CM noise than a row of individual soft ferrites, so it is best to layout PCBs so that selected CM chokes can be fitted instead of a row of individual resistors or ferrites (see Figure 2S below), double-padding if necessary. If it turns out that a CM choke is necessary (although, due to its higher cost, it was hoped that it wouldn’t be) this little bit of forethought will save the many weeks delay and the cost of a board ‘respin’.

The above filter types can be combined together to create multistage filters with greater attenuation. For EMC use, most low-power DC, analogue and digital signal filters rarely seem to need to use more than a single stage filter. But filters for equipments’ AC supplies (mains inputs) and filters for pulse-width modulated (PWM) and other semiconductor power controlled outputs may need to use multi-stage filters to pass regulatory or contractual EMC tests.

Section 6.4 below describes PCB layouts for all low-power DC, analogue and digital signals that enter or leave a PCB via ‘off-board’ cables. Similar design considerations apply to all filters used on traces between circuit zones within a PCB (e.g. Figures 2, 11, 12, 13 and 14) except that the 0V plane should never be gapped or split except as part of an overall EMC plan carefully-designed by a PCB EMC expert.

Gaps and splits in planes are discussed in Part 4 of this series (in a future issue of this Journal), so this issue will not be discussed here, expect to say that gapping and splitting planes was a good idea twenty years ago when most problem frequencies lay below 200MHz, but these days it is generally a very bad idea. Unfortunately most of the application notes for microprocessors, A/D and D/A converters, codecs and the like still seem to be stuck in a ‘traditional’ rut and recommend gapped and split planes despite the significant signal integrity and EMC benefits provided by ‘solid’ (unbroken) planes.
6.3 High-performance filtering requires a good quality RF reference

PCB shielding-cans require an unbroken internal metal plane layer as their 6th side. An unbroken internal metal plane layer also makes a high-quality RF reference for a filter, without which filtering performance will suffer.

We can see that the provision of an unbroken plane layer (usually the 0V plane) allows the implementation of advanced PCB segregation techniques (using shielding and filtering), as well as the many other PCB EMC benefits which will be described in Part 4 of this series (in a future issue of this Journal).

6.4 Design of single-stage low-power and signal PCB filters

In general – where all the items of interconnected equipment are not referenced to large plates of well-bonded metal (as they are in a typical warship or submarine) – the best type of filtering for an unshielded off-board connector/cable has a series resistor or soft ferrite suppresser as its final component before the off-board conductor. An example of a PCB layout for an unshielded off-board connector, using RC or LC filtering with low-cost two-terminal capacitors, is shown in Figure 2S. (Multi-padding so that CM chokes can be used instead of resistors or ferrites is not shown in this Figure.)

Aligning filter components in rows
Figure 2S shows how the ferrites connected to the off-board connector/cable are arranged all in a neat row. This layout detail is most important to optimise the attenuation of these devices at frequencies above 100MHz. Due to the connection density of some modern connectors, it is tempting to stagger the layout of the resistors or ferrites, but this should never be done. Staggering the layout of the ferrites increases the stray capacitive coupling between their filtered and unfiltered terminals – it may not seem like very much extra capacitance but it can be enough to entirely negate their filtering effect.

If achieving a single neat row of resistors or ferrites is impossible, then either smaller ferrite components (0402 sizes are becoming increasingly available) or integrated ferrite arrays should be used, or else the ferrites should be arranged on both the top and bottom of the PCB – with the top row placed exactly above the bottom row.

Arranging the series resistors or ferrites in a row is also necessary to assist with fitting a CM choke instead, if one is required. The input and output connections for a CM choke should always be kept well apart from each other.

The RC or LC filter capacitors are also arranged in a neat row behind the row of resistors or ferrites, with their 0V ends via’d to the unbroken internal 0V plane layer using the shortest fattest traces possible (to minimise their series inductance and improve the capacitor’s high-frequency performance). Via-in-pad techniques are preferred for the 0V terminals of the filter capacitors – easy to achieve when using micro-via PCB techniques (which will be discussed in Part 7 of this series, in a future issue of this Journal) or wave-soldered PCBs. It is generally held that via-in-pad techniques cannot be used with reflow soldering, but some PCB fabricators seem able to achieve this without increased costs and with good yields.

**Filtering the off-board ‘GND’ conductors**
The ‘GND’ connections in the connector/cable are also fitted with pads for ferrites, because it often helps to fit the same type of ferrites in an off-board 0V connection as are fitted in the signal paths. If a CM choke is required it must have all of the off-board conductors routed through it at once (or at least each signal plus its dedicated return conductor in a number of CM chokes), so providing suitable pads for the GND signals will help.

**Cutting back the 0V plane**

Figure 2S shows the 0V plane cut back over part of the filter’s area – in fact it is cut back just as far as the ‘circuit side’ terminals of the resistors, ferrites or CM chokes. This is done because the proximity of the 0V plane to the connector/cable terminals of these components increases their stray capacitance and reduces their filtering performance at high frequencies. Cutting back the 0V plane as shown also helps to prevent unwanted coupling between the noises in the external conductors and the PCB’s reference 0V plane. Sometimes it may be better not to cut back the 0V plane, even though this would compromise the performance of the series resistors, ferrites or CM chokes, as discussed in Section 7.

All of the examples in this section have series resistors; ferrites or CM chokes as their final filter components before the connector/cable. Other types of filters (e.g. Pi) that connect the connector/cable conductors directly through a capacitor to the 0V plane should not use a cut-back 0V plane – the plane should extend right to the edge of the PCB and be ‘webbed’ around the connector/cable connections as described in Part 4 of this series (in a later issue of this Journal).

**No other traces or components in the ‘Connector Zone’**

A dotted area is shown in Figure 2S, called the “Connector Zone”. This is the zone of the PCB dedicated solely to the filtering of off-board (external) conductors. Stray capacitance and mutual inductance between the filter’s components and traces in this zone can completely ruin
the filtering provided for the off-board connector/cable – so no other traces, components or power planes are permitted in this zone, on any layer of the PCB – even if the 0V plane is not cut back as described above.

**Shielding the connector zone**

The “Connector Zone” would be the area covered by a shielding-can, if shielding was found to be necessary (as it might be). Such shielding would be designed according to the sections on PCB shielding-cans above – but in the case of an off-board connector/cable filter zone it would have an open side for the connector or cable.

Where a metal (or metallised plastic) connector panel is used, the open side of the connector zone’s shielding-can must make a multipoint electrical bond to the inside surface of the connector panel – usually best achieved (for low-cost assembly) with a suitable type of conductive ‘EMC gasket’. Even if it is hoped to use a plain plastic enclosure for the PCB with no enclosure shielding, it is still best to design so that metal plated or conductively painted plastic can be used, or else an internal metal foil can be applied, bonded at multiple points to the PCB’s unbroken internal 0V plane as described in Part 3 of this series (in a future issue of this Journal).

**Using shielding to improve filter performance**

The performance of the series resistors, ferrites or CM chokes shown in Figure 2S would be improved if the wall of a PCB shielding-can were aligned with the cut-back edge of the 0V plane, so that the resistors or ferrites protruded through mouseholes in it. The design of the shielding-can would follow Sections 2 and 3 above.

Where a shielding-can was already fitted over the whole connector zone, it should include an internal wall splitting it into two compartments. This internal wall is the one that aligns with cut-back edge of the 0V plane and has the mouseholes for the resistors or ferrites.
Where there is no shielding-can fitted over the whole connector zone, then the shield wall that is used to improve the performance of the series resistors or ferrites could be part of a shielding-can that included the ‘PCB side’ of the filter’s circuitry (maybe also covering other circuit zone), or part of a connector/cable shielding-can that is bonded to the connector panel as described above.

**Tee filtering**

Figure 2T shows how the ‘design rules’, described in detail for Figure 2S above, apply to a Tee filter. The connector zone for this filter type extends to cover at least half of the series resistors or ferrites on the circuit side of the filter. Mouseholed shielding-can walls to improve filter performance could be fitted along the centre of either of the rows of series resistors, ferrites or CM choke(s); or along the row of capacitors. Even better filter performance could be achieved by fitting shielding-can walls along any two, or even all three, rows of filter components. If only one such mouseholed wall was to be used, it would be best located along the row of capacitors.

Figure 2U shows a variant on the Tee filter of Figure 2T, this time using three-terminal capacitors to achieve better filtering at frequencies above 300MHz. Whenever using three-terminal filters a 0V guard trace is required for soldering their centre terminals to, and
there should always be two 0V via holes equally spaced on either side of each device to
improve their high-frequency performance. The provision of mouseholed shielding-can walls
to improve filter performance follows the design rules of Figure 2T, but a wall aligned with the
capacitors should follow their 0V guard trace and be electrically bonded to it according to the
Sections 2 and 3 above.

Figure 2V shows an alternative higher-performance circuit design and PCB layout to Figure
2T, and it could also be an improvement on Figure 2U (depending on the application). The two
current loops associated with the input and output of a Tee filter both share the same
capacitor, and there is inevitable magnetic flux coupling between them that degrades the filter
performance. This would be true even if there were no partial inductances in the capacitor, its
traces or via holes (which, of course, there always is). Figure 2V reduces this coupling by
using two half-value capacitors spaced far apart, so that the current loop associated with the
filter’s input circuit couples less magnetic flux with its output circuit.
The maximum spacing between the two half-value capacitors in Figure 2V is $\lambda/20$ (using the $\lambda$ values for propagation in air, in FR4 it would be $\lambda/10$) at the highest frequency to be filtered; otherwise the current loop between the two capacitors becomes resonant, reducing its benefit.

Figure 2X shows the correct use of an integrated Tee filter, such as the Murata NFE31 series. Integrated Tee filters are three-terminal devices and their centre terminals must be soldered directly to a 0V guard trace as was also shown in Figures 2B and 2L in Sections 2 and 3 respectively, and Figure 2U. Don’t forget that there should be two 0V via holes equally spaced in the guard trace on either side of each filter.

Where it is desired to use mouseholed shielding-can walls to improve the performance of Figure 2X’s filter, it should follow the 0V guard trace and be electrically bonded to it according to the Sections 2 and 3 above.
Figure 2Y shows the use of an IC-style integrated filter. IC filters can be arrays of ferrites, RC, LC, Tee or Pi filters, and their main benefit is that they save PCB space. Resistive RC, Tee, and Pi filters are becoming available made using silicon IC processes (e.g. from California Micro Devices), and this is sometimes claimed to improve their filtering performance at frequencies above 300MHz due to the lower inductances associated with their internal capacitors. It is not obvious where to fit a mouseholed shielding-can wall over an IC filter, so in the absence of any other information it should follow the centre line of the device.

![Figure 2Y Example unshielded off-board connector layout, using an IC filter](image)

The use of integrated filters such as those shown in Figures 2X and 2Y provides less filter choice than discrete filter components such as those shown in Figures 2S, 2T, 2U and 2V, but the PCB space required can be much less so the compromise may be acceptable.

6.5 Power filtering on PCBs

AC supply (mains) and similar high-power filters should follow the same design considerations as described in section 6.4 above, making suitable allowances for the increased size of the components.

SAFETY NOTE: It is very important to correctly design all of the safety aspects of such filters, such as creepage and clearance distances, leakage currents in the protective (earth/ground) conductor, the use of safety approved parts, etc.) – for more on this refer to Volume 4 of [5].
6.6 Filtering for shielded connectors

When using shielded off-board connectors/cables having 360° shield terminations to the unbroken 0V reference plane in the PCB – and at the other end of the cable (see: Part 4 of [1] or [2]: Volume 2 of [5]; Chapter 8 of [21] or Chapter 6 of [22]) – then filters may not be needed at all. If filters are employed they will generally employ capacitors, or RC, LC, or Pi types with the connector/cable conductors firstly connected via a capacitor to the 0V plane, and the 0V lane will not be cut back in the vicinity of the connector.

7 Placement of off-board interconnections

All of the off-board conductive interconnections (e.g. cable connectors) should ideally be located along one edge of the PCB, close together, with no active circuitry located between them. It may be that EMC improvements can be achieved by locating the off-board connectors on two adjacent sides of a PCB, as close as possible to one corner. The purpose of this placement strategy is to minimise the CM potential differences between the off-board conductors, which is a direct cause of emissions.

The provision of a single unbroken 0V plane (often called a reference plane or RF reference plane) in a PCB – plus ensuring that each off-board conductor is electrically bonded to that 0V plane (directly or capacitively) – is an extremely powerful technique for reducing the emissions from off-board conductors. It is described in more detail in Part 4 of this series (in a future issue of this Journal).

Nevertheless, despite the very low partial inductance of such reference planes, the increasingly high frequency currents flowing in them as a result of the use of modern silicon devices can cause significant noise potential differences between one part of the plane and another. If conductors enter or exit the PCB at locations suffering from differing plane noise voltages, they will tend to behave as ‘accidental antennas’ and radiate the plane noise,
thereby increasing the board’s emissions. This is the reason for the ‘connector placement rule’ described above.

If for some reason the off-board connectors have to be placed far apart, or have active components located in areas of the PCB between them, it may be a better compromise not to cut back the 0V plane in the connector area. This would trade off a reduced performance for the filter (see 6.4) with an improved plane inductance for lower CM noise due to plane noise. It is almost impossible to predict which will be best, so experiments with each design may be required to find the best compromise.

8 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques, but in real life there are a great many design trade-offs (compromises) to be made, and this is where the circuit and PCB designers really earn their keep. It is very important for a designer to know all of the compromises he/she is making, and their costs and benefits, to avoid accidentally neglecting an important issue that will cause unplanned costs or delays later in a project – when the true costs of changes are much higher than the same changes made early in a design project, see Figure 1A of [23].

Where any of these “Advanced PCB Design Techniques for EMC” cannot be employed, appropriate problems with EMC must be expected. If the problems are not found to arise on the current project, this does not mean they can be neglected. They will arise on the next project, or the one after that, due to the continuing shrinking of the silicon feature sizes in all transistors and ICs [23] and the increasing density of electronic components on PCBs. The EMC problems caused by neglecting these techniques might manifest themselves as increased development time, poor yield in serial manufacture, difficulties in commissioning
custom-designed equipment, failure to meet regulatory compliance standards, or increased levels of warranty returns, all with their associated damage to company profitability.

So at least use this article as a checklist, and ensure that – where each of its recommendations are not followed – this was a cost-effective technical compromise based on all of the facts. If it is not obvious whether a compromise is acceptable or if it will create more problems than it saves, experiments are recommended at an early stage in the project. EMC experiments might not need to employ EMC test labs or IEC/EN test methods – quite often the relative performance of two options can be judged using the low-cost and quick ‘development’ test methods described in [24].

9 References


I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than this series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named in a magazine article like this, but the following names stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

Some useful textbooks and other references are:


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Advanced PCB design and layout for EMC.

Part 3 – PCB-to-chassis bonding

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the third in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues
A previous series by the same author in the EMC & Compliance Journal in 1999 "Design Techniques for EMC" [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not spend much time analysing why these techniques work, they will focus on describing their practical application and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1. Introduction to PCB-to-chassis bonding

Electronic equipment is typically constructed using PCBs fixed to a conductive chassis. Most PCBs will have an unbroken 0V plane on one layer (and if they don’t, they probably should, see [1] – [5]). There is usually at least one electrical bond, usually at a fixing, between the 0V plane and the chassis, usually near to the external cable connectors if nowhere else, see Figure 3A.
Sometimes galvanic isolation is required between a PCB and its chassis, in which case the bonds are made via suitably rated capacitors. This article discusses the EMC design issues associated with bonding PCB 0V planes to their local chassis.

1.1 What do we mean by ‘chassis’?

The word ‘chassis’ in this article refers to a metal support structure for a PCB, e.g. the wall or floor of a metal enclosure. A shielded metal enclosure makes a very good chassis for a PCB, but a chassis need not be a shield, or even an enclosure – it could just be a piece of metal. For instance, some PCBs with power semiconductors are supported entirely by their heatsink, in which case the heatsink would be considered the PCB’s chassis. In the personal computer (PC) industry, some companies (such as Intel) recommend bonding a motherboard to a sheet metal chassis, which they sometimes call a ‘basepan’ (or even a ‘diaper’, for reasons best known to themselves).

Where plastic housings, enclosures or other structures are used to support a PCB they can be used as a ‘chassis’ in the context of this article if they are made conductive (e.g. by metallisation, conductive painting, or using a conductive filler).
Bonding the PCB 0V plane to its local chassis generally has benefits for EMC; with cast or sheet metal chassis providing the best benefits. Some manufacturers use plain plastic housings and add sheets of metallised cardboard or PVC, or conductively paint or metallise some of their housing’s internal surfaces, as needed, to help pass EMC tests. It is difficult to call a sheet of metallised cardboard or similar a chassis, when it seems more like a shield of some sort, but unless it wraps all around the PCB it is best to consider it as if it is a chassis. When designing an entire item of equipment, the chassis we are discussing here forms part of what is sometimes called the RF Reference Plane – created by bonding all of the different metal (or conductive) parts together using connections that have a very low impedance at the highest frequency of concern. A totally shielded enclosure makes the best RF reference plane, but shielding is not essential.

1.2 What do we mean by ‘bonding’?

For the purposes of this article, the type of bonding that concerns us is ‘RF bonding’ – a low impedance connection at the frequencies of concern for EMC. The word ‘low’ here generally means less than 1Ω, although how low it needs to be will depend upon the particular application. For EMC purposes, we often do not care whether a PCB-to-chassis bond provides a low impedance at frequencies below 10kHz, or even at DC, as long as it has a low impedance over the frequency range of concern for EMC.

The lowest impedance bonds at RF are achieved by pressing one metal surface against another. Pointed metal contacts tend to have higher impedance at RF than is achieved by pressing one area of metal against another, so EMC designers generally try to avoid using point contact bonds. It is usually recommended that each bonding location employs a PCB pad of at least 3mm diameter, not covered by solder resist, pressed against a metal spacer which in turn presses against the chassis. It is normal to ensure a good bond between these
pads on the outer layers of the PCB and an inner 0V plane by using a ring of via holes, as shown in Figure 3B.

Good surface conductivity is required for all the metal-to-metal contact areas, and they should not corrode over the life of the product – so it is best to plate each part with the same metal, such as tin. Fixings such as screws or bolts should not be relied upon as bonds, they should simply ensure that the contact areas of the bonding components are pressed together firmly. Captive metal spacers with threaded holes are often used, but the means by which the spacer is held captive in the chassis must achieve a cold-weld all around the spacer, add no impedance, and not corrode.

A variety of components are available to help achieve 0V plane-chassis bonding at low cost, such as the conductive snap-in PCB spacers shown in Figure 3P. Some other components and bonding techniques are mentioned later.
The minimum requirements are usually for RF bonds between the 0V plane and the chassis or frame near every input or output connector, and at least one RF bond close to the highest-speed or 'noisiest' (most emissive) devices.

Where a shielded cable is connected to a PCB, its shield should usually be RF bonded (sometimes called 360° bonded) to the chassis or frame of the unit at the place where it enters (see Parts 2 and 4 of [2]), which requires a shielded connector (or a shielded shell on a connector). To ease assembly and reduce assembly time we prefer to use PCB-mounted connectors that locate with cutouts in connector panels.

360° bonding can easily be achieved for PCB-mounted connectors by sandwiching a conductive gasket between their metal bodies or shells and their connector panel. If their metal bodies or shells are also soldered at multiple points to the 0V plane (usually at the lugs that provide their mechanical support) — then 0V plane-chassis bonding is easily achieved too. This technique can sometimes be used without any mechanical fixings between the connector panel and the connectors, further reducing assembly time whilst helping to achieve good EMC performance. An example of such an assembly is shown in Figure 3Q.
Even if the cable is not a shielded type, it is a good idea to use shielded PCB-mounted connectors as described here, to improve 0V plane — chassis bonding near the input and output connectors. Soft conductive gasket material is usually used, die-cut to suit the arrangement of the connectors (as in Figure 3Q). The typical gasket material consists of a plastic foam core covered with metallised fabric, but types are now becoming available that use a conductive foam to give improved bonding (so-called "Z-axis conductive").

Spring finger gaskets are available for individual D-types, and custom spring-finger gaskets can also be created. Examples of custom-designed spring finger gaskets can be found at the expansion card slots of most modern PCs. Unfortunately, some types of PCs do not use a stiff enough connector panel in the expansion card area, and the combined pressure on all the spring fingers causes the panel to bow outwards in the middle, opening up large gaps and reducing the performance of the PC case’s shielding whilst also degrading the 0V-chassis bonding for the expansion cards.
Because for EMC we often don’t care whether a low bond impedance is achieved all the way down to DC, we sometimes choose to make our bonds through capacitors. When galvanic isolation is required between a PCB and its chassis, capacitive bonding is the only solution (using suitably rated, and maybe safety-approved capacitors). Galvanically isolated medical circuits may have to meet very stringent leakage current specifications, and this could place an upper limit on the total value of capacitance that may be used between a PCB and its local chassis. In this case some of the techniques described later might not be able to be used.

An important consideration with the use of bonding capacitors is that, in conjunction with the inductive impedance that inevitably appears in series with them (e.g. due to traces and via holes), they self-resonate and only provide low impedances over a limited range of frequencies, as Figure 3C shows.

![Figure 3C](image)

Above its self-resonant frequency (SRF), the impedance of a capacitor increases with frequency. In fact, this slope is the overall inductive impedance of the capacitor and its pads, traces and via hole(s). All capacitors inevitable have some internal inductance, typically between 1 and 2 nanoHenries (nH) for small multi-layer ceramics rated up to 100V. The pads, traces and via holes that connect the capacitors to the PCB accumulate inductance at the rate
of about 1nH per millimetre of their length (as do leads, if using leaded capacitors instead of surface mounted). At 1GHz each additional nH of inductance (L) adds 6.3Ω additional inductive impedance to a PCB-chassis bond ($X_L = 2\pi f L$).

1.3 Hybrid bonding

This technique uses a variety of types of bonds between the PCB’s 0V plane and the chassis…

- direct (as shown in Figure 3B);
- via a capacitor (see Figure 3C);
- via a resistor, for damping structural resonances (see later).

Each application is different, and there are sometimes good technical reasons for using hybrid bonding despite the fact that capacitive bonds are generally less than ideal for broadband RF bonding (see Figure 3B). It is often difficult to know in advance of EMC testing what type of bond will give the best overall EMC performance, for each location, so prototype PCBs can benefit from the use of a multi-purpose bonding pad pattern, like that shown in Figure 3D.
Experimental EMC tests (e.g. so-called ‘pre-compliance’ tests) are recommended to discover which is the best configuration of DC, capacitive, and resistive (see later) bonds, and which are the best values to use.

1.4 ‘Ground loops’ and tradition

A tradition has grown up amongst designers of DC and low-frequency (LF) instrumentation and amplification (e.g. audio) of avoiding ‘ground loops’ by only having a single bond between the 0V reference for their circuit and the chassis (which is itself often connected to the protective earthing safety conductor in the AC power lead). But at the same time, designers of RF amplifiers and the like established a tradition of multi-point bonding between their 0V planes and their chassis, with the spacing between the bonds being very small compared with the wavelength at their highest frequency of concern.

The DC/LF camp have in the past employed what they called single-point grounding (or ‘star’ grounding) almost as if it was an article of faith, and seemingly never stopped to ask why their RF counterparts could design perfectly good DC/LF circuits using multipoint bonding which creates numerous ground loops.

These days, many DC/LF circuit designers are learning that to achieve good RF immunity and pass their EMC Directive compliance tests they need to employ multipoint bonding after all. Some of them are learning that giving their PCBs a good ‘solid’ unbroken 0V plane and using that for all the ‘grounding’, and bonding that 0V plane to their chassis at multiple locations, generally is a big help in meeting immunity standards and also improves their circuit’s functional performance.

In some professional audio equipment, changing from traditional single-point grounding to unbroken 0V planes with multiple PCB-chassis bonds has reduced audio-band noise levels by 10dB below what had for decades been considered the minimum physically achievable (see
A similar multi-point bonding approach can work very well in large audio installations too, see [6] - [11]. But we still find DC/LF circuit designers using ‘hybrid’ bonding to try to preserve their ancient tradition of single-point chassis bonding whilst achieving multi-point bonding via capacitors for EMC. Unfortunately, the result can be a less than optimal design for signal-to-noise, cost and/or EMC. For cost-effective engineering, traditional design techniques should never be accepted without question.

2. Why bond PCB 0V planes to chassis anyway?

2.1 Reduced transfer impedance

As signal return currents flow through the inevitable impedances in a PCB’s 0V structure, they cause different parts of the PCB to experience different voltages from each other. These voltages are common-mode (CM), and CM voltages and currents are the major cause of EMC problems. One of the many EMC and signal integrity benefits of an unbroken 0V plane in a PCB is that it has lower impedance at RF, so CM voltage differences at RF are reduced and emissions of electric fields are reduced. An impedance that converts a wanted current (e.g. signal return) into unwanted CM voltage (or a wanted voltage into an unwanted CM current) is called a ‘transfer impedance’ – an important concept in EMC engineering.

0V planes are especially valuable where off-board conductors (e.g. cables) are attached to different parts of the PCB. The length of these conductors often makes them very efficient ‘accidental antennas’ and reducing the CM voltage difference between the different parts of the PCB they are attached to is an excellent way to reduce their emissions.

When RF CM currents are injected into a PCB by coupling from the external electromagnetic environment (with off-board conductors being major sources of injection) – having a lower
transfer impedance in the PCB’s 0V structure means that the resulting signal voltage noise is lower and much less likely to interfere with circuit operation.

The transfer impedance of a well-designed 0V plane (see the next part of this series) is several orders of magnitude less than the transfer impedance of a PCB trace or a wire. To take advantage of the low transfer impedance of the plane, all traces, wires or cables that exit a plane’s area must be RF bonded to the plane, either by ‘360° bonding’ of their shields or by filters with a capacitor connected to the 0V plane.

Bonding the 0V plane to the chassis at multiple points helps reduce the transfer impedance even more than can be achieved with a plane alone, and so helps improve EMC performance. Metal chassis have much lower resistance than can be achieved in a layer of copper in a PCB, so they also help reduce the transfer impedance at much lower frequencies than the plane can achieve on its own, even down to DC.

Because of the above considerations, it is normal EMC practice to bond 0V planes to chassis at least at each of the corners of the PCB’s 0V plane and also near to the entry/exit point of each off-board conductor. Figure 3E shows one of the benefits of reducing a PCB’s transfer impedance by bonding its 0V plane to its chassis.
2.2 Better control of ‘fringing fields’

The operation of the circuit on the PCB causes RF voltages that differ from the voltages on nearby conductive items, such as the chassis, and these RF voltage differences give rise to emissions, as shown by Figure 3F. Where the 0V system is a plane, all the emissions are from its edges, sometimes called fringing fields.

There are a number of sources of RF voltage on a PCB. Signal return currents flowing in the 0V system are one source of RF voltages (see above and Figure 3E). RF currents flowing in the impedances of the circuit’s external power supply (e.g. the AC supply) are yet another source of RF voltages. The signals in the circuit may have some RF content in their spectrum (digital signals always do). The RF voltages on transistors and ICs themselves (especially those fitted with heatsinks) are becoming more significant as operating frequencies increase. So another reason for bonding a PCB’s 0V plane to the chassis is to try to equalise the RF voltages between them, to reduce the emissions from their fringing fields. A reciprocal argument can be made to show that improving the RF bonding between PCB and its nearby chassis helps improve immunity.
Reducing the effects of CM emissions is the reason why PCBs often have at least one bond between their 0V planes and local chassis, located close to the source of the PCB’s highest-frequency noise emissions. This is often a clock oscillator or clock buffer, or a VLSI integrated circuit (IC) such as a powerful microprocessor, gate array, or digital signal processor.

Basic PCB-chassis bonding guidelines thus require PCB-chassis bonds at least at each corner of the 0V plane, at least one near to each cable port, and at least one near to each high-speed device.

Now that we understand the basics of PCB-chassis bonding, we can move to discussing the design issues that are arising due to the continual increase in the highest frequency of concern, due to the technology issues discussed in Part 1 of this series [12].

3. The ‘highest frequency of concern’

Throughout this series of articles, an important issue is the ‘highest frequency of concern’ because this governs a great many of EMC design issues. The choice of the highest frequency is up to the head of the equipment’s design team, who might choose it on the basis of...

- the minimum regulatory requirements it is hoped to ‘get away with’ in the countries being marketed to;
- what could cause annoyance to customers and/or poor quality performance or unreliability in real life;
- the highest frequency the technology is capable of emitting or being susceptible to;
- future developments in regulations, test standards, the electromagnetic environment or the devices used (e.g. die shrinks) to avoid having to redesign the equipment too soon.

It is worth pointing out here that although the EMC Directive’s notified emissions standards may be limited in the upper frequency they test to, compliance with the EMC Directive’s essential Protection Requirements mean that emissions that could cause a nuisance to others are not permitted at any frequency up to 400GHz.
It is a similar issue for immunity. Even though the most relevant notified immunity standard is limited in its range of disturbances and their levels and frequencies, compliance with the EMC Protection Requirements requires that the equipment be sufficiently immune to its real electromagnetic environment up to 400GHz. (The 400GHz limit of the EMC Directive comes about because signals above that frequency are considered to be infra-red, then visible light, ultra-violet, X-rays, etc. as the frequency increases still further. Although these are all electromagnetic phenomena, they are not covered by the EMC Directive.)

So, simply testing to the current versions of the most relevant EN or IEC EMC emissions and immunity standards is not enough to ensure EMC Directive compliance, and not enough to ensure happy customers either. Where the electronic technology used could cause emissions above the highest frequency covered by the standard it is recommended that quick tests (at least) be done to see if the emissions are excessive and need suppressing to prevent interference.

In the case of immunity, the issue is whether there could be significant sources of ambient noise present in the equipment’s operational environment, at frequencies higher than those covered by the most relevant immunity standard. If there are, it is recommended that quick tests (at least) be done to see if the susceptibility to these frequencies is significant, and whether the equipment needs modifying to prevent it from being interfered with in real-life operation.

**4. Benefits of closer spacing between a PCB and its chassis**

Ideally, we would like zero coupling between our digital, analogue and switch-mode circuits and their external electromagnetic environment, because then we would have no emissions and perfect immunity. We can never achieve zero coupling, but a great many EMC design techniques are associated with reducing it.
The fact that circuit operation causes voltage differences between PCB and chassis, causing fringing fields, was mentioned earlier. Some EMC engineers analyse the structure consisting of the PCB’s 0V plane and its nearby chassis using transmission-line methods. They find that the closer they are together; the lower is their coupling to the external electromagnetic environment [13]. Figure 3G shows this graphically.

![Figure 3G](image)

Where the PCB-chassis spacing is greater than half a wavelength, reducing the spacing could possibly make the coupling between the transmission-line structure and the external environment more efficient, increasing emissions and worsening immunity. One solution to this problem is to ensure that the spacing is reduced to much less than half a wavelength. The closer the PCB is to its chassis, the lower is the impedance of the bonds between them. Inductance scales linearly with length, so halving the PCB’s spacing from the chassis will half the length (and hence halve the partial inductance) of the bonds. Reduced inductance in PCB-chassis bonds has benefits for the overall transfer impedance, and helps return CM currents more quickly to the PCB, improving emissions and immunity in two ways. Finally, closer spacing will increase the resonant frequencies of the cavities between the PCB and the chassis (see later) – not by much, but it all helps.
5. Controlling resonances in the PCB-chassis cavity

5.1 Why and how the cavity resonates

As the ‘highest frequency of concern’ keeps getting higher (see above, and [12]) many of the physical structures in electronic equipment become resonant, creating new problems for both signal integrity and EMC. The resonance problem is caused when the wavelengths ($\lambda$) of the frequencies become comparable with the physical dimensions of the structure. This is why EMC design engineers are often as concerned with millimetres as they are with MHz.

The black curve in Figure 3L below is a measurement of an example PCB-chassis structure. At resonance, a structure couples very well indeed with its external electromagnetic environment, becoming a very efficient ‘accidental antenna’. This is not what we want because it increases emissions and worsens immunity. At resonance, emissions from physical structures can be 20dB (or more) higher than at nearby non-resonant frequencies (and by a reciprocal argument, their immunity can be 20dB or more worse).

Also, at resonance, coupling between circuits on the PCB and elsewhere in the equipment is increased. This is often called crosstalk, and can cause problems for signal-to-noise and signal integrity.

Part 2 of this series [14] discussed the structural resonances of PCB-mounted shielding cans, and its Figures 2H and 2J shows the effects of their structural (cavity) resonances on crosstalk and emissions respectively. Exactly the same issues arise due to the structural resonances of the cavities formed between the PCB and its chassis [15] [16], the topic covered by this part of the series.

If there were only PCB-chassis bonds at the four corners of a rectangular PCB, then there would be just the one cavity to analyse, but often there are more bonds and so more (and smaller) cavities. In most cases, what we are mostly concerned with is the first (lowest)
resonant frequency the PCB-chassis bonded structure, which is associated with the longest diagonal of its cavities.

A crude analysis of the likely resonant frequency for a structure that has PCB-chassis bonds only at its corners, and where PCB-chassis spacing is small (as is usually the situation) is easy enough, uses the formula…

\[ f_{\text{lowest}} = 150 \sqrt{(L^2 + W^2) - 1} \] (in GHz, when L and W are in mm)

…where L and W are the PCB 0V plane’s length and width respectively. For example, a structure consisting of a PCB 0V plane 160 x 120mm spaced 5mm above a chassis, and bonded to it at its four corners, would have its lowest resonant frequency at around 0.75GHz.

The above formula is only a crude approximation because it is based on the resonances inside a totally metal-sided cavity, whereas our structure is simply two metal plates with open edges connected together at a few locations with non-zero impedances. Such a structure requires a three-dimensional field solver to simulate what is really going on at any frequency of interest.

Where a cavity has PCB-chassis bonds on only one side (e.g. at only two corners), or on two adjacent sides (e.g. at only three corners), a crude approximation for its lowest resonant frequency is…

\[ f_{\text{lowest}} = 75 \sqrt{(L^2 + W^2) - 1} \] (in GHz, when L and W are in mm)

5.2 Wavelength rules

To help avoid structural resonances, EMC engineers often employ general guidelines (‘rules of thumb’) for physical dimensions based on \( \lambda/10 \). The dimensions concerned could be spacings between RF bonds, or a number of other issues, but the idea is that as long as they are less than \( \lambda/10 \) resonance cannot occur. \( \lambda/20 \) or \( \lambda/100 \) ‘rules’ are sometimes used instead, for better EMC performance.
Some designers know the rise and fall times of their signals, but not their associated highest frequency of concern. In this case the dimension given by the $\lambda/10$ guide is equivalent to 100mm times the real risetime in ns (or the real falltime, if it is shorter). It is very important to use the real rise/falltimes achieved at the output pins of the ICs, not their datasheet figures, since die-shrinks usually result in ICs that have actual rise and fall times that are much faster than the maximum values in their datasheets [12]. If you do not know the real rise and falltimes for saturating logic like CMOS and TTL, divide their datasheet figures by 10 to be on the safe side. For non-saturating logic (such as ECL), divide the datasheet values by 4. But it is much better to measure them than to use these estimates.

When measuring rise and fall times: use an oscilloscope and probes that have much faster rise and fall times than the measured signals (ideally more than twice as fast); and use correct high-frequency probing techniques as described in the oscilloscope manufacturer’s application notes. Always measure at the actual pins of the IC or transistor that is the source of the signal.

5.3 Increasing the number of bonds to increase resonant frequencies

To help prevent resonances from occurring in the PCB-chassis structure the general guidance is to use PCB-chassis bonds that are no further than $\lambda/10$ from any other bond (preferably closer), where the $\lambda$ used corresponds to the highest frequency of concern. In air $\lambda = c/f$, where $c = \text{the speed of light (3.10^8 m/s)}$, and when $f$ is in Hz, $\lambda$ is in metres.

Mark Montrose [17] recommends using bonds that are no more than $\lambda/20$ apart from each other, at the highest frequency of concern, as shown in Figure 3H. He uses an argument based on the efficiency of dipole antennas, rather than cavity resonances. $\lambda/20$ will give better performance than $\lambda/10$, but will quadruple the number of bonds for a given $\lambda$. 
Once a PCB has sufficient fixings to control its movement during shock and vibration, adding extra PCB-chassis bonds that required fixings would add to assembly time. However, a number of techniques exist that allow PCB-chassis bonds to be added without increasing assembly times. One of them is shown in Figure 3J, a (slightly out of focus) photograph of a PCB-chassis bonding location between a PC motherboard and its chassis (basepan).
This technique uses a sheet metal chassis that is ‘semi-punched’ to create a number of vertical protrusions (‘lugs’) that align with slots cut out of the PCB. The PCB is pushed down over the lugs and metal spring finger clips make contact with the lugs as they protrude through the slots. The example shown in Figure 3J is especially notable because the lugs were shaped so that once pressed down, the PCB was then slid sideways into a feature in the lugs to lock it into position at each lug. Only a single screw-fixing was required to prevent the PCB from sliding sideways and becoming disengaged from the lugs, so assembling this motherboard to its basepan was a very quick and easy operation. It is very rewarding when good EMC design techniques can also be combined with savings in the overall cost of manufacture, as they often can when the natural urge to spend the least cost on the PCB is resisted (see [12]).

Another technique is to provide PCB pads on the bottom of the PCB so that spring fingers or conductive ‘bumps’ can make contact between the pad and the chassis, as shown in Figure 3K. A wide variety of alternatives are available for use as conductive bumps, usually small pieces of compressible conductive gasket.
The spring fingers or conductive gaskets could either be fitted to the PCB, or to the chassis. Spring fingers are available as surface-mounted components that can be soldered to the PCB pads. Many types of spring finger and conductive gasket are also available with self-adhesive backing, making their assembly to the chassis or PCB relatively easy. Some shielding and other manufacturers make components designed especially for bonding PCB 0V planes to chassis, but anything based on a coiled metal spring should be avoided unless the highest frequency of concern is not very high (say, below 50MHz, depending on the application). For example, Kitagawa makes some very small surface-mounted spring finger components, initially for use in cellphones.

In high volume serial manufacture, and where PCB-chassis spacings are 2.5mm or less, it may be worthwhile considering the robotic application of blobs of form-in-place (FIP) conductive gasket. Types of FIP gasket material are now available that foam up after application, to create larger and/or softer gasket bumps.

One of the problems with PCB-chassis bonds is that PCBs are often changed late in a design and development project – when problems are found during functional or compliance testing – and this can mean that the locations of some of the bonds need to be changed too. Where the PCB bonds rely on the chassis metalwork (e.g. captive metal spacers, semi-punched lugs, etc.) the changes in the PCB layout have a knock-on effect that adds to costs and timescales. But bonds that use spring fingers or conductive bumps applied to the PCB don’t cause the same problems.

Mark Montrose describes (in [17]) using conductive polymer parts for PCB-chassis bonding, retained between the PCB and the chassis by punched holes in a plastic sheet. When the PCB changes, the punching pattern for the plastic sheet is changed to suit.
Good PCB-chassis bonding performance relies on good (high) surface conductivity being achieved over the life of the equipment. This is especially important where spring finger or conductive bump techniques are used, because their contact pressures are much less than at a screwed fixing, so thin films of oxide or corrosion will have a much worse effect. Where metal parts are concerned, it is best to plate each part with the same highly-conductive metal, such as tin or gold. Conductive gasket materials are harder to choose to prevent corrosion, but any professional EMC gasket manufacturer should be able to provide highly detailed application guides and test results showing which gasket materials should be used with which metals.

5.4 What if we can't use enough bonds?

Ideally, we would reduce the spacing of the PCB-chassis bonds until the lowest resonance frequency was higher than the highest frequency of concern. Then – as long as the highest frequency of concern does not increase – we should have design for which the PCB-chassis bonding structure is not likely to be the cause of significant EMC problems despite design changes, alternative components, and manufacturing tolerances.

But to achieve a lowest resonant frequency of 3.0GHz (for example) – so that no resonant effects should cause problems below about 2.5GHz – following the λ/10 rule would require PCB-chassis bonds no further apart than 10mm (5mm if using the λ/20 rule).

Such very frequent bond spacing would increase PCB layout difficulties, and the total force required to compress all the spring fingers or conductive bumps might make the PCB and/or the chassis bend, unless extra fixings or stiffening components are used.

So to control PCB-chassis cavity resonances above about 500MHz, we may need to employ other techniques, described below.

5.5 Spreading the resonances more widely to reduce peak amplitude
It might prove impractical to add sufficient PCB-chassis bonds to make the lowest resonant frequency higher than the highest frequency of concern. In this situation there may be an advantage in avoiding too regular an arrangement of bond locations. An irregular bonding pattern has two advantages…

- The resonances in the length and width directions of different cavities are not the same
- The resonant frequencies of the multiple smaller cavities created by the multiple bonds do not coincide

Breaking up the resonances in this way should reduce the worst-case peak amplitudes of the resonances, trading them for broader resonant regions (lower Q values). If using this technique to reduce emissions or improve immunity at a particular frequency, be aware that it might worsen EMC performance at other frequencies.

This approach should be reasonably ‘robust’ as far as design changes and component variations are concerned, but EMC-competent QA and change control are always recommended (see later).

5.6 Designing resonances to miss problem frequencies

Each cavity resonance covers a range of frequencies (see the black line in Figure 3L below for a typical example), and generally only cause problems when the frequencies emitted by the PCB’s circuit fall within this range. Most circuits have their highest emissions at their clocks’ fundamentals and their harmonics, and careful design of the PCB-chassis bonds may be able to ensure that these do not fall into any resonant frequency ranges.
The use of high-frequency clocks can make this technique easier to apply, if their harmonic spacing is great enough that they ‘bracket’ the resonant regions rather than fall into any of them. It can also be an advantage to increase the Q of each resonance, by making all of the resonant cavities created by the multiple PCB-chassis bonds identical in shape and size wherever practical. This is the exact opposite effect to the previous technique. A higher Q means the frequency range over which emissions are increased is narrower, and easier to avoid with clock harmonics.

Simple experiments with plain copper sheets may not be sufficiently representative of real life, because the PCB’s devices, trace routings, perforations and gaps in the 0V plane – plus any apertures, shape changes and the proximity of cables and other components – will modify the resonant frequencies. But we do not want to wait until we can EMC test a structure that is reasonably representative of the final design – because by this time changes to the design will be much more costly than if they were done earlier (see [12], especially Figure 1A).

This clever technique can help reduce unit manufacturing costs, but investing in a three-dimensional field solver (and in the training in how to use it properly) is almost a necessity if is to be used cost-effectively. The author’s experience with such computer-aided
engineering tools, over many years, has been that they seem to take a very long time to learn how to use effectively, but then they suddenly allow design iterations that would have taken days or weeks to be done in minutes or hours. A dozen design iterations in a day is not unreasonable at an early stage in the project, and at that point the true value of the investment becomes apparent to all. Of course, the field solver will need to be provided with a reasonably accurate description of the final design, to give useful predictions that reduce project timescale risk. The garbage in garbage out rule always applies.

But this is not a design technique that is very ‘robust’ as far as design changes and component variations is concerned. Even quite small changes, such as altering the clock frequency to use the latest ICs, could completely alter the EMC performance of the equipment, so EMC-competent QA and change control is very important (see later).

5.7 Being clever with capacitors

The values of the capacitors used in capacitive or hybrid bonding might affect the EMC performance. Unlike the ‘designing resonances to miss problem frequencies’ technique above, this approach lends itself to last-minute modifications – as long as the PCB has already been laid out using appropriate pad patterns at the bonding locations (see Figures 3D, 3K and 3M). Usually, the equipment is subjected to pre-compliance EMC tests and the types and values of capacitors (or zero-Ω links, or resistors) fitted at each bond are varied until the optimum is found. An assembly bench equipped with appropriate soldering/desoldering tools and a complete set of all likely components needs to be provided just outside the test chamber. The number of possible alternatives is huge, so most people stop iterating when further improvement is proving too time-consuming.

If zero-Ω links provide the best EMC, on a future revision of the PCB they could be replaced by direct bonds between the chassis and the 0V plane (e.g. as shown in to Figure 3C). However,
a zero-Ω link plus its pads, traces and via hole will have a significant overall series inductance – replacing this with a direct bond might affect EMC, so retesting is recommended.

If it is found that carefully chosen values of capacitance are necessary, then – like the “designing resonances to miss problem frequencies” technique above – small changes in ICs, circuits or assembly parts or methods could dramatically worsen the EMC performance, so EMC-competent QA and change control is very important (see later).

5.8 Using resistors to ‘dampen’ cavity resonances

[15] and [16] describe using resistive PCB-chassis bonds to ‘dampen’ cavity resonances and reduce the amplitude of the resonant peaks. In practice, this technique is like the hybrid bonding technique described earlier, using resistors instead of capacitors (or resistors in series with capacitors) with appropriate pad patterns (see Figures 3D and 3K, and 3M below). The higher the inductive impedance of a PCB-chassis bond, the lower the benefits for EMC. But the higher the resistive impedance of a bond, the lower the amplitude of the PCB-chassis cavity resonances. At the resonant frequencies of a PCB-chassis cavity, much higher currents flow through the bonding points. Resistance is lossy, converting current into heat, so any resistance in the bonds will cause greater losses at the resonant frequencies – reducing the peak amplitude of the resonances (reducing the cavity’s “Q”).

Increasing PCB-chassis bonding impedances with resistors has the downside of decreasing EMC performance at non-resonant frequencies. So, when using this technique to reduce emissions or improve immunity at a cavity resonance frequency, be aware that it might make a marginal performance at other frequencies non-compliant.

[15] and [16] found that resistors between 47 and 100Ω worked best, but maybe this was related to the 50Ω source impedance used for the experiments. Experimental EMC tests (e.g. pre-compliance tests) are always recommended to discover which is the best configuration of
DC, capacitive, and resistive bonds, and which are the best values of capacitors and resistors to use.

A well-damped PCB-chassis structure is not likely to be the cause of significant EMC problems despite design changes, alternative components, and manufacturing tolerances, but EMC-competent QA and change control is always recommended.

5.9 Using absorber to ‘dampen’ cavity resonances

Carbon and/or ferrite-loaded materials (usually elastomers) are available that absorb RF energy. These are similar to the material used to line EMC test chambers to dampen their cavity resonances, and they can also be used inside shielded boxes to dampen their resonances (see [14]).

When they are placed in a cavity they convert electromagnetic energy into heat, and (like the resistive bonds described above) they reduce the resonant peakiness (the cavity’s “Q”) thereby reducing emissions at the resonant frequencies (and, by a reciprocal argument, increasing immunity).

A number of manufacturers now offer suitable ferrite-loaded materials, usually based on flexible sheets with self-adhesive backing. The thicker sheets usually achieve greater damping at lower frequencies. Ferrite-loaded sheets should work best when located near to the PCB-chassis bonds, where the magnetic fields at resonance should be the highest.

Carbon-loaded materials (usually blocks of foamed plastic) should provide their best damping when located in-between the bonds, where the electric fields are the highest at resonance. However, experimental EMC tests (e.g. pre-compliance tests) are always recommended to discover which is the best and lowest-cost material to use, where best to locate it and how best to support it.
There seems to be no reason why ordinary ferrite material, such as has been used for many years to suppress CM currents on cables, could not be used instead, apart from the difficulty of mounting such hard, brittle and dense materials. Maybe standard ferrite cylinders or toroids could simply be slipped over the metal spacers used for bonding (perhaps with a blob of silicone glue to help prevent vibration and wear)?

Ferrite cylinders and toroids have for many years been available at low cost in a very wide variety of dimensions, in a material that gave a wide choice of resistive impedances all with their peak lossiness around 300MHz. Recently new materials have been developed that achieve their peak lossinesses around 700MHz or 2.45GHz. As far as the author knows, solid ferrite has never been used in this way as a means of damping a PCB-chassis resonance, but it seems an idea worth trying.

As for resistive damping above, absorber damping should continue to be effective despite design changes, alternative components, and manufacturing tolerances, but EMC-competent QA and change control is always recommended.

5.10 Reducing the impedance of capacitive bonds

The extra inductance associated with using capacitive bonds (see above, and Figure 3D and 3K) can be reduced by using multiple capacitors arranged radially around each bonding location, as shown by Figure 3M.
The inductances associated with each capacitor and its pads, traces and via holes all appear in parallel. Using a radial arrangement, such as that as shown in Figure 3M, ensures that the mutual inductance between them cancels out, so that their overall inductance is simply the value of one capacitive bond divided by the number of capacitors. Arranging the capacitors in a parallel array would not cancel out their mutual inductances and the overall inductance achieved would not be as low as with the radial arrangement shown.

Three capacitors were chosen for the sketch in Figure 3M, but just two capacitors, or four or more, could (of course) be used instead.

5.11 Using shielding techniques

We could surround our PCB with spring fingers or conductive gasket that makes a continuous perimeter bond between the edges of the 0V plane and the chassis. This would make the PCB-chassis cavity into a fully shielded enclosure, reducing its emissions considerably (and improving the immunity of the PCB’s circuit).

Just like the PCB shielding cans shown in Figures 2H and 2J in [14], such shielding could increase crosstalk between different circuits on the PCB, and at its resonant frequencies its
emissions might not be reduced by as much as might be expected. The same remedies for this problem as were described in [14] also apply to the PCB-chassis cavity…

- Break the cavity up into many smaller cavities each with a its lowest resonant frequency higher than the highest frequency of concern
- Add absorber to the cavity to dampen its resonant peaks

Breaking the cavity up into many smaller cavities could in some applications simply mean using a mesh-shaped conductive gasket, making contact with exposed traces on the bottom of the PCB. These bonding traces replace the bonding pads described earlier in this article, and should be via’d to the internal unbroken 0V plane using the PCB shielding rules given in [14].

5.12 Using fully shielded PCB assemblies

If fully shielded PCB assemblies as described in [14] are used, the need for PCB-chassis bonding to improve EMC is reduced, although bonding to a solid metal or sheet metal chassis might still provide a useful reduction in transfer impedance (see above), especially at lower frequencies.

6. Daughter and mezzanine boards

Everything that has been written above also applies to mezzanine and daughter boards. For such boards, the 0V plane in their motherboard can provide some of the benefits of a local chassis. The cavity created between them can resonate, creating problems for emissions and immunity, especially where the mezzanine/daughter board is connected to external cables (as numerous designers have discovered at great cost to their projects). For these reasons, all of the PCB-chassis bonding benefits and techniques discussed so far also apply to a mezzanine/daughter board-motherboard structure.
In some circumstances it can be sufficient to bond the mezzanine/daughter board frequently enough to the motherboard. The inter-board connectors can help with the bonding, by using numerous 0V pins to bond the two boards’ 0V planes all along the length of the connector. A chassis can also be used to improve the EMC of a mezzanine/daughter board, using all of the techniques described above. It will generally be best if the bonds between the mezzanine/daughter board and its motherboard are carried straight through the motherboard to bond to the chassis.

7. EMC-competent QA, change control, cost-reduction

Most types of equipment these days rely on advanced silicon ICs, although they are often such commodity items that we don’t tend to notice the amazingly sophisticated technologies they routinely employ. High-tech silicon has many EMC problems; and EMC regulations are widespread world-wide; and as a result EMC-competent QA and change control is now a standard requirement in almost all electronics companies.

EMC-competent QA would ensure that serial manufacture always resulted in goods with similar enough EMC performance. This requires that all the EMC-critical aspects of the design are identified and controlled in manufacture, for instance by using appropriate Work
Instructions. Good EMC QA also employs custom EMC tests when goods are delivered, plus custom EMC tests at various stages during assembly, and at final test.

Custom EMC tests can be surprisingly low-cost to set-up and easy to apply, but they are often application-specific. Good EMC QA will also randomly select a product from time-to-time and subject it to full compliance tests, with records kept and trends analysed to prevent a bad batch of products from being made, or worse still – shipped.

EMC-competent change control is vital. EMC-competent people and EMC test facilities (ideally in-house, to save cost) are used to assess every request for a change or a concession, no matter how trivial they might seem, for their possible EMC implications. Of course, change control cannot be done if it is not known what EMC design techniques an equipment relies upon, so it relies on designers documenting important EMC issues in such a way that future engineers who need to know what consequences a change might have, are fully informed.

Products in serial manufacture are often subjected to cost-reduction exercises to reduce manufacturing costs and improve profitability. The author knows of several instances where such cost-reduction exercises resulted in such severe problems with interference in operation that the overall cost to the company was increased dramatically, rather than reduced. So the EMC-competent change control described above must also be applied to any cost-reduction exercises, no matter how trivial the issues seem to be.

For instance, the production manager in one company decided to employ self-tapping screws that were pre-lubricated with a blob of wax, to save time and tool-wear in assembly. But the wax increased the resistance at all the metal bonds that they were relying on to create a reasonable RF Reference Plane to help achieve EMC compliance (although they did not realise this at the time). Numerous similar very costly real-life examples could be described to
emphasise how very important it is to fully understand the EMC design of an equipment, and
to employ EMC-competent control on every change to it.

8. Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design
techniques – but in real-life there are a great many design trade-offs (compromises) to be
made, and this is where the circuit and PCB designers really earn their keep.
Designers are often put under cost or time pressure by managers who don’t understand the
technical trade-offs, and so don’t understand that their actions could have the opposite effect
to that which they intend and actually increase project costs and delays, as well as maybe
increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of
this series [12], plus the final section of part 2 [14].

9. References

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[5] “EMC and Electrical Safety Design Manuals”, a set of four volumes edited by Keith
Volume 4 – Safety of Electrical Equipment ISBN 1-902009-08-8


A similar paper with the same title was presented at the IEE’s Seminar: “EMC – its (nearly) all about the cabling”, Wednesday 22 January 2003, sales@iee.org.uk.


I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than this series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose
Compliance Services, http://www.montrosecollection.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

Some useful textbooks and other references are:


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Advanced PCB design and layout for EMC
Part 4 - Reference planes for 0V and power

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the fourth in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to...

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest integrated circuit (IC) technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues
A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not spend much time analysing why these techniques work, they will focus on describing their practical application and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1 Introduction to Reference Planes

A well-designed 0V reference plane, sometimes called an ‘earth’ or ‘ground’ plane (although it has nothing to do with the safety earth or ground), is increasingly essential as the shrinking feature sizes of ICs decreases the rise and fall times of their logic transitions, as discussed in Part 1 of this series [6]. A well-designed power reference plane might also be required, for the same reason.

The data sheets for digital devices only provide maximum rise and fall times (if they even include that information) – this allows the IC manufacturers to move their devices to smaller fabrication processes. The resulting ‘mask-shrinks’ or ‘die-shrinks’ save them a great deal of money, but can create potentially huge EMC problems for their customers. Some
manufacturers have had to spend millions of dollars redesigning existing products to maintain EMC compliance, after their microprocessor manufacturer implemented a die shrink. Devices such as 74HC ‘glue logic’ series that has been around for nearly 20 years originally used to only emit significantly at up to 200MHz – now the same part numbers from the same manufacturers are found to cause emissions problems up to 900MHz. This makes it important for manufacturers to retest old products that are still in production every few years, to check their EMC compliance. There is no sign of any end to this trend to ever-faster edge rates and ever-higher frequencies, for at least the next 10 to 15 years.

Ideally, a reference plane is a solid copper sheet in (or on) a PCB. It is definitely not a ‘copper fill’ or ‘ground mesh’ (see later).

Unfortunately, copper planes without numerous perforations are impossible in practice without using ‘HDI’ PCB fabrication technology (often called ‘micro-via’, see section 5). This article will discuss how to get the best EMC performance out of PCB reference planes despite the restrictions of typical modern PCB fabrication technologies, such as through-hole-plate (THP) – in which holes are drilled right through a PCB, then plated with metal so as to provide electrical connections between the top, bottom and any internal copper layers.

0V reference planes are the single most cost-effective EMC measure that can be applied at PCB assembly level (or higher). It is hard to understate how important the use of 0V reference planes in PCBs is for EMC. When advanced PCB EMC techniques are required – a well-designed 0V reference plane is absolutely essential.

Planes provide a number of very valuable EMC and Signal Integrity (SI) functions…

- They provide very low impedance, which means they can provide devices and circuits with stable reference voltages at radio frequency (RF).

We normally estimate the impedance of wires or PCB traces to be 1nH for each millimetre of their length, meaning that 10mm of wire or trace has approximately $63\times937$; of inductive impedance at 1GHz. So when
we need to provide a variety of devices with high-frequency currents from a reference voltage (as we increasingly do) we need to use a plane to distribute the reference voltage.

- Their low impedance return path is essential if capacitive filters mounted on the PCB are to achieve good performance above a few MHz. See Part 2 of this series [7] for PCB design for filters.
- They encourage returning RF currents to flow in the path that provides the least emissions and the lowest susceptibility.

When the return RF current path for a signal or power circuit flows in a plane conductor, it can follow whatever path it prefers – and it prefers the path with the least overall impedance. This is the path that achieves the least inductance in the overall current loop (‘loop inductance’), and also the path with highest capacitance to the send path. This concentrates the electric and magnetic fields associated with the differential-mode circuit into smaller volumes; reducing their coupling to other structures and to the electromagnetic environment, thereby reducing their common-mode emissions and improving the circuit’s susceptibility.

- They behave as image planes, so will provide a degree of shielding effectiveness for components and traces that are not close to an edge or a split.

Image planes provide shielding even when they are not connected to the circuit concerned. For example: a trace spaced 1mm above the centre of a large plane, the image plane effect results in at least 30dB of shielding effectiveness at frequencies above 100kHz. Closer spacing of components or traces to the plane gives more shielding effectiveness, so low-profile components are better for EMC.

- They reduce common-mode emissions from the cables attached to the PCB’s circuitry, at the frequencies at which they are ‘RF bonded’ to the plane. This issue was also mentioned in section 2.1 of Part 3 of this series [8].

RF bonding to a plane either means a direct connection, or a capacitive filter, between the conductor and the plane, at the point where the conductor leaves the area covered by the plane. In the case of conductors carrying signals, the value of the capacitor should be low enough not to compromise the signal.

Simply connecting capacitors from an external conductor to a PCB’s reference plane can encourage external noise currents to flow through the plane, and can increase the RF currents from output drivers. These increased RF noise currents flowing in the plane will cause increased noise voltages wherever the plane is imperfect (as they often are, for example where there are clearances around through-hole vias). So these ‘RF bonding’ capacitors will often need to be used with series resistors or soft ferrites on one or both sides to optimise the
PCB’s EMC. Refer to Part 2 of this series [7] for the EMC design issues associated with the filtering of signals and power conductors as they enter or exit a PCB.

It is not the purpose of this article to describe the theory of PCB reference planes, but [9], [10] and [11] are very useful references for the issues bulleted above, and cover the relevant mathematics.

2 Design issues for reference planes

2.1 Plane dimensions

As was mentioned above, a reference plane is ideally a solid copper sheet in (or on) a PCB. It is definitely not a ‘copper fill’ or ‘ground mesh’ (see later for using fills and meshes).

Planes must lie under all of their associated components and their traces and the 0V reference plane should extend beyond them on all sides of the PCB by as far as possible. It may even be worthwhile making a PCB larger simply to extend its 0V plane even further beyond the PCB’s devices and traces.

One reason for this is that signal or power return RF currents flowing in the plane layer (or planes) adjacent to the trace follow the path of the trace, but although the highest current density is underneath the trace the RF current also spreads out in the plane to either side of the trace’s route, as shown by Figure 4A.
About 95% of the return current is generally assumed to travel in a strip of plane as wide as 3 times the trace-plane spacing \((H)\) or three times as wide as the trace width \((W)\) – whichever is the smaller – centred along the trace’s route. It is considered to be an important basic PCB layout technique not to have any holes, splits or edges in this region of the plane. (Note that the analysis in Figure 4A assumes that \(H\) is smaller than \(W\).)

For higher EMC performance, the region of unbroken plane should extend even further away from the route taken by the trace, along both sides of its route. For very high frequency analogue signals or high-rate data with edges of less than 2ns (in real life, not the data sheet specification), it is often recommended that the trace is routed no closer than 10mm from any plane edge or split.

Another reason for extending the 0V reference plane even further is that its RF impedance falls as the plane’s size increases (an infinite plane has zero impedance at d.c.) and most/all of the plane benefits in the bulleted list in section 1 above are improved as a result.

But, like all metal conductors and structures, planes have natural resonant frequencies that depend on their shapes, sizes and environments. So in practice it may be necessary to limit the size of a plane to optimise its overall EMC benefits. Plane resonances are discussed later.
Part 2 of this series [7] described ‘segregation’ techniques in PCB layout. It is important to note that even though segregated circuits will almost always share the same 0V reference plane, the segregation ‘rules’ in [7] still apply in full. (These days it is not generally recommended that 0V planes are split, and this is discussed later.)

Power planes are designed much like 0V planes, but their use is intimately tied up with the power supply decoupling strategy. Decoupling is the subject of Part 5 of this series, and will not be discussed here. It is common for there to be several areas of power plane on a PCB e.g. 5V, 3.3V, 2.8V, +12V, -12V, and when the PCB’s circuits have been carefully segregated it is often possible to fit all of these on a single PCB layer.

2.2 Dealing with gaps and holes in planes

Any gap or hole in a PCB plane is a bad thing for EMC, because it is bound to increase impedance and inhibit the free movement of RF return currents. Where plane gaps or holes (or edges) are far enough away from traces (see 2.1 above) the general EMC guidance for all PCBs is that no gaps or holes should have longest dimensions greater than one-hundredth of the wavelength (λ) at the highest frequency of concern (i.e. the highest frequency to be controlled for EMC).

In air or vacuum, \( \lambda = \frac{300}{f} \) (λ in metres gives f in MHz). But if the gap or hole is filled with something other than air or vacuum, the dielectric constant, \( k \), (= relative permittivity) of the filling material will shorten the wavelength according to: \( \lambda = \frac{\lambda}{\sqrt{k}} \). For example, if the plane gap or hole is filled with PCB substrate (assumed to be FR4 unless stated otherwise), its \( k \) of 4.0 at frequencies above 1MHz means that its \( \lambda \) is half what it would be in air or vacuum: \( \lambda = \frac{150}{f} \) (λ in metres, f in MHz).

Modern PCBs have such high densities that through hole plate (THP) PCB manufacturing techniques cause massive perforation of any planes, due to the clearance holes (antipads)
required around each via. Such high levels of plane perforation cause a significant increase in plane impedance and reduce all of the benefits bulleted in section 1 above.

To improve EMC, antipads should be as small as possible – but without causing significantly decreased yield in their manufacture. However, some manufacturers use very low-cost PCB manufacturers whose accuracy in aligning PCB layers is very poor compared with what is typically achieved these days, and so require very large antipads to keep costs down. In such cases it will often be more cost-effective overall to use a better PCB manufacturer, and shrink the antipad diameters to 1mm.

There are specialist manufacturers who can provide much smaller antipads diameters than 1mm, at a price. But plane perforation by antipads can be *largely eliminated* by the use of HDI PCB fabrication technology (see section 5) that gives the best EMC performance from the planes.

Another important issue with dense THP PCB layouts is that the antipads should not merge into each other to create larger gaps or slots in a plane. This often happens when via holes are placed too close together; and/or when the computer-aided-drawing (CAD) system is set up to have too large a minimum radius when drawing planes; and/or when a PCB manufacturer overexposes the plane layer phototools. Figure 4B gives some examples of antipad merging errors.
Figure 4C shows an example of how not to create planes on a PCB. This PCB could have had acceptable EMC performance using microprocessors purchased in the 1980s, but not with those purchased this millennium (even if they had the same type numbers).

Via holes that are placed too close together can easily be detected by a review of the draft layout, and then corrected. CAD plane drawing rules are often set to a large minimum radius to shorten processing time to help speed design – which is acceptable as long as the final checking plots are created with a small minimum radius to prevent antipads from merging.
PCB fabricators who overexpose plane layer phototools to avoid having to take care over layer registration should never be used again, as their corporate quality culture is obviously deficient. Often, early deliveries of a PCB design use the antipads diameters that were designed, but when the product has settled down in regular production some suppliers will ‘grow’ their antipads to improve their yields. So it is always worthwhile carrying out simple checks on deliveries of bare PCBs, including a check on antipads diameters.

When a PCB has a large number of through-holes and via holes, care should be taken to prevent their antipads from merging together or encroaching on the current return paths of the traces (see Figure 4A). Figures 4D, 4E and 4F show how careful design can overcome these problems.

![Figure 4D Example of a poorly designed 0V plane](image)
Most PCB designers would be able to improve on the layout of Figure 4F, but at least it illustrates the point.

Figure 4G shows some of the common mistakes when traces are routed too close to antipads, plane splits or edges, thereby adding impedance to the return currents associated with the traces and worsening EMC. Note that from a SI viewpoint, adding impedance in a return current path has the same bad effect on waveshape as adding impedance in the send path (i.e. in the signal’s trace).
Planes are made of the same thin copper foil that is used for signal traces, so their resistance can sometimes be a problem where heavy d.c. or low frequency currents are employed. PCB manufacturers can ‘plate up’ the standard ‘½ounce’ (½oz) or ‘1oz’ foil thickness up to 8oz, to reduce plane resistance. Some PCB manufacturers can laminate metal sheets into a PCB, for use as a heat sink (sometimes called ‘thermal clad’ PCBs). Where their process allows the plated through holes and vias to make a reliable electrical connection to the metal sheet, plane resistance can be reduced considerably. Bonding the PCB’s 0V plane to its chassis can also help reduce plane resistance, and techniques for doing this were described in [8].

2.3 Cross-hatching and copper fills

A copper fill is not a plane, it is just a mess of RF resonators and antennas and worsens a PCB’s EMC performance. If there is an unbroken copper 0V reference plane layer on a PCB, a copper fill on another layer can be prevented from behaving as a mess of RF resonators and antennas by linking all parts of the fill to the unbroken 0V plane with via holes at least every $\lambda/10$ ($\lambda/20$ or less would be even better) at the highest frequency of concern, taking the $k$ of the PCB’s dielectric into account (nominally 4.0 for FR4). For example, to prevent copper fills
from acting as antennas at up to 1GHz, they should be via’d to the unbroken 0V reference plane every 15mm along their length and over their areas (preferably every 7.5mm or less).

A question that arises sometimes is whether a plane area should be created as a cross-hatched grid, rather than a solid copper area. Cross-hatched plane areas were used to help avoid PCB warping during automated soldering (where the whole PCB is heated) due to unequal amounts of copper on different layers (sometimes called ‘copper-balancing’).

Cross-hatched plane areas were common in the 1970s when the slow silicon technologies typically used in ICs allowed us to use double-sided PCBs with only partial plane areas. But a cross-hatched plane, even if extended to the full size of a PCB instead of being shared with traces, gives nothing like the EMC benefits of a solid copper plane. So to achieve copper balancing when using solid copper planes we must pay attention to the stack-up of the PCB, to balance the plane layers to achieve a symmetrical construction. (Stack-up will be one of the issues discussed in Part 7 of this series.)

Copper balancing using plane layers can sometimes result in more layers than are thought necessary for SI or EMC. In this case it is sometimes possible to add copper fills to one or more trace layers to prevent board warping during automated soldering. But remember that all parts of the copper fills must be via’d to an unbroken 0V reference plane at least every λ/10 at the highest frequency of concern, so they don’t worsen EMC.

2.4 Connecting devices to planes

Having gone to the trouble of creating planes with very low impedances (over the frequency ranges where we want to control EMC) – the benefits of the planes can be compromised by the impedance of the connections between the devices and the planes. So we need to minimise the inductance of the component-to-plane connections. This generally means (in order of importance)…
• Reducing the length of any trace (‘via-in-pad’ is best)
  This applies to any trace used to connect the component’s solder pad to the through/via hole that connects it to the plane layer.
• Increasing the width of any trace (applies as above).
  As a general guide, the inductance per millimetre length reduces as the square root of the increase in trace width. So halving the inductance requires the width to be increased four-fold.
• Reducing the spacing between the plane and the component, in the PCB’s ‘stack up’.
  This will shorten the length of the through-hole or via hole that is carrying the current, reducing its inductance. It is usually assumed that plated holes add a ‘partial inductance’ of about 1nH for each millimetre of their length that carries current (25nH/inch).
• Where through-holes or via holes carry opposing currents (e.g. the 0V and power pins of an IC) – placing them very close together (e.g. 1mm, or less if practical)
  Close spacing of opposing current paths maximises the mutual inductance between the two holes, effectively ‘cancelling out’ a proportion of their partial inductance. For example: two 0.5mm diameter via holes each carrying opposing currents for 1mm of their length, add a total of 1.2nH (0.6nH each) if they are 5mm apart, but only 0.53nH (0.26nH each) if they are spaced 1mm apart.
• Using multiple through-holes or via holes in parallel. The reduction in inductance is greater, the further they are apart. But if traces have to be used to increase the spacing, their extra inductance will reduce the benefit of paralleling.
• Increasing the diameter of a plated hole to decrease its partial inductance. As a general guide, the inductance per millimetre length reduces as the square root of the increase in diameter. So (for example) halving the inductance requires the diameter to be increased four-fold. Significant reductions in inductance therefore require quite large holes, with correspondingly large antipads perforating the planes, which can reduce the EMC benefits from those planes.

Figure 4H shows how these requirements are applied to the layout of some example decoupling capacitors.
Figure 4J shows how the bulleted requirements above are applied to some examples of component pin-escapes that connect to planes.

‘Via-in-pad’ has been mentioned above, and means that the plated hole that connects the component pad to the plane does so directly – the hole is situated within the pad’s area. Holes that penetrate right through a PCB, as is normal with THP PCBs, can ‘steal’ solder from the component’s terminal, possibly leading to dry joints and unreliable circuit operation with some kinds of automated soldering processes.

It is generally considered that via-in-pad can be used with THP PCBs that are wave-soldered, but that it is not a suitable technique for reflow soldering. However, the author knows at least one electronic manufacturer in the UK that uses via-in-pad on reflow soldered THP boards without any apparent yield or reliability problems. So it seems that some PCB manufacturers have skills or processes that others may not, and it may be possible to take advantage of their abilities to improve EMC cost-effectively.

Via-in-pad is normal practice when using HDI PCB technology (see section 5), because the via holes are very narrow in diameter and ‘blind’ – they end in a metal wall and do not go right through the PCB.
through the PCB, so they steal very little solder. This is one of the reasons why HDI or microvia PCBs are so good for EMC.

### 2.5 Thermal breaks

Planes were first used on PCBs for leaded components, and the thermal inertia of the plane often made the leads that connected to it harder to solder automatically. So it became commonplace to use a “thermal break pad” on the plated through-holes that connected to a plane. Thermal break pads use a thin trace (or traces) to connect the barrel of the through-hole to the plane, on the plane’s layer, thereby reducing the amount of heat lost to the plane during soldering and making the automated soldering of PCBs using planes easier.

As a result, many PCB designers got into the habit of always using thermal break pads on any plane connections, and this was made a rule in some PCB design departments. Thermal break pads increase the impedance of the plane connection, and whilst this was not significant for a leaded component (since there was a much higher impedance in its leads anyway) it can be important when using surface mounted components. These days, the impedance of a thermal break can be enough to reduce EMC performance at the high frequencies that are of concern these days.

For improved EMC without compromising automated soldering, thermal break pads should only be used for the through-holes associated with leaded components. They should not be generally used for via holes or the plane connections of surface-mounted components although they may be needed for ‘via-in-pad’ designs. Where thermal break pads seem to be necessary, they should be carefully assessed to see if they could compromise EMC. Maybe an adjustment to the normal automated soldering process might be enough to avoid the need for thermal breaks.

### 2.6 Device placement
The electrical activity in ICs and other semiconductors creates intense local fields around them. Where these fields couple with conductors, common-mode (CM) currents will be created. To optimise EMC these ‘leaked’ CM currents need to be returned to the silicon junctions they originated from as quickly as possible. Luckily, planes make excellent return paths for CM currents.

So, just as for traces (see above and Figure 4F): ICs, other semiconductors and crystals, should never be placed near plane edges, splits, or gaps. For high speed devices – e.g. ICs carrying digital signals with \textit{actual} rise or fall times of under 2ns (real rise/fall times, \textit{not} data sheet specifications) or analogue signals with frequencies of more than 200MHz – an unbroken plane is usually required under the IC and extending \textbf{at least} 5mm beyond its periphery.

A top or bottom 0V plane under an IC helps improve its EMC by providing an ‘image plane’ which is closer to it than internal plane layers can be. So, even when overall planes aren’t used on outer layers (see below), small plane areas under noisy devices (e.g. clock generators or buffers) can help, but they must always have multiple vias, spread over their whole areas, to an unbroken internal 0V plane.

Usually, a larger area of unbroken plane around an IC means better EMC: 10 or 15mm is not an unusual requirement even for 8-bit processors running at 16MHz on four-layer boards. Higher-speed devices need more attention to the design of their local planes. Unfortunately, the areas of the planes closest to an IC are usually the most highly perforated of any areas of the PCB, due to the antipads associated with the via holes for all the pin escapes.

Antipad diameters can only be reduced so far using ‘traditional’ THP PCB fabrication, but device pin-count is increasing so plane perforation near ICs is increasing. This problem is another reason for seriously considering the use of HDI PCB technology (see section 5).
The PCB’s stack-up is also important, with closer proximity of an IC to its nearest plane layer helping to improve EMC. Stack up issues will be considered in Part 7 of this series.

2.7 Fills and meshes

There is often great pressure from managers to reduce the number of layers on a PCB, to minimise the cost of the bare board. But the profitable selling price of a product has no direct relationship with the cost of its Bill Of Materials (BOM) – despite what many engineers and their managers still seem to persist in believing. This issue was discussed in detail in Part 1 of this series [6].

Nevertheless, it helps profitability if the cost of a bare board can be reduced by reducing the number of layers – but only as long as this does not create problems for SI or EMC that delay market introduction, require additional costs for filtering and shielding, or create unreliable or non-compliant products. So PCB layer reduction should now only be implemented as part of overall product EMC (emissions and immunity) and SI schemes under the control of competent staff supported by the necessary tools.

Another point to understand is that in reasonable volumes, 4 layer PCBs now cost little more than 2 layer (typically 20% more). But most PCB suppliers specialise in PCBs with a certain number of layers, usually 1, 2, 4, then 6 or more. So (for example) the PCB manufacturer that gives the best price for a 2-layer board will generally not give the best price for a 4 layer. Many engineers in companies using PCBs with 4 layers or less are put off increasing the number of layers, because their buying departments simply ask their usual suppliers for a price and don’t ‘shop around’ as they should.

Planes are the single most powerful and cost-effective EMC technique available in PCB design. So trying to save costs by reducing the numbers of plane layers often results in
increased costs overall, plus delay in time-to-market, and maybe increased warranty costs too (due to increased unreliability in real life electromagnetic environments).

When using 2 layer THP PCBs it is best for EMC to try to get all of the traces on one layer (usually the component side), and make the second layer as solid a 0V plane as possible. Where trace crossovers are required, it is best to use wire-link crossover components (‘zero-ohm links’) instead of ‘sneaking’ traces into the 0V plane area. If traces must be ‘sneaked’ into the 0V plane, they should be kept as short as possible. This technique is easiest to apply on analogue circuits, and the author has used it to improve the immunity of a domestic/commercial passive infra-red security device in an unshielded plastic housing, from 5V/m at 900MHz, to 50V/m, making false alarms due to nearby cellphone use very much less common.

Where it is impractical to employ an unbroken 0V reference plane in a PCB, a 0V mesh (or grid) should be created instead. A mesh should, usually achieve some useful degree of control over SI and EMC at frequencies up to those with a wavelength (in the PCB dielectric) no less than 10 times longer than the longest mesh dimension (its diameter or longest diagonal, \(D\)). In other words, for FR4 PCB dielectric with a \(k\) of 4.0: \(f_{\text{MAX}} = 15/D\) (\(D\) in metres gives \(f_{\text{MAX}}\) in MHz).

So, for example, an FR4 PCB with a 0V mesh with a \(D\) of 20mm should give some useful control up to 75MHz, with progressively less benefit up to maybe 250MHz. Above 250MHz it will give complex behaviour, probably including amplification of emissions and worsening of susceptibility at some frequencies. Remember that ‘some useful control’ does not mean the kind of performance that would be achieved by an unbroken copper sheet of the same area.

To achieve a meshed 0V area (it cannot be called a plane) on a 2-layer THP PCB, it is usual to route the two layers perpendicular to each other, then do a ‘0V copper fill’ on both layers.
Next, the top and bottom copper fills are ‘stitched’ together with manually placed via holes to make a mesh. This usually results in some large areas where there is no mesh – usually close to the microprocessor because the trace density is usually highest in that area.

Unfortunately, for the best EMC from our PCB we need the best control of the highest frequencies closest to the microprocessor, so it is normal to have to spend some time iterating the layout and redoing the copper fills and stitching, to improve the quality of the mesh (reduce the size of $D$ for each mesh element) over the whole PCB and especially near any microprocessors and their crystals and support ICs.

### 2.8 Resonances in the 0V plane

All conductors have electrical resonant frequencies that depend on the impedances of the media around their edges, just as they have acoustic resonant frequencies. A long thin conductor (e.g. a wire or trace) can be terminated in its characteristic impedance to its return conductor at one or both of its ends, to prevent any resonances – but this option is not available to 0V planes.

The resonant frequencies of a rectangular plane are given by:

$$f_{\text{RES}} = 150 \times \sqrt{(l/L)^2 + (m/W)^2}$$

This formula gives $f_{\text{RES}}$ in MHz if $L$ and $W$ (the plane’s length and width) are in metres. $l$ and $m$ are integers (0, 1, 2, 3 etc.) and correspond to the various modes of resonance, but it is usually only the first (lowest) resonant frequency we are most concerned with and this is easily found from: $f = 150/D$, where $D$ is the plane’s longest diagonal dimension ($D$ in metres gives the frequency $f$ in MHz, $D$ in millimetres gives it in GHz).

At its resonant frequencies a 0V plane can behave as a significant antenna, causing increases in emissions and worsening immunity. This appears mostly to be a problem for sensitive analogue circuits exposed to high levels of RF fields, for example during testing for immunity
to automotive industry immunity requirements. However, the segregation techniques described in [7] and the decoupling techniques described in Part 5 of this series – plus the circuit design techniques described in [1] to [5] – will help to reduce the effect of 0V plane resonances.

Where resonances in the 0V plane cause problems, it may be necessary to split the plane to create smaller plane areas for the problem circuits – but how the signals and power cross the resulting plane gap(s) is crucial and can easily cause emissions and immunity problems that are much greater than the improvements achieved by splitting the plane. Crossing plane gaps with low-frequency analogue signals is not difficult, using the techniques described in section 3 below using RC or LC low-pass filters (where the L is a soft ferrite bead) designed to give good attenuation up to the highest frequency of concern [12], [13]. However, crossing plane gaps with high frequency or high speed signals is very difficult.

In the 1980’s, splitting 0V planes used to be considered good EMC practice. But the short rise/fall times achieved in real life by modern ICs now makes splits a major embarrassment for EMC. Plane splits are such a big problem for EMC that for many PCBs it is much better to use an unbroken 0V reference plane over its whole area. The issue of splitting planes is very important, especially given its history as a recommended EMC technique, so it is discussed in detail in section 3 below.

2.9 Cavity resonances in plane pairs

Two or more 0V planes are employed in a PCB to permit the use of transmission-line traces on several layers (see Part 6 of this series); or to route stripline transmission lines; or for ‘copper balancing’ (see above) to prevent board warp during automated soldering. 0V and power planes are often used as adjacent pairs in PCB stack-ups, to provide high-frequency decoupling of the power supplies to the ICs (see Part 5 of this series).
But pairs of planes can suffer from cavity resonances in exactly the same way as was described in Part 3 of this series [8], for the cavity resonances between a 0V plane and a metal chassis. And when they resonate their impedances at some locations can be much higher than normal, and their voltage differences at those locations will be much higher too. The natural resonant frequencies for a rectangular plane pair are given by similar equations as were used for a single rectangular plane, above, and for a rectangular plane-chassis [8] cavity. But because the cavity between the planes is now filled with a PCB substrate with dielectric constant \( k \), the speed of electromagnetic propagation in the cavity is less and this makes the frequency associated with a given wavelength lower. So the resonant frequencies of a plane pair filled with \( k \) are given by:

\[
\text{f}_{\text{RES}} = \left(\frac{150}{\sqrt{k}}\right) \times \sqrt{(\frac{l}{L})^2 + (\frac{m}{W})^2}
\]

This formula gives \( \text{f}_{\text{RES}} \) in MHz if \( L \) and \( W \) (the plane pair’s length and width) are in metres. \( l \) and \( m \) are integers (0, 1, 2, 3 etc.) and correspond to the various modes of resonance, but it is usually only the first (lowest) resonant frequency we are most concerned with. For FR4 material (\( k \) nominally 4.0) this is easily found from:

\[
f = \frac{75}{D}, \quad \text{where } D \text{ is the plane’s longest diagonal dimension (in metres gives the frequency in MHz, in millimetres gives it in GHz)}.
\]

For non-rectangular planes that are not simple shapes, it will usually be easiest to determine their resonant frequencies by computer simulation using field solvers, or measurement of a test PCB. But their lowest resonant frequency will still be easily estimated as \( \frac{75}{D} \) MHz (for FR4, with \( k = 4.0 \)) where \( D \) is the plane’s longest dimension, in metres.

To prevent cavity resonances from occurring in the frequency range of concern for EMC, all the 0V planes (including any small or broken plane areas) should be interconnected with via holes spaced \textit{no more} than \( \lambda/10 \) at the highest frequency of concern, taking the dielectric constant of the PCB, \( k \), into account as described above. So, for example, to prevent cavity
resonances in a plane pair at frequencies up to 1GHz, plane-linking vias should be located no more than 15mm from each other, all over the planes’ areas. Closer spacing of the vias will give better EMC.

Figure 4K shows a tested example of a small test PCB with its top and bottom layers dedicated to unbroken 0V planes. This was not a functional PCB, just something to test the idea of linking 0V planes together with vias to see the effect on the cavity resonant frequencies. Figure 4K shows that the first resonance at approximately 2GHz was moved higher in frequency by the addition of some interplane vias, giving a 20dB reduction in plane impedance at 1.5GHz, implying a significant improvement in EMC performance up to that frequency.

The partial inductance of the via holes (at 1nH per mm of their length) prevents them from being a perfect short-circuit between 0V planes, especially at the very high frequencies (1GHz and above) that must be considered in modern PCBs. For example, a 1.5mm via hole has an impedance of about 10Ω at 1GHz. This should be compared with the natural impedance of a solid 0V plane at 1GHz, which can be lower than 0.03Ω if it is far from resonance, and as much as 10Ω at its resonant peak.
0V/power plane pairs obviously cannot be stitched together with vias, instead, we use ‘decoupling’ capacitors, often known as ‘decaps’. Unfortunately, discrete decaps are severely limited in their effect above 500MHz due to their internal self-inductance and the inductance of their current loop comprising pads, traces, via holes connecting them to the 0V and power planes, and the area they enclose.

However, we can place 0V and power planes much closer together in the PCB’s stack-up, and this reduces the fringing fields around their edges – the principal cause of emissions from a plane pair. Halving the 0V/power plane spacing generally halves the emissions – if all else is held equal – but reducing the spacing between 0V and power plane can also reduce emissions (and improve immunity) for a given circuit, as discussed in Part 5 of this series. The fringing fields around a pair of planes are sometimes called ‘edge-fired’ emissions.

One of the consequences of very close 0V/power plane pair spacing – 0.05mm (2 thou) or less – is that the peak amplitude of their impedance at resonance is decreased. Another way to put it would be that the ‘Quality factor’ (Q) of the cavity is reduced. By using much thinner dielectric layers than normally used in THP PCBs it is possible to reduce the Q to 1, at which point the cavity created by the planes does not resonate at all, no matter what its size or shape. This will be discussed in more detail in Part 5 of this series.

One of the reasons for the high Q of the cavity formed by a pair of planes (where their spacing is more than 0.05mm) is that there is very little loss in the cavity to provide damping. In fact, real PCBs usually have lower peak resonances than suggested by simple computations or test boards, because of the damping provided by the presence of lossy electronic components. Damping can be deliberately added by replacing some of the interplane vias by resistors with between 2 and 10Ω. In the case of 0V/power plane pairs, some of the decaps have a resistor added in series with them. Some component manufacturers are understood to have standard
products consisting of a capacitor in series with a resistor, specifically for 0V/power plane pair damping.

There usually only need be a few damping resistors spread around a PCB, for best effect they should be placed at the resonant ‘hot-spots’, where the RF voltage differences between the planes are the highest. For simple plane shapes it is possible to predict where the lowest frequency resonant ‘hot spots’ will probably occur, although device loading may modify their actual locations. Computer simulation or experiments will probably be required on most PCBs to find the best locations.

Loading the PCB’s dielectric with particles of ferrite absorber also helps dampen resonant peaks, and may well reduce emissions in other ways. But this is not yet a common method, because the ferrite particles increase the wear on the PCB punching and drilling tools. Maybe when laser-drilled HDI PCB technology (see later) becomes commonplace, ferrite-loaded substrates will become more attractive.

Another way to reduce cavity resonances is by careful design of the planes’ shapes. This will have little effect on the lowest frequency, which is governed simply by the longest dimension, but may have a useful effect on some of the higher frequency resonances.

Where the length \((L)\) of a rectangular plane is an integer or other simple multiple of its width \((W)\), such as 1, 1.5 or 2, the resonant frequencies of the length and width directions will coincide at some frequencies, causing higher-Q peaks (more intense resonances) than usual.

Murphy’s law tells us that when the clock frequency is changed just before product launch to get the best performance out of the latest microprocessors, these higher than usual resonances will just happen to coincide with an important clock harmonic that cannot be filtered out, causing problems for EMC compliance at a time when it is very costly and time-consuming to make any changes and delay that cannot be tolerated.
So it is best to avoid square planes and simple $L:W$ ratios – ideally, choose irrational numbers. There is an infinite number of irrational numbers to choose from and the author recommends the use of the 'Golden Mean': 1.618…etc… (call it 1.62), because (as Renaissance artists and ancient Greek architects knew) – it gives a pleasing appearance. Thin planes should always be avoided (i.e. the $L:W$ ratio should never be larger than 3 or smaller than 0.33). It may also help a little to have non-parallel plane edges, and to avoid simple regular shapes such as rectangles or circles.

2.10 Reducing the 'edge-fired' emissions from plane pairs

When plane pairs resonate, their emissions come from the fringing fields at their edges. This is why they are sometimes called ‘edge-fired’ emissions. 0V/power plane pairs can reduce their edge-fired emissions by reducing their spacing, as described earlier, but this technique cannot generally be used for multiple planes.

We would like to have some way of reducing these edge-fired emissions that did not involve costly enclosure shielding, and one technique that is sometimes recommended is the ‘20H rule’. The 20H rule requires all reference planes (0V or power), except for the main 0V reference plane, to be smaller than the main 0V plane by 20 times their layer spacing. This modifies the shape of the fringing fields, but there does not seem to be much hard evidence for significant reductions in emissions using this method.

Using a ‘decap wall’ can reduce the emissions from the edges of 0V/power plane pairs. The decaps (typically in the 100pF - 10nF range) are located all around the periphery of the power plane, which should be at least ‘20H’ inside the 0V plane periphery.

For any plane combinations, the general technique recommended here is called a 'PCB guard ring'. Don’t confuse this with guard ring techniques that may have been used in the past – this requires wide guard traces on both outer PCB layers all around the perimeter of the main 0V
plane(s) – with the two traces connected together and to all the 0V planes by a ‘via wall’ or ‘edge plating’.

Wider guard traces give lower emissions, with top and bottom planes being the best. All of the 0V planes in the ‘guard ringed’ area must extend right to the edge of the area, their edges aligned with the outer edges of the two guard traces. The guard traces must have a minimum width of 3mm, and be widened or extended into the PCB area at every opportunity. There is no point in extending the guard ring with thin traces. All guard ring areas created by widening or extending the guard traces must be linked to the main 0V plane with vias spaced according to the guide for preventing plane resonances, above.

The use of top and bottom planes leads us to consider the possibility of totally shielding the PCB, and this is dealt with in section 6 below.

The vias in a via wall link the top and bottom guard rings and all of the 0V planes’ edges together – all around the perimeter of the 0V planed area (usually the outline of the PCB). The spacings between the vias in a via wall should be less than \( \lambda /50 \) (taking the dielectric constant, \( k \), of the PCB substrate into account) at the highest frequency of concern. So to control emissions up to 1GHz the spacing between the vias in the via wall must be no more than 3mm. This is equivalent (in FR4) to a spacing of 10mm x risetime in ns (the real risetime, or the falltime if it is shorter, not the data sheet value). Where the guard rings traces are wide enough, they should have extra linking vias between them and all of the 0V planes all over their area, as described in the section on plane cavity resonances above.

Figure 4L shows an example of the use of a guard ring on a PC expansion board. In this example guard traces have been placed on every PCB layer except for the 0V plane areas. This helps to ensure that no traces or power planes get too close to the edge of the 0V plane (see earlier), so is a helpful design rule, and it also helps a little to reduce the edge-fired
emissions. Of course, the top and bottom guard traces cannot be routed where there is an edge connector, but the guard tracers on the internal layers can be, and this helps reduce the emissions that are caused by any gap in the guard ring.

The example in Figure 4L is for a PCB with a single overall 0V plane. Where split 0V planes are used, each plane area should have a via wall around it (as shown in Figure 4L) so some of the 'perimeter guard traces' and their via walls will now lie inside the PCB's overall perimeter. Areas of circuitry with separate 0V planes are — of course — 'segregated circuit zones' as described in Part 2 of this series [7] and any conductors interconnecting them, whether wires or traces, should be treated as [7] recommends. Please note that split 0V planes are not generally recommended these days — this is discussed in detail in section 3 below.

Instead of a via wall, some designers use 'PCB edge plating' to link the guard traces and 0V planes together around the perimeter of the 0V planes. This uses the 'de-smearing' PCB fabrication technique that plates the barrels of the through-holes and vias, to plate the edges of the PCB as well. Some companies edge-plate with no problems, whilst others have difficulty, so it seems that not all PCB manufacturers have equal skills or processes.

2.11 Locating via holes for aggressive signals or power
The return currents associated with via holes excite the cavity resonances in plane pairs. This is one reason why it is important to route all of the most aggressive signals (e.g. clocks, strobes, etc.) on a single PCB layers, as far as possible (described in more detail in Part 7 of this series).

But the excitation caused by via hole currents can be minimised, improving EMC, by locating these via holes at the places where the plane pair resonance causes a low impedance to occur at the cavity resonant frequency of concern [14]. For simple plane shapes, determining where these low-impedance points occur can sometimes be done by inspection and simple mathematics (see above) – but complex plane shapes will require a computer simulation of the PCB, or experiments with a test board.

For the best EMC, the most aggressive signals should generally be routed as striplines, which are sandwiched between two planes (described in Part 6 of this series). If these striplines are kept on a single layer, they will only have to change layers at their ends to connect to the devices soldered to the outer layers of the PCB. So to improve EMC the devices that drive these aggressive traces should be placed at the places where the cavity resonances cause low impedances.

2.12 When traces change layers

The RF plane return currents associated with traces (see Figure 4A) are forced by ‘skin effect’ to flow in the surface of the plane that is closest to the trace. When traces change layers, their surface RF return currents cannot flow through the thickness of the plane. So where a trace becomes routed against the other side of the same plane, its return current will flow to the other surface around the rim of the antipad in the plane created by the via hole for the trace.
Where a trace becomes routed against a different plane at the same voltage (usually 0V) the interplane capacitance is insufficient to make a good connection – so a via hole should be added to link the two planes together very close (i.e. < 3mm) to the trace’s layer-change.

But where a trace becomes routed against a plane with a different voltage, it is important to fit a decoupling capacitor between the two planes, very close (i.e. < 3mm) to the trace’s layer-change. The return current will pass through the decap, so the value and type of decap, and its self-resonant frequency, should be chosen to suit the spectrum of the signal.

As will be discussed in Part 6 of this series, adequately controlling the return current path for very high-speed signals for good EMC may require no layer changes along the length of a trace, except for the connections to the devices at either end of the trace. This often leads to an increase in the number of plane layers.

2.13 Component-side planes for DC/DC converters and clocks

Transient currents in DC/DC converters can be very intense and even in the low impedances of an unbroken 0V plane can give rise to significant amounts of noise, possibly due to the resistance of the plane. So most DC/DC manufacturers recommend a separate very small component-side 0V plane for the DC/DC components, that is only connected to the main 0V plane at one point by a single large-diameter via (or by a number of smaller vias grouped closely together).

3 Splitting a 0V plane is not generally a good idea any more

Never split a 0V plane just because ‘we always used to do it’, or because any EMC guideline or IC application note says so. It used to be traditional to split planes between analogue and digital areas, but the author has found on hundreds of PCB designs since 1981 that PCBs can generally be designed to have better signal quality and EMC by using one 0V plane for all the circuits. Many other electronic designers have found the same. It is not unusual for analogue
signal quality to be significantly better than what had previously been considered for decades
to be the state of the art.

Due to the small silicon processes used in modern ICs, split 0V planes should now only be
used as part of a well thought-out EMC plan, implemented by people who are sufficiently
EMC-competent and equipped with all necessary EMC tools. 0V plane splits of any practical
width don’t work well as splits above 1GHz anyway, and hardly have any effect >2.5GHz, due
to the reducing impedance of the stray capacitance across the split as frequencies increase.
The problem is that – for traces that must cross a 0V plane split – it is very important indeed to
maintain the intimate proximity of the send and return currents. This is not always easy, or
low-cost, but if it is not done correctly the resulting degradation in EMC will be much worse
than the benefits that could ever be hoped to be achieved by the use of a split. How to deal
with traces that cross plane splits is discussed in the next section.

One way of dealing with uncertainty over whether to split a 0V plane or not, is to construct a
prototype PCB designed to provide both options, then test it to see what works best.

Because the circuit has been laid out on the PCB in segregated circuit zones, as described in
[7], it is easy to split the 0V plane between these zones. Then pad patterns that can be used
for small capacitors, resistors or zero-ohm links should be placed at regular intervals around
all the perimeters of all of the plane splits, so that they can be used to connect between the
planes on either side of the split. These are often called ‘plane stitching’ components, and

Figure 4M shows the general idea.
The spacings between the plane stitching components, around the perimeter of a split, should not exceed $\lambda/10$ at the highest frequency of concern (calculating $\lambda$ taking the PCB dielectric’s $k$ into account). So, for example, to control up to 1GHz in an FR4 PCB, the spacing between the stitching components should be no greater than 15mm.

The prototype PCB should employ as near to the final circuits and software as possible, and be tested for signal quality (analogue), SI and EMC, starting off with no stitching components fitted at all (except for any zero-ohm links used to connect to each plane at a single location, if this is not already done with traces). There is no need to apply full EMC testing as if for a final product – it is often possible to test emissions well enough on an ordinary laboratory bench using close-field probes and a low-cost or hired spectrum analyser. See [15] for close-field probe construction details.

Capacitors of various values (usually in the range 1-100nF) are then fitted to some or all of the stitching pads to see if the functional performance is improved and emissions reduced (or immunity improved). A single plane connection at d.c. plus capacitive stitching can be regarded as a hybrid plane bonding scheme, rather like the hybrid chassis bonding scheme discussed in [8]. Zero-ohm links can also be fitted at some or all of the stitching pads, and if
resonance is suspected it might be worthwhile trying some resistors (or series resistor-capacitors) instead.

It should be borne in mind that unless all of the stitching components are fitted, adequate control of SI and emissions may not be achieved at the higher frequencies of concern. In some cases adding a few stitching components might make some emissions worse, but adding more might make it better than the initial result.

The alert reader will, of course, have spotted that the range of possible stitching experiments is enormous. Most designers will try a few obvious alternatives, for example…

- all stitching pads fitted with zero-ohm links
- all stitching pads fitted with capacitors, using 1, 2.7, 4.7 and 10nF devices in turn around each perimeter.

Then they will iterate depending on which gave the best results compared with the initial experiment with only the essential d.c. plane connections.

Although the author prefers not to split 0V planes at all, there are some instances where it is essential, for example where there is a galvanically isolated circuit zones sharing a PCB. In this situation the galvanically isolated area of 0V should be stitched to the main 0V plane with a number of small capacitors spread around the perimeter of the split according to the above rules, as shown in Figure 4N.
The plane split provides the necessary galvanic isolation at d.c. and powerline or even audio frequencies, and the stitching capacitors approximate (as best as they can) the benefits of an unbroken 0V plane over the whole PCB at RF. The stitching capacitors often need to be high-voltage types. Where safety is an issue, the types and values of the capacitors will usually need to be chosen for safety as well as for EMC reasons.

4 When traces must cross a 0V or power plane split

Where possible, never allow a trace to cross a plane split because it is difficult to control the trace’s return RF currents (which flow in the surface of the adjacent plane or planes) so as not to cause EMC problems. Some designers think that low-frequency analogue signals or power have no RF content so there is no need to worry about the RF return currents for such traces, but such signals and power are always vulnerable to RF interference, so the same PCB EMC design techniques should be applied.

In any case, any product that employs switch-mode power conversion (e.g. DC/DC converters) or clocked digital circuits (e.g. a microcontroller) has common-mode RF currents flowing in all of its traces, whatever the type of signal or power they are intended to carry. Common-mode
currents are the major cause of EMC problems, so all of the EMC techniques described in this series apply to all traces, unless otherwise noted.

Issues concerning the splitting of 0V planes were discussed in the preceding section, and 0V planes should only be split as part of a well-thought-out EMC plan. But power planes are often split, and the best way to deal with traces that would have to cross power plane splits is to add an unbroken 0V plane between the traces and the power plane layer.

But if you must cross a split with a trace – you must provide a return path as physically close to the send path as possible, even if this creates a short-circuit across the split. At the frequencies of concern for EMC these days it is much more important to keep the return current path intimately associated with the send path, than it is to employ split planes.

To help maintain the purpose of the plane’s split without worsening EMC too much, the send and return current paths for each trace must be filtered so they are band-limited to suit the wanted signal (or fitted with a CM choke). This allows the split to continue to provide isolation at other frequencies. Figure 4P shows a number of examples of filters fitted in send and return paths crossing a split, but only the series element of each filter that crosses the split is shown, to make the figure easier to read.
Where the bandwidth must be the highest and no filtering is possible, the return path must be a trace at least three times wider than the signal trace (see figure 4A), on an adjacent layer, centred under the signal trace. Closely-coupled differential transmission lines are the least affected by crossing plane splits. Coplanar transmission lines can be used instead, for single-ended or differential lines. For more on transmission lines, see Part 6 of this series.

CM chokes wind both the send and return current paths in the same direction on a magnetic core. They have little effect on the differential-mode (DM) current (the wanted signal) but put an impedance in the path of the CM current. Consequently CM chokes are ideal for use when signals must cross plane splits — they have very little filtering effect on the DM signals’ send and return current paths — and they help maintain the purpose of the split. CM chokes are now available in a wide variety of impedances and current ratings, and recent developments include types suitable for USB2 and similar high-speed serial communications. Unfortunately, CM chokes are not the cheapest or smallest components.

After providing all the necessary filtering or CM chokes for the send and return paths, as described above, experiments on late-stage prototype boards should be conducted with the values, numbers, types and locations of the ‘plane stitching’ components, to see if emissions or immunity can be further improved. These experiments have already been briefly described in the preceding section.

5 Advantages of ‘High Density Interconnect’ (HDI), ‘build-up’ and ‘microvia’ PCB technologies

These are all different terms for essentially the same PCB technology, which I shall call ‘HDI’ in this series. HDI PCBs use plated via holes that are no taller than the layers they interconnect. Instead of laminating all of the layers and then drilling all of the via holes right through the whole PCB stack, HDI drills and plates the vias in each layer separately, using
micro-via holes that are very small – typically 0.15mm diameter (6 thousands of an inch). The micro-via holes don’t steal solder, so via-in-pad can be used. There are a number of other EMC advantages to HDI PCBs, and they will be discussed in more detail in Part 7 of this series. A comprehensive review of HDI and its benefits can be found in [16], and the basic standard for the design of HDI PCBs is IPC-2315 [17].

For the purposes of this article, the EMC advantage of HDI technology is that it is possible to create very dense PCBs that include reference planes with very few perforations. These planes are a much closer approximation to the ideal unbroken copper sheet than can ever be achieved using THP PCB technology.

Because of its ability to create unperforated planes with high performance, HDI technology is already used in cellphones, high-power computing and telecommunications products. As IC feature sizes continue to shrink, and as component density on PCBs continues to increase, HDI PCBs will be more widely required. HDI is used in high-reliability products because their microvias are more robust than vias that are drilled right through a PCB. HDI techniques can reduce the area of PCB required by 40%, reduce the number of layers by 33%, and be much easier to design [16].

The usual complaint when this is mentioned is that the PCBs will cost more – but the author remembers this same complaint being raised when double-sided PCBs were first proposed, then again when THP was developed, then again when 4-layer THP PCBs were starting to become necessary, and then again when 4 layers were no longer enough.

Now more than 50% or the world’s production of PCBs use 6 or more layers, and are used in personal computers and cellphones that cost much less than equivalent products – using simpler PCB technologies – did years ago. So when anyone complains about the high cost of a new PCB technology, they should generally be ignored. New PCB technologies are
continually being required to create products that are more powerful and cost less, very strongly driven by the developments in ICs and their packaging. Continuing to use an old PCB technology simply to minimise bare-board cost can make products less competitive. The profitable selling price of a product is not determined by simply multiplying the cost of its BOM by some pre-determined number (see section 1.2 of [3] for more on this).

However, an IPC survey in May 2000 found that HDI PCBs could be purchased for the same bare-board price as ‘traditional’ THP. So, in reasonable volumes, there should now be no need to pay more for a HDI PCB than for a THP one. As time goes on and the PCB manufacturers pay off their HDI production machines, the break-even point between THP and HDI will no doubt occur at even lower volumes.

These days, the use of HDI PCB technologies can reduce the costs of assembled PCBs (never mind reducing the overall product cost by reducing the requirements for enclosure shielding and filtering). Where Ball Grid Arrays (BGAs) with less than 1mm pitch, or when chip-scale, Tape Automated Bonding (TAB), or flip-chip packaged devices are to be used – HDI is probably essential for SI, EMC, time-to-market and low cost.

6 The totally shielded PCB assembly

This section does not really belong in an article on planes, but it grows naturally out of the guard ring technique described earlier so it is included here.

A totally shielded PCB assembly is a big help in achieving a product’s EMC quickly at the lowest cost (see [6]), and thanks to the recent advances in low-cost PCB shielding techniques (see [7]) it is no longer difficult or costly, and still allows the whole PCB assembly to be automatically soldered in one pass, with no need for an additional hand-assembly stage.

By extending the guard ring traces (see the section above) by so much that they create top and bottom 0V planes, most of the PCB will be shielded. We might call these ultimately
extended guard rings ‘guard planes’. Only the devices on the PCB and the external wires and cables are left to cause EMC problems.

PCB-mounted shielding cans, and the filtering of unshielded cables as they exit a 0V planed area, were both discussed in Part 2 of this series [7]. Shielded cables need good shielding connectors bonded all around their periphery to the 0V plane or PCB shielding can wall. Combining these techniques with ‘guard planes’ allows the creation of totally shielded PCB assemblies.

Of course, maximising the area of 0V plane on the top and bottom PCB layers will prevent them from being used for routing. But the guard planes will have gaps in them where the components are soldered to their pads, and for the short traces required for their break-outs and pin-escapes to connect to internal routing layers.

Of course, as discussed earlier, all areas of the top guard planes must be connected to the bottom guard plane (as well as the via wall or edge plating) – and to all the other internal 0V planes – by vias spaced every λ/10 at the highest frequency of concern (calculating λ taking the PCB dielectric’s k into account), over the whole PCB area to prevent plane resonances. Closer via spacing is better.

Figures 4Q and 4R show examples of fully shielded and partially-shielded PCB assemblies, using the techniques discussed so far in this series.
7 EMC-competent QA, change control, cost-reduction

See section 8 of Part 3 for a discussion of this important issue.

8 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques – but in real-life there are a great many design trade-offs (compromises) to be made, and this is where the circuit and PCB designers really earn their keep.

Designers are often put under cost or time pressure by managers who don’t understand the technical trade-offs, and so don’t understand that their actions could have the opposite effect.
to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of this series [6], plus the final section of part 2 [7].

9 References


http://www.compliance-club.com/KeithArmstrongPortfolio


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I would like to reference all of the academic studies and other papers that back-up the practical techniques described here, but the reference list would take longer to write than this series! However, I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.
Some other useful textbooks are:


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Advanced PCB design and layout for EMC -
Part 5 Decoupling, including buried capacitance technology

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the fifth in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout ("Part 5 – PCB Design and Layout", October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not spend much time analysing why these techniques work, they will focus on describing their practical application and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1. Introduction to decoupling
We need very low impedances in the power distribution networks (‘power busses’) that provide DC voltages to the devices on our PCBs, so that the fluctuating current demands of the ICs and transistors don’t cause excessive emissions of electric and/or magnetic fields. These fluctuating currents are caused by…

- Stray capacitances associated with the loads on the signals
- Shoot-through currents in totem-pole drivers
- Core (processing) noise

These three sources of current ‘noise’, and the resulting voltage noise created as they flow through the power bus impedance, are shown by Figure 5A.

‘Stray’ capacitance is unavoidably associated with all signal loads (e.g. an input to a CMOS IC or an operational amplifier) due to device terminals, lead frames, bond wires, and the capacitance associated with the internal semiconductor features. To this must be added the stray capacitance of the traces and pads of the PCB itself. The capacitances involved are quite small, often just a few tens of pF in total. As the transition time of digital signals continues to decrease (see Part 1 of this series [6]) the transient currents created by charging and discharging the capacitances associated with a load increase, increasing the levels of the emissions from the power busses.
‘Shoot-through’ currents are created by totem-pole type driver circuits, at the instant of their switching. For a very brief time, both the upper and lower transistors in the totem pole are ‘on’ together, momentarily shorting out the power bus. It is possible to design totem-pole driver circuits so that the conduction times of the upper and lower devices do not overlap, and this is often done in high-power switch-mode converters to prevent actual device damage from the very high currents that flow when the power bus is short-circuited, but it not typically done in digital ICs. The inductance in the path of the resulting current limits the rate of rise of the shoot-through current, which would reach very high levels if the shoot-through period was not so short.

The shoot-through current of a modern 74HC glue logic device can exceed the current fluctuations caused by driving its output signals by as much as 15dB at frequencies above 30MHz. And despite its data sheet rise/fall time specification of 5ns (maximum) both of these noise currents can exist at significant levels at frequencies up to (and maybe beyond) 600MHz.

The inductances associated with the power bus inside an IC cause voltage noises (with respect to the PCB) to appear on its internal 0V and power voltage references. These noises are called ‘ground bounce’ and ‘rail bounce’ (sometimes: ‘rail collapse’). Because these noises occur on all of the IC’s input and output pins they contribute to the common-mode noise emissions from a device and from the PCB it is mounted on. It can be important for good EMC performance of a PCB to design or select ICs to have a low ground-bounce and rail-bounce, but device selection is not a subject of this series of articles (see [1] or [2] instead).

Core noise is a feature of VLSI ICs, such as microprocessors and large FPGAs, which have a core of semiconductors operating at very high speeds. These internal circuits have to drive
signals into internal capacitive loads, can suffer from shoot-through currents, and their transient current demands add to an IC’s overall current fluctuations. The frequencies of core noise currents are usually much higher than those from the other two causes, for example: the core of some Xilinx FPGAs can have power current demands with 50ps durations – equivalent to a noise frequency spectrum that extends to at least 13GHz.

Magnetic field emissions are dealt with by making the areas enclosed by the DC power current loops as small as possible. Where the 0V and power is supplied by traces, these traces must be as close together as possible, usually achieved by routing 0V and power traces side-by-side or broadside along their whole route.

But Part 4 of this series [7] showed how important a PCB 0V plane is for EMC, for a variety of reasons, and when we have a 0V plane we achieve a small current loop by routing DC power ‘bus’ traces (often called power busses or power rails) on a PCB layer that is adjacent to a 0V plane. Closer layer spacing means smaller loop areas and lower emissions.

[7] also mentioned the use of a 0V/Power plane pair, in which both the 0V and power distributions use planes, on adjacent layers. Using this technique in a PCB stack-up achieves the minimum possible current loop area. Closer 0V/Power plane spacing means even smaller loop areas and lower emissions of magnetic fields.

Electric field emissions are dealt with by making the impedance of the power bus – at the point of connection of the IC or transistor that is drawing fluctuating currents – as low as possible at all of the frequencies of concern. This aims to reduce the magnitude of the fluctuating voltages created by the fluctuating DC currents, because smaller voltage fluctuations will give rise to lower electric-field emissions. The classical way of achieving a low impedance at the point of connection is to fit a capacitor there – known as a decoupling capacitor, or decap. Also, closer
spacing of the power bus and its 0V return reduces the amount of electric field emitted, for a
given power bus noise voltage.

The distributed capacitance of a 0V/Power plane pair is another way of achieving a low power
bus impedance, aided by the low DC resistances of planes (versus traces) and also by the
high mutual inductance between the two adjacent planes. Closer 0V/Power plane spacing
generally means lower power bus impedances.

Unfortunately, decaps are not perfect capacitors and 0V/power plane pairs can cause
problems if not designed carefully – as a result, effectively decoupling modern PCBs can be a
difficult task. The rest of this article explores these issues and how they are overcome at
present. It then goes on to describe the buried capacitance technique that – along with HDI
(see section 5 of Part 4 [7] and Part 7 of this series) – will no doubt be as ubiquitous and
‘normal’ in a few year’s time, as FR4 and through-hole-plate (THP) PCBs are today.

Bypassing is another word for decoupling, and bypass capacitors another description for
decoupling capacitors. This series does not use the ‘bypass’ words – partly because ‘decap’ is
a nicer abbreviation than ‘bypasscap’.

2. Decoupling with discrete capacitors

Unless otherwise stated, this section of this article assumes a 0V plane with low impedance at
the highest frequency of concern (see [7] for design details) – and power distribution using thin
traces.

2.1 Which circuit locations need decaps?

Because of the very high switching speeds now achieved by digital ICs due to the continual
die-shrinking by the semiconductor industry (“Moore’s Law”), decaps are now required at
every power pin of every IC (even old-fashioned glue logic) as shown by Figure 5B.
And to improve emissions and immunity performance decaps are also required at least at every other location on the PCB where fluctuating currents are drawn from a power bus, whether the circuits are digital, analogue, radio-frequency, or switch-mode.

Whichever DC voltages they are connected to, all decaps should connect to the 0V plane used by the circuit their device is a part of. (See [7] for more on 0V planes, including what to do with a galvanically isolated area of 0V plane).

It also helps EMC to fit decaps near to every off-board connector, whether they carry signals or power. And fitting decaps to the voltage reference nodes of operational amplifier and comparator circuits, and the voltage reference pins of A/D and D/A converters, can also help improve functionality and improve immunity to EMI.

2.2 The benefits of decaps in ICs and MCMs

The most effective decoupling per pF of decap is achieved by silicon nitride decaps actually created in the silicon die of an IC itself. The next most effective use of decap pF is mounting decaps in an IC’s package (‘hybrid circuit’ construction) – and mounting decaps on a multi-chip module (MCM), as is done with Pentium IV™, is the next in effectiveness.
The above three decap locations are the most effective at controlling the very highest frequencies because they achieve the smallest possible size of current loop. So when choosing devices or designing FPGAs or ASICs or MCMs it will greatly ease the design (and cost) of the PCB power bus decoupling if as much decoupling capacitance as possible is embedded in the silicon chips or on the MCMs themselves.

It is very important that the discrete decaps used have the very lowest ESL – such as is achieved for example by AVX’s IDC and LICA devices, and X2Y® devices (see section 2.4). Going any further with this topic would be outside the scope of this article.

### 2.3 How much decoupling capacitance to use?

The basic functional reason for decoupling digital ICs is to maintain the voltage rail within certain specified tolerances despite their fluctuating current demands. It is easy to calculate the amount of decoupling capacitance $C$ required for an IC using the expression $C \Delta V = I \Delta t$.

$\Delta V$ is the maximum permitted reduction from the actual power bus voltage, in Volts, that will still permit the IC to function correctly – and is easily calculated from the worst-case power bus voltage (taking into account regulator initial tolerances, temperature coefficients and operating temperature ranges, ageing coefficients, the voltage drop due to the resistance between the power bus and the IC, plus the minimum operating voltage specification from the IC’s data sheet). $I$ is the maximum current demand in Amps and $\Delta t$ is the time this demand exists for.

The problem is that it is difficult to specify $I \Delta t$ for modern VLSI devices because it is a fluctuating quantity that depends on the operational mode of the device and the loads it is driving. But it may be possible to measure an IC’s transient current demands with a high-frequency current probe, when the IC is operating in representative worst-case conditions.
It often turns out that 10nF is sufficient for decoupling glue logic, but most VLSI devices will need more and their manufacturers will usually recommend how much. For example, Xilinx [8] recommend using much more than $1/m$ times the ‘equivalent switched capacitance’ (where $m$ is the maximum percentage variation permitted in the power bus voltage at the IC’s power pin).

Equivalent switched capacitance is defined as $P/V^2$ (where $P =$ the total wattage consumed by the IC; $V =$ its DC supply voltage; $f =$ its clock frequency).

Xilinx say that once the equivalent switched capacitance has been determined, it is multiplied by much more than $1/m$ to find the total capacitance required by the IC, then this total is divided by the total number of power pins connected to the same power bus to find the value of capacitance to be placed near each of the pins connected to the power bus in question.

A significant problem is that the type of decap used and/or the inductance in the current loop formed by the decap and its associated IC, could prevent the decap being effective when there are fast fluctuations in device power bus current. As a result, good VLSI manufacturers generally provide a wealth of data on how to decouple their devices (for example, [9] from Xilinx).

Our discussion on decoupling in section 2.3 has so far concerned decoupling for reliable functionality, but decoupling to improve EMC performance at PCB-level is much more difficult. So please be aware that IC manufacturers’ application notes and other decoupling advice might not be as good as the very up-to-date EMC practices described in the rest of this article.

### 2.4 Types of decaps

The best decoupling capacitors are surface-mounted multilayer ceramic (MLCC), because ceramic dielectrics are true electrostatic barriers (charge separation devices) that can release all their charge at whatever rate is required. In practice, their rate of discharge is limited by the self-inductance (‘equivalent series inductance’, or ESL) of the device and the inductance in its
external circuit (which are also limitations for all other types of capacitors). MLCCs especially designed for high frequencies exist, such as the Murata GRH700 series, and some designers prefer to use them, but because they are not purchased globally in very high volumes they are more costly than ordinary MLCCs.

Plastic dielectrics suffer from dielectric absorption, which means that not all of their stored charge is available instantaneously. Some dielectrics (e.g. Teflon, polycarbonate) are better than others, but they are more costly and the commonplace low-cost polyester dielectric gets progressively worse as frequencies increase above a few MHz. Plastic decaps also tend to have higher ESLs than MLCCs, due to the way they are constructed.

Electrolytic capacitors, including solid tantalum, rely on chemical changes to store their charge, and until recently have been valued for having a higher charge storage density than plastic or ceramic types. Having to wait for chemical changes to happen in them before the charge is released restricts their practical use to frequencies under 1MHz. Electrolytics also tend to have higher ESLs than MLCCs, due to their internal construction.

Recent years have seen significant advancements in MLCCs, with 100nF now available from some suppliers in the very good X7R and/or Z5U dielectrics in the extremely small 0201 package size. The lower internal impedances of MLCCs can enable them to do as good a job of decoupling lower frequencies as electrolytics that have values up to 5 times larger, so a 100nF MLCC can sometimes replace a 470nF electrolytic. The only reasons for using electrolytics these days are decoupling high voltages, or where lowest cost is more important than size, weight, and reliability.

A decap’s ESL is an important contributor to the inductance of the current loop consisting of the decap, the IC it is associated with, and the interconnection between the two – see Section
2.5 and Figure 5C below. It is very important to reduce the inductance of this current loop, and so it is very important to use decaps with low ESLs.

Smaller and/or lower-profile surface-mounted MLCCs tend to have lower ESLs. Standard three-terminal feedthrough capacitors can be used to achieve lower ESL, and X2Y Attenuators are another recent development in low-ESL decaps, and both are discussed in more detail in section 2.10 below.

‘Reversed aspect’ MLCCs have their metallised terminals along their long edges – instead of on their short edges (as is more usual with surface mounted capacitors) and this reduces their ESLs. For example, 0508 and 0306 styles indicate a reversed aspect package (instead of the more usual 0805 and 0603 styles). AVX say that an 0805 MLCC has an ESL of around 1nH, whereas an 0508 has around 400pH and 0306 around 325pH [10]. AVX also offer ‘interdigitated capacitors’ (IDC) and ‘low inductance chip arrays’ (LICA), which offer much lower ESLs than reversed aspect decaps. For example, [10] says that an 0508 IDC has an ESL of under 100pH, whereas LICA (which uses a ball-grid array package style) has under 30pH.

2.5 **Layouts that reduce the size of the current loop**

To obtain the greatest reduction in magnetic and electric field emissions, the area enclosed by the current loop created by the decap and the device it is decoupling must be minimised. Since this series is about advanced EMC techniques in PCBs, this article assumes that a high-integrity 0V plane (at least) is used in the PCB (see [7]). Figure 5C shows the schematic of the current loop that we are concerned with, and Figure 5D shows a suitable layout.
As was mentioned earlier – the complete power current loop between decap and IC is important – and this includes the lead frame, bond wires, and silicon of the IC. Since we often don’t know the path taken by the power current inside the IC, this article ignores it. But when choosing devices or designing FPGAs or ASICs it is important to ensure that the inductance created by its internal power bus does not prevent the PCB designer from decoupling well enough to achieve good EMC performance at the PCB level. Some Ball Grid Arrays (BGAs) have many hundreds of pins dedicated just to 0V and power connections exactly for this purpose. Lo-profile ICs (such as BGAs) and/or ICs which include internal 0V planes, will generally be an aid to PCB decoupling. IC sockets should, in general, not be used because the inductance they add between IC and decap prevents PCB decoupling from being effective for EMC purposes.

The inductance of simple two-dimensional shapes of current loops can easily be calculated using standard equations – but they are not given here because it is much quicker to use on-line calculators generously provided free on the Internet [11]. Real decap-IC current loops are usually three-dimensional, and the inductance of the complex shapes they create can be hard to determine without a field solver (see later). Methods of reducing the inductance of the
decap-IC current loops – and the internal inductance of the discrete decaps – are covered during the rest of this article.

The minimum decap-IC current loop inductance is achieved by choosing a decap with a low value of ESL, and minimising the inductance of the interconnections to its IC (or other device).

In the case of a 0V plane and power trace – the layout that achieves the minimum interconnect inductance is shown by Figure 5D.

The power terminal of the decap shares the same pad as the power pin of the IC, with minimum spacing between IC and the decap. The 0V plane should be the next layer down from the surface layer where the components are mounted, and all components should connect to it using the shortest widest traces (via-in-pad where practical). Closer spacing of the 0V plane to the component side of the PCB will reduce the interconnect inductance further.

To help the decap remove noise from the power bus, it helps if the current from the power supply has to flow across the pad of the decap to get to the IC.

To help with the design of the layout for a decap, Figure 5E shows how the partial inductance of a trace routed over an adjacent 0V plane varies with trace width and spacing from the plane.
Where it is not possible to share the same pad because the decap has to be moved further away from the power pin for some reason, it is best to minimise the decap’s interconnect inductance by employing a small copper area (a small power plane) instead of a trace between the IC and decap as shown by Figure 5F. As before the 0V plane must lie on the layer adjacent to the small power plane, and closer spacing between these two layers will reduce the interconnect inductance.

The reason for specifying the layer that is used for the 0V plane is that the decap’s interconnect inductance is significantly reduced by maximising the mutual inductance
between the 'send' and 'return' currents, by placing them on adjacent layers. Closer spacing of these layers increases their mutual inductance, and this reduces the overall loop inductance. This issue is discussed in more detail in section 3 below.

To help reduce the area of the current loop on PCBs with 0V and power planes – where the IC to be decoupled is closest to its 0V plane layer its decap should be placed close to its power pin(s). But if the IC is closest to the layer on which its power trace or plane is routed, its decap should be placed close to its 0V pin(s).

To help achieve low power bus impedance, some manufacturers embed decaps inside their PCB itself. Some do this by making parallel plate capacitors out of copper areas and small areas of special insulating material with a high dielectric constant. Some others do it by milling an oval hole in the PCB, plating its ends, and soldering a discrete decap inside the hole. These are both expensive and/or problematic techniques that are not recommended for general use.

The reduction of the areas or volumes enclosed by the decaps’ interconnects is important for all types of circuits, not just digital. When decoupling analogue circuits, the basic issues for decoupling are usually stability, rejection of power supply noise, and immunity to EMI.

Opamps used for low-frequency instrumentation and audio circuits usually employ 100nF multilayer ceramic decaps at each power pin, whereas high frequency and RF devices might need to employ 10nF or even 1nF for stability, and might need to employ similar techniques to those described below to maintain a low power bus impedance over a wide range of frequencies.

2.6 Series resonances in decaps

All decaps have ESL which, in combination with the inductance of their decap’s interconnect (see Figure 5C), causes them to behave as a series resonant circuit.
Series resonant circuits have a Self Resonant Frequency (SRF) at which their impedance falls to a minimum (limited only by resistance in the circuit). \( f_{\text{SRF}} = \frac{1}{2\pi \sqrt{L_{\text{TOT}}C}} \), where \( L_{\text{TOT}} \) = the total inductance associated with the decap (the ESL of the capacitor plus the decap’s interconnect inductance, see Figure 5C). \( L_{\text{TOT}} \) in Henries (H) and C in Farads (F) gives \( f_{\text{SRF}} \) in Hz. Above the \( f_{\text{SRF}} \) the decap impedance is simply \( 2\pi f L_{\text{TOT}} \), so it increases with increasing frequency. Figure 5G shows the series resonant behaviour of some example decaps, assuming average 0805 or 0603 decaps with an ESL of around 1nH, plus a good pad pattern (from Figure 4H of [7]) that achieves an \( L_{\text{TOT}} \) of 2nH.

The dotted lines in Figure 5G shows how we might expect an ideal decap’s self-impedance to continually decrease with increasing frequency, assuming no inductance in the current loop at all. But the solid lines show that, at their SRF, real decaps can have an impedance that is lower than that of an ideal capacitor of the same value. Figure 5G also shows that at frequencies above their SRF, decap impedance is totally defined by \( L_{\text{TOT}} \).

Modern ICs switch so quickly that they generate significant levels of emissions at frequencies above 300MHz, and so Figure 5G shows us how very important it is to minimise \( L_{\text{TOT}} \), to try to reduce the power bus impedance at such high frequencies.
The rest of this article includes design techniques to overcome the problem of inductance in power bus decoupling.

2.7 Using ferrites in decoupling

Wherever the impedance of the portion of power bus closest to a device (such as an IC) is not low enough, noisy currents will tend to circulate around the PCB’s whole power bus, including any wires connecting to an off-board DC power supply, and this will increase emissions. Adding a ferrite bead between each power pin and its power supply, as shown by Figures 5H and 5J, can reduce emissions by increasing the RF impedance of the power supply in such a way that more of the noise current remains local to the decap/device combination. As long as the longest dimension of the current loop between the decap and the IC remains smaller than one-quarter of a wavelength (λ), the emissions will then be less than they would be without the ferrite. (λ/4 for 1GHz in FR4 is 37mm.)
The ferrite beads used for this purpose should be RF suppression devices, not inductors wound on ferrite cores, no matter how small. It is often possible to choose specific types of ferrite beads that are more effective than others at the emissions (or immunity) frequencies of concern.

The ferrite bead-decap combination can be thought of as a low-pass filter that helps to keep noisy currents from an IC out of the main power bus. When this technique is used it may be found that only some of the ICs need ferrites in their DC rails — for example: clock generators and clock buffers. It may also be found that some IC cannot use ferrites in their power bus because the resistance is too high (check with the IC manufacturers’ application notes).

However, simply adding a ferrite as shown above will cause the impedance of the power bus as seen by the IC will rise, so it will suffer from higher values of supply noise (rail bounce). With some ICs this can cause functional problems, so ferrite decoupling may require the use of higher values or higher specification decaps (see 2.8, 2.9, 2.10 and section 3 below).

### 2.8 Splitting the decap into two

A decap in combination with the stray impedances of a power bus can be thought of as a filter. A problem with single-capacitor filters is that the current loops associated with the input and
output sides of the filter share a common boundary – the capacitor – enabling the magnetic flux associated with the input loop to couple quite well with output loop (and vice-versa). The resulting mutual inductance between the filter’s input and output circuits reduces the attenuation it achieves in real life.

One way to deal with this problem is described by [12], and was also used in Part 2 of this series [13]. Two decaps are used along a power trace, spaced as far apart as possible – but no further apart than one-tenth of the wavelength in the PCB dielectric at the highest frequency of concern (see Figure 2V of [13]). The wavelength is given in meters by $300/\sqrt{f \cdot k}$ where $f$ is the frequency in MHz and $k$ is the relative dielectric constant of the PCB substrate (the term $\varepsilon_r$ is often used instead of $k$). The $k$ for FR4 is nominally 4.0 at frequencies above 1MHz, so for a top frequency of 300MHz with an FR4 dielectric in the PCB – the maximum spacing between the two decaps would be 50mm.

Providing the component placement and trace routing is done carefully, so as not to compromise the physical segregation achieved between these two loops, the mutual inductance between the input and output current loops is considerably reduced. The restriction of the spacing between the two decaps to $<\lambda/10$ prevents the newly-created current loop between the two decaps from becoming resonant – as this would once again couple the input and output loops very closely. Clearly, this technique could also employ three or more decaps in series along a power trace to get even better noise filtering.

2.9 Using multiple decaps in parallel

Using a number of decaps in parallel is one way of reducing the effect of their ESL. But this only has a significant overall benefit if the inductance of the decap’s interconnect is much smaller than the ESL of a single decap (see section 2.4 and its figures above). Since it can be
difficult to share an IC’s power pin pad with more than one decap, the scheme of Figure 5F is often used with all the decaps to be paralleled sharing the same small power plane.

When \( n \) identical decaps are paralleled the impedance they achieve is reduced. The reduction depends on their layout with respect to one another, but \( 1/n \) times the impedance of a single decap can be achieved. So 10 decaps with the same ESL can be arranged to have 1/10th the impedance of just one decap.

The most obvious way of arranging multiple decaps is to place them in a bank, side-by-side, with all their 0V connections at the same end – but this would not create the impedance reduction required. Since their current flows are in the same orientation, and the devices are close enough to have significant mutual inductance, the reduction in overall impedance is not as much as \( 1/n \). With such a regular layout, the devices should be far apart to minimise their mutual inductance and hence minimise their overall impedance, as shown in Figure 5K.

However, the devices can be placed close together if they are arranged so that the magnetic fluxes, created by the current flowing through their bodies, cancel. Figure 5P below shows an example of this technique with just two decaps. Figure 5K shows how this technique might be applied when using five decaps, but if you are planning on using this technique take care not to infringe Dell Patent #6,337,798.
It is claimed that a bank of X2Y® Attenuators used as decaps (see section 2.10) can be closely spaced together in the same orientation without their mutual inductance compromising their overall effect, but this requires identical and symmetrical locations for the 0V via hole(s) for each device.

At the time of writing there are two conflicting recommendations on the values to use when paralleling decaps – some experts recommend using identical values whilst others recommend using a variety of values. But all of them agree that it is essential to choose decaps with the smallest ESLs and to minimise the inductance in the decaps' interconnections.

Figure 5L shows the effects of using ten identical 10nF decaps – assuming they share the small power plane of a layout similar to Figure 5F and assuming they are laid out optimally to achieve $1/n$ improvement in overall ESL (see Figure 5K).
Using identical types and values of decaps avoids the problems of parallel resonances that occur when decaps with different SRFs are used. Figure 5M shows the sort of thing that happens when three different values of decap are paralleled under the same conditions as Figure 5L. In-between each pair of series resonant frequencies, a parallel resonance with a high impedance appears – not what we wanted.

The effects sketched in Figure 5M are easy to simulate using SPICE with simple models for the decaps that just include their capacitance values and ESLs, and many designers take this to be a good reason for not using different decap values in parallel. But it is possible to use a
number of different values to achieve an overall power bus impedance that may give better overall performance than using identical values. The idea is to spread the series resonances around to get a lower impedance over a wider range, and choose values that are close enough together that the parallel resonances cannot achieve very high impedances. Figure 5N shows an example of such a decoupling scheme using ten decaps with values ranging from 100 to 1nF (assuming they are laid out optimally to achieve 1/n improvement in overall ESL, see Figure 5K). The overall impedance of ten identical 10nF capacitors (from Figure 5L) is shown for comparison.

Figure 5N shows that using closely-spaced values of decaps we can achieve lower impedance over parts of the frequency range (in this example, below 12MHz and from 60 – 150MHz) with the trade-off of a higher impedance over part of the range (12-60MHz). Above about 150MHz the impedance is the same for both sets of parallel capacitors – simply equal to the impedance of 10 off 2nH inductors in parallel. For more on using multiple values of decap to extend the low-impedance frequency range, see [14].

When laying out the decaps for an IC using a variety of decap values, the decaps with the lower capacitance values should be placed closest to the IC’s power pin. It is often remarked
that there is little value in using decaps with values below 1nF, but if their equivalent series resistances (ESRs) are low enough Figure 5N indicates that they may help achieve lower overall impedances at frequencies above 150MHz.

MLCCs with NPO or COG dielectrics tend to self-resonate at higher frequencies, for a given value of capacitance, which makes them more attractive for decoupling. But they have lower ESRs than the X7R and Z5U ceramic dielectrics usually used to pack much more capacitance into small decaps. Lower ESRs mean lower impedances at their SRFs, but the reduction in damping caused by the lower ESR losses makes the parallel resonance peak impedances higher. So in general it is better to avoid COG or NPO dielectrics and choose decaps with ESRs of 10mW or more. When using NPO or COG decaps their low ESRs make it very important to route them to their ICs in a way that achieves the lowest possible loop inductance. This helps reduce the amplitude of their parallel resonance peaks.

**2.10 Other ways to reduce decap ESL**

The ESL of a decap is caused by the flow of current within it. One way of reducing ESL is to place two decaps close together in an orientation such that the magnetic fluxes caused by their internal currents cancel each other out, as shown by Figure 5P (taken from [15], which in turn references [16]). Obviously, this technique can be applied to any number of decaps (see 2.9 above, and Figure 5K) – but if intending to use this technique, take care not to infringe Dell Patent #6,337,798.
Surface-mounted 3-terminal ‘feedthrough’ capacitors [17] and especially ‘X2Y® attenuators’, with one centrally located via (or two symmetrically located vias) to their 0V plane, have lower ESL than a similar size of 2-terminal capacitor. This is due to the magnetic field inside the capacitor being partially cancelled due to there being two current paths in opposite directions for at least part of their path through the body of the devices. The result is a higher SRF, and a lower impedance above the SRF, for a given capacitor value and package size. X2Y® attenuators have a special three-electrode internal structure that achieves better internal magnetic flux cancellation than a normal 3-terminal capacitor.

Figure 5Q shows a the schematic and pad pattern for an X2Y® attenuator when used with both 0V and power planes, plus a graph (from [18]) comparing the impedance of a 470nF X2Y device compared with that achieved by a parallel combination of five ordinary 2-terminal MLCC decaps (150 + 100 + 68 + 47 + 33nF). The graph shows that the single X2Y® has a better-controlled impedance curve and a lower impedance at frequencies above the SRF, implying that (in this example, at least) the X2Y® device and its interconnect achieves an inductance that is less than that of five MLCCs in parallel.
7. References


http://www.compliance-club.com/KeithArmstrongPortfolio


[11] For example the on-line inductance calculators kindly provided by the EMC Laboratory at the University of Missouri-Rolla at http://emcsun.ece.umr.edu/new-induct


I would like to reference all of the articles, papers, application notes and textbooks that back-up the techniques described in this series, but the reference list would take longer to write than this series! However, I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing and his staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand...
out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

Some other useful textbooks are:


Due to the length of this part of Keith's series, we have split it into two and the rest of it will appear in the next issue 56 (January 2005).

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Advanced PCB design and layout for EMC
Part 5 - Decoupling, including buried capacitance technology (Second Part)

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the second part of Keith Armstrong’s article that appeared in Issue 55, EMC & Compliance Journal, November 2004. Due to its length we had to split it between the two issues. This issue contains Section 3 - Decoupling with 0V/Power plane pairs, onwards.

This is the fifth in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. This series will not repeat the basic design information in these articles – it will build upon it.

Like the above articles, this series will not spend much time analysing why these techniques work, they will focus on describing their practical application and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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3. Decoupling with 0V/Power plane pairs

3.1 Introduction to the decoupling benefits of 0V/Power plane pairs

It was mentioned in section 2.5 above that placing 0V and power planes areas on adjacent layers significantly increases the mutual inductance between them. Since the current flows in each plane are equal and opposite, this mutual inductance reduces the decaps’ interconnection inductances, which is a very good thing. Closer spacing between the two planes means higher mutual inductance and lower decap interconnection inductances. Another consequence of having 0V and power planes in close proximity on adjacent PCB layers (known as a 0V/Power plane pair) is that they create a distributed capacitance – and this can be used as an embedded decoupling capacitance to help achieve a low impedance power bus at frequencies up to many GHz.

The use of large power planes to create useful amounts of embedded, distributed decoupling capacitance is the main topic of this section. As far as the propagation of the wanted digital and analogue signals is concerned, a power plane is a copper sheet just like a 0V plane, so all of the general issues about planes, especially when signals are routed near to, or cross, their edges applies in just the same way – and the guidance in [7] (especially its section 4) applies equally to power planes.

Some EMC experts prefer not to use power planes, because if not used carefully the cavity resonances that naturally arise when they are used in combination with another plane can
cause an increase in emissions. This section will show how power planes can easily be used to reliably achieve a net overall EMC benefit.

3.2 The distributed capacitance of a 0V/Power plane pair

It is very difficult to achieve a low power bus impedance above 500MHz using discrete decaps mounted on a PCB, see Figures 5G, 5L, 5M, 5N and 5Q. The best that can be done in this frequency range is to place so many decaps in parallel that their overall inductance gives a low enough impedance.

Intrinsic 0V/Power plane pair capacitance has excellent performance beyond 1GHz due to its extremely low ESL, which makes its SRF very high indeed. In fact, the SRF of a 0V/Power plane pair is so high that it is never an issue of concern. If we were to plot the impedance of 1nF of 0V/Power plane pair capacitance on Figure 5G above, it would follow the dotted line that indicates the impedance-versus-frequency performance of an ideal 1nF capacitor, even if the horizontal axis was extended to 10GHz or more.

\[ C_{\text{plane pair}} = \frac{35}{d} \text{nF per square metre}, \text{ for FR4 (} k = 4 \text{)}, \] where

\[ d = \text{the interplane spacing in millimetres} \]

Thinner interplane spacing increases the capacitance, and a spacing of 50µm (2 thousandths of an inch) achieves 770nF/sq. metre (as used by the ZBC2000 product, see below). Using 2 or more sets of 0V/Power plane pairs in parallel is a simple way to double (or more) the distributed plane pair capacitance available for decoupling.

Figure 5R shows how the low impedance at high frequencies achieved by the 0V/Power plane pair can be used in combination with voltage regulators and discrete decaps to achieve a low power bus impedance over the whole frequency range of concern.
3.3 PCB 0V and power routing with 0V/Power plane pairs

A summary of decap pad patterns for connections to 0V/Power plane pairs with brief comments on their effectiveness was given in Figure 4H of [7]. Some suitable pad patterns for connecting IC 0V and power pins to their respective planes were shown in Figure 4J of [7] and are also described in [19]. Also see Figures 5T and 5U.
Section 2.4 of [7] listed some valuable layout rules for connecting components to planes. When they are applied to the decaps and 0V and power pins of ICs, they help minimise the decaps’ interconnection inductances and allow the charge stored in the decaps to be delivered to the ICs more quickly.

Because we are trying to take advantage of the 0V/Power plane pair’s capacitance at frequencies above 500MHz, the inductance of the connection between IC and plane must be very low indeed. So it is very important indeed to connect an IC’s 0V and power pins immediately to their respective planes, as shown in Figures 5T and 5U and section 2.4 of [7].
The decaps should also be connected directly to their planes, because the interconnection inductance of the planes is much less than any trace. Via-in-pad is preferred, which can always be done for wave-soldered THP PCBs, and which some PCB assemblers can achieve using reflow-soldered THP PCBs. Via-in-pad is normal when using HDI (‘microvia’) PCB technology, see section 5 of [7] and Part 7 of this series.

The partial inductance of the length of the via holes that actually carries current between a component and a plane becomes very significant at frequencies above a few hundred MHz. (A physics purist would say that the problem was really the current loop area caused by the spacing between the component and the plane). So, to provide good power bus impedance up to and beyond 1GHz, we need to stack-up our PCBs so that they provide 0V/Power plane pairs as close to the surface-mounted components as possible, minimising the length of the via holes that must carry current.

As was mentioned in [7], the bad influence of via holes’ current-carrying lengths can be reduced by placing vias carrying equal and opposite currents very close together. Also, multiple parallel vias can be used for any current path but they must be far apart (compared with their current-carrying length) for this to be very effective. Vias with larger diameters have lower partial inductances, but (when using THP and not HDI PCB construction) larger diameter power vias make larger holes in the 0V plane and compromise its performance (see [7]), so multiple small vias are generally preferred.

Some designers have in the past preferred to ‘keep the noise out of the planes’ by using traces to connect between decaps and ICs, then connecting the decaps to the planes. The purpose of this is to avoid exciting the 0V/Power plane pair’s cavity resonances – but it is not an optimum solution because it increases the inductances in the decaps’ interconnections and
prevents the full benefits of the 0V/Power plane pair’s distributed capacitance from being used.

There is no problem with noisy currents in planes providing the planes used for the power bus maintain a low impedance over all the frequencies of concern – by designing them to avoid or damp their cavity resonances. Later in this article I will describe practical low-cost methods that will achieve 0V/Power plane-based power busses that have no significant resonances over the frequency range of concern, improving the EMC (and functional) performance of the circuits on the PCB.

3.4 Defeating parallel decap resonances when using 0V/power plane pairs

Section 2 above suggested using small power plane areas to help reduce decaps’ interconnection inductance, when using multiple capacitors in parallel to reduce power bus impedance at the IC. When a power plane is extended in area to embrace all of the ICs its power bus services, and all of their decaps, we find we now have a much higher number of decaps in parallel.

When using different values of decap, as described in section 2.9 above, the use of large power planes provides so many series resonances spaced so closely together that the high impedances caused by parallel resonances are very low [14].

To take advantage of this, and also to help prevent cavity resonances in the 0V/Power plane pair (see below) it is recommended to place decaps all over a power plane, not just near to the ICs, no further apart than 25mm, and to minimise each decap’s overall inductance by careful layout (see Figure 4H of [7]) and careful choice of decap components. One way of looking at this approach is to say that it creates alternative low-impedance current paths nearby each high-impedance (parallel resonating) current path – so the IC’s power bus currents always can
always find a low-impedance path. Figure 5V below shows an example of exactly this from UMR.

Figure 5V shows the result of some experiments at the University of Missouri-Rolla [19]. It shows that increasing the number of 10nF decaps from 4 to 64 has significantly reduced the amplitudes of most of the parallel resonances. However, the highest-frequency resonance (caused by the 0V/Power plane capacitance with its very small ESR) was not been reduced in amplitude – it was moved to a higher frequency.

![Figure 5V](image)

An interesting observation is that when the spacing between the 0V and power planes in the pair is less than 250µm (10 thousands of an inch) the placement of the decaps with respect to their ICs becomes less critical, easing PCB layout [20].

Although Figure 5V came from an experiment that used large number of decaps all (but one) of the same value (10nF) – page 159 of [19] tells us that each capacitor had a different interconnect inductance associated with it (between 1 and 8nH). So instead of having very similar SRFs, these decaps would have had different SRFs, just as they would have had if their values were different and their interconnect inductances the same. One possible conclusion from this is that the impedance between 200MHz and the last (large) resonance
would probably have been less if all of the devices had used different values but their layouts all achieved the lowest possible interconnect inductance.

3.5 ‘Cavity resonances’ in 0V/power plane pairs

Cavity resonance between 0V and power plane pairs was discussed in Part 4 of this series [7], but the implications and design issues for decoupling were left to this Part.

Achieving a low plane impedance at every frequency can be made difficult by cavity resonances (sometimes called ‘parallel plate’ resonances) – where the 0V/power plane pairs behave like unterminated transmission lines.

The natural resonant frequencies for a rectangular plane pair filled with a material with a relative dielectric constant of $k$ are given by: $f_{\text{RES}} = (150/\sqrt{k}) \times \sqrt{(l/L)^2 + (m/W)^2}$

This formula gives $f_{\text{RES}}$ in MHz if $L$ and $W$ (the plane pairs’ length and width) are in metres. $l$ and $m$ are integers (0, 1, 2, 3 etc.) and correspond to the various modes of resonance, but it is usually only the first (lowest) resonant frequency we are most concerned with. For FR4 material ($k$ nominally 4.0 at >1MHz) this is easily found from: $f = 75/D$, where $D$ is the plane’s longest diagonal dimension ($D$ in metres gives the frequency $f$ in MHz, $D$ in millimetres gives it in GHz).

For non-rectangular planes that are not simple shapes, it will usually be necessary to determine their resonant frequencies by computer simulation using field solvers, or measurement of a test PCB. But their lowest resonant frequency will still be easily estimated as $75/D$ MHz for FR4, where $D$ is the plane’s longest dimension, in metres.

It is important to understand that in real life the bare-board plane resonances are significantly modified in amplitude and frequency by the presence of the electronic components and the numbers, values, types, and locations of the decaps. So the above simple analyses are only
of use during a design process, and do not predict the actual resonances in a real-life power bus on a fully assembled PCB.

One way to reduce the worst effects of cavity resonances is by careful design of the planes’ shapes, and this was mentioned in [7]. This will have little effect on the lowest frequency (governed simply by the longest dimension) but it may have a useful effect on some of the higher frequency resonances.

Where the length \( L \) of a rectangular plane is an integer or other simple multiple of its width \( W \), such as 1, 1.5 or 2, the resonant frequencies of the length and width directions will coincide at some frequencies, causing higher-Q peaks (more intense resonances) at those frequencies. Murphy’s law tells us that when the clock frequency is changed just before product launch, one or more of the new harmonic frequencies will just happen to coincide with one of these more intense resonances, causing problems for EMC compliance at a time when it is very costly and time-consuming to make any changes and delays cannot be tolerated.

So it is best to avoid simple regular power plane shapes such as squares and circles, and also avoid simple \( L:W \) ratios. Ideally, choose an irrational number for the ratio of length to width of a rectangular plane. There is an infinite number of irrational numbers to choose from, but the ‘Golden Mean’ (1.618…etc… call it 1.62) gives a pleasing appearance (as Renaissance artists and ancient Greek architects knew). Thin planes should always be avoided, meaning that their \( L:W \) ratio should never be larger than 3 (or smaller than 0.33). It may also help to have non-parallel plane edges, and to avoid regular shapes such as rectangles.

Closer plane-pair spacing increases the losses in their cavity, decreasing its Q and making the cavity resonances less peaky. Closer spacing also reduces their fringing fields, reducing ‘edge-fired’ emissions. This very powerful EMC technique requires plane spacings no greater
3.6 Bonding planes with decaps to increase resonant frequencies

When cavity resonances between pairs of 0V planes was discussed in [7], it was shown that bonding them very frequently together with via holes increased the frequency at which their first resonance occurred. The idea was to ‘push’ the first resonance to such a high frequency that it was no longer a concern for EMC. The effectiveness of the technique is limited by the partial inductance of the via holes.

The equivalent technique for 0V/Power plane pairs is to ‘RF bond’ them together using decaps at very frequent intervals, *all over* the power plane’s area, even where there are no ICs or other active devices. The maximum distance between any two decaps should be less than $\lambda/4$ (in FR4) at the highest frequency of concern, and for 1GHz this would mean a distance of 37mm. Multiple decaps all over a power plane were recommended earlier, for a different reason, so this technique has at least two different benefits for decoupling.

The effectiveness of the technique is limited by the ESLs of the decaps and the partial inductances of their pad patterns and via holes. So there seems little point in going below 25mm decap spacing whilst using THP PCBs.

When not using a 0V/Power plane spacing of 50µm or less (see later), a bare-board power plane should not have dimensions larger than $\lambda/8$ (in air, $\lambda/4$ in FR4) to avoid cavity resonances at the highest frequency of concern. For example, to have no cavity resonances below 600MHz, the longest dimension (diagonal) of the power plane should be no longer than 63mm.

Sprinkling decaps all over this 0V/Power plane pair whilst carefully minimising their ESLs and interconnect inductances, as recommended above, will $\lambda/4$ in FR4 whilst allow the use of
power plane areas with diagonals larger than still avoiding cavity resonances. But it is not easy to calculate the maximum size of the power plane that will not suffer from cavity resonances in such a design – experiments are generally needed, if a suitable simulator (see later) is not available.

3.7 Power plane islands fed by π filters

A common technique to prevent cavity resonances from increasing emissions from the power bus of a PCB is to use many small power plane ‘islands’ instead of one large one. The area of the power plane ‘island’ should be chosen so that (in combination with its paralleled decaps, see section 3.6 above) its lowest resonant frequency is above the highest frequency of concern for EMC. This smaller area reduces the size of the embedded 0V/power plane pair capacitance available to devices associated with each island – so a trade-off may be required. Another reason for using power plane islands is to isolate a noisy or sensitive IC from others on the PCB, a useful circuit segregation technique (see [21]).

All of the plane islands associated with a power bus will be connected by traces, and this creates structures with quite low resonant frequencies that can couple noise from one island to another. So it is very important to decouple each island from the others by providing the DC power to each island through its own π filters are easily created by connecting to each plane via a soft ferrite RF suppresser bead and ensuring that a decap is located near each end of each bead.
There is little benefit in making the gap between two power plane islands larger than twice the spacing between the layer carrying the power plane islands and the 0V plane layer. If two islands resonate at the same frequency they will suffer very effective coupling across a gap of any size – even from one side of the PCB to another – so either ensure the island’s resonant frequencies are higher than the highest frequency of concern, or else don’t use islands which have the same cavity resonant frequencies. For more on power plane islands, read [22] and [23].

3.8 Damping cavity resonance peaks

IC loads and transmission-line terminations help to dampen 0V/Power plane resonances, so their peak impedances are often not as high as bare-board simulations or tests would suggest. Adding resistors of 1 - 10Ω between two planes adds more losses so also helps damp resonances, but for a 0V/Power plane pair they need to be in series with a capacitor so as not to consume too much DC power. At least one manufacturer offers decaps with an internal series resistance for just this purpose.

There usually only needs to be a few damping resistors spread around a PCB, ideally placed at resonant ‘hot-spots’ where the voltage fluctuations between the 0V and power planes is the
highest. The locations of the hot spots may be able to be simulated (see later) or measured – if 0V/Power probing points have been provided at many locations.

In the case of half-wave resonances, such as the first three (lowest frequency) resonances, the hot spots only appear at the power plane corners or along their edges. This observation leads to the technique known as dissipative edge termination, which applies series resistor-capacitor decaps around the perimeter of a power plane [24]. [25] claims that dissipative edge termination is better than the 20-H technique (see below) when the power plane is not ‘shielded’ by extended 0V planes on both sides.

Loading the PCB’s dielectric with particles of ferrite absorber also helps dampen resonant peaks (see section 2.9 of [7]), and may well reduce emissions in other ways. But this is not yet a common method, because the ferrite particles increase the wear on the PCB punching and drilling tools. Maybe when laser-drilled HDI PCB technology (see section 5 of [7], and Part 7 of this series) becomes commonplace, ferrite-loaded substrates will become more attractive.

### 3.9 The spreading inductance of planes

So far in this series planes and 0V/Power plane pairs have been described as if any two points on their surfaces, that were the same distance apart, had the same low impedance between them. But this is not the case – what is called their ‘spreading inductance’ increases the inductance between points placed near to edges, or (worse still) near corners.

This is one of the reasons for the recommendations in earlier parts of this series ([7] and [21]) that planes should extend well beyond all of the devices and traces they are associated with.

Figure 5X gives an idea of the scale of this issue. As this figure shows, spreading inductance has less effect when the planes are closer together – another good reason for using very close 0V/Power plane spacing.
3.10 The 20-H rule

Applying the “20-H Rule” means ensuring that the power plane is cut-back from the edge of the 0V plane by a distance equivalent to at least 20 times the spacing between the planes. It is described in Mark Montrose’s books and is often called upon as a means of reducing the edge-fired emissions from a 0V/Power plane structure. But the 20-H rule only provides significant benefits under certain specific conditions, as described in [25]…

- The rise/fall times of the current fluctuations in the power bus are less than 1ns
- The power plane is on an internal layer of the PCB and has a 0V plane on both sides, each of these 0V planes extending beyond the power plane by a distance that is equivalent to at least 20 times their spacing from the power plane
- The power bus structure is not resonant at any frequencies of concern
- The number of layers in the PCB is 8 or more.

Other techniques described in this series either help the 20-H method to work correctly, or eliminate the need for it.

3.11 Taking advantage of decap series resonances

Some manufacturers put lots of sites for decouplers all over their PCBs (as well as very close to IC power pins). Then, whilst testing emissions, they add decaps with values that have the
greatest effect on the lowest frequency at which the emissions are too high. Next, they choose
decaps values which suit the 2nd lowest problem frequency – then the 3rd problem frequency,
4th, 5th, etc. They are using the decaps’ SRFs to minimise emissions.
This is a clever way of using the SRF to best effect, but is not generally recommended
because it is very sensitive to layout changes, and also sensitive to subtle changes in the
capacitors themselves that may not be under the control of the manufacturer.

3.12 Decap walls

The use of power plane islands and π filtering for segregating areas of circuit from each other
has already been described (section 3.7). Decap walls is a technique that can be used to
reduce the noise that passes from one circuit area to another when they share the same
power plane.

Quite simply, the area of circuitry to be protected (or protected from) other circuit areas is
completely surrounded by decaps, making a ‘decap wall’ around it. The spacings between the
decaps must be small, and their ESLs and interconnect inductances must be low. It is not as
effective as using power plane islands, but it may be a useful technique in some situations.

An extension of this technique is to try to reduce emissions from a power plane’s edges by
placing a row of decaps around its perimeter. Instead of damping the cavity resonance – as
dissipative edge termination tries to do (see section 3.8 above) – this technique tries to create
a low impedance around the perimeter so that voltage differences are reduced and the
emitted E-field is therefore also reduced.

3.13 Other 0V/Power plane pair techniques to reduce emissions

When a plane pair resonates, its electric field emissions are launched from its perimeter, due
to the voltage differences between the two planes at their edges. If all else remains the same
– reducing the spacing of the planes reduces the Volts/metre at the plane pair edge and
therefore reduces the intensity of the electric fields that are launched [26]. The relationship is linear – halving the plane pair spacing reduces the emissions by 6dB.

As shown elsewhere in this article, reducing the plane pair spacing has a number of other beneficial effects for decoupling for EMC performance – reducing the decaps’ interconnection inductances and increasing the amount of distributed capacitance.

Wrapping the power plane with 0V planes on both sides also helps reduce emissions from a cavity-resonating plane pair [26]. This technique employs the perimeter guard ring technique described in section 2.10 of [7], extending the 0V guard traces as far as possible towards the centre of the PCB. In the limit, the board is completely covered with 0V plane on both sides.

Clearly, since there are components mounted on at least one side of the PCB it is impossible to completely shield a PCB without using PCB-mounted shielding cans, as described in section 6 of [7].

Another technique is simply to ensure that the no clock harmonics coincide with the resonant frequencies of the 0V/Power plane cavity (or cavities, when multiple power plane islands are used).

3.14 The buried capacitance technique

The most common PCB buried capacitance technique used to be called Zycon Buried Capacitance (ZBC), which has been used for a several years by a number of computer, cellphone and other manufacturers. Each 0V or power plane in the PCB is converted into a pair of 0V/power planes separated by very thin layer of dielectric. Zycon originally invented the technique, Hadco Corp. then bought them, and Hadco was in turn bought by Sanmina-SCI [27].

Sanmina-SCI offer two products: ZBC1000 and ZBC2000. ZBC1000 uses a ‘core’ consisting of two copper layers separated by 1 thousandth of an inch of FR4, and achieves 900pF/sq.
inch (in metric units this corresponds to a thickness of approximately 25µm that achieves 140pF/sq. cm). ZBC2000 uses 2 thousandth of an inch of FR4, and achieves 500pF/sq. inch (in metric units this corresponds to a thickness of approximately 51µm that achieves 77.5pF/sq. cm). It seems that only ZBC2000 is currently used in volume.

Using these products requires no modifications to the PCB layout or its Gerber files by the PCB designer – the bare-board PCB manufacturer simply replaces each 0V or power plane on the PCB with a core of ZBC1000 or 2000, one side being connected to the 0V and the other to the power. Where an original PCB had a single 0V and a single power plane, the result of adding two layers of ZBC2000 is a distributed capacitance of 1000pF/sq. inch (150pF/sq. cm) – considered to be the minimum required to provide good decoupling at frequencies above 500MHz [28].

Figure 5Y shows the stack-up of a 6 layer board with an equally-spaced stack-up and (originally) no embedded 0V/Power plane capacitance. Such PCBs were very common in the 1990’s but when fitted with present day ICs with their faster switching edges they will probably now have poor EMC performance due to their high-impedance power busses. Replacing each plane with a closely-spaced pair of planes, such as ZBC2000, will dramatically reduce their power bus impedance and reduce emissions up to at least 1GHz.
The stack-up shown in Figure 5Y is not ideal for EMC. For example it can be improved by moving each of the two new 0V/Power plane pairs closer to the components on either face of the PCB, to reduce the length of the via holes that carry power bus currents. This issue is explored in more detail in Part 7 of this series.

The use of a 2 thou thick core of FR4 to provide buried capacitance in a PCB is patented, so the only legal way to use this exact technique is for a PCB manufacturer to purchase the ZBC materials from Sanmina-SCI. Although the materials themselves are not very expensive, a license fee has to be paid and this increases the cost. Despite this the net result on the cost of the PCB can be neutral, or even negative, due to the elimination of most/all decaps (apart from ‘bulk’ decaps) and consequent reduction in the area of PCB required for the circuit. The improvement of production yield and reliability in the field, caused by the reduction in the number of components, also helps make a financial case for using ZBC products.

However, it may be possible to avoid infringing the patents when creating your own buried capacitance using a core with a different thickness, or by using 50µm pre-preg layers instead of a 50µm core – but it may be best to check with a patent lawyer first. With such small thicknesses of FR4 the quality of the materials and the accuracy and cleanliness with which
they are handled is very important if yields are to be kept high, so if you intend to do follow this route you should probably avoid choosing your PCB manufacturer solely on the basis of the lowest price tendered.

ZBC was originally developed to reduce the number of components on a PCB and thereby reduce size and improve yield and reliability (since there are fewer solder joints to fail). Hadco have said in the past that their users claim ZBC routinely improves their EMC emissions by between 6 and 16dB. But to get the best EMC performance from buried capacitance it should provide enough capacitance to avoid any use of discrete decaps (other than ‘bulk’ capacitance, typically 4.7µF or more) – to avoid the creation of peaks in the power bus impedance due to their parallel resonances.

Unfortunately, 150pF/sq. cm (1000pF/sq. inch) may not be enough to provide good decoupling below 500MHz, depending on the transient current demands of the ICs and other devices. So to able to eliminate all discrete decaps, and hence eliminate their parallel resonances, we may need to use a material with a higher ‘k’ value than FR4.

A great deal of research and development is going on at the moment in the area of buried capacitance, and the alternatives to FR4 that are being developed include...

- EmCap® (Samnina) ceramic powder filled epoxy, k = 36
- Hi-K™ (Dupont) ceramic powder filled polyimide, k = 12
- C-Ply (3M) ceramic powder filled epoxy, k = 21, 5.5nF/sq. inch (850pF/sq. cm)
- FaradFlex™ (Oak-Mitsui Technologies) modified FR4, k = 4, with 12, 16 and 24µm thicknesses, also investigating different materials with higher k that can give up to 40nF/sq. in (6nF/sq. cm).
- Ceramic powder with no binding agent (Fujitsu) k = 400, 300nF/sq. cm [30]

Using a high-k dielectric reduces the propagation velocity for the plane pair, lowering their ‘cavity resonance’ frequencies – not what we really wanted – and causing more resonant peaks to arise in a given frequency range – also not what we really wanted. But closer spacing increases the losses in the cavity, reducing its ‘Q factor’ and reducing the peak amplitudes of
the resonances – especially with spacings of 50µm (2 thou) or less. Figure 5Z shows the sort of effects on the power bus impedance of reducing plane pair’s spacing and increasing the k of the dielectric between them.

Tests using C-Ply with a thickness of 5µm (0.2 thousandths of an inch) found a Q of 1 in the 0V/Power plane cavity, meaning critical damping – no resonances at all. Since its k was 21, such a thin layer achieved 4nF/sq.cm, giving much higher-performance decoupling than could ever be achieved on a practical PCB using discrete components.

With such thin dielectric (insulating) layers concern naturally arises about breakdown voltages, so it is interesting to note that ZBC1000 is rated for >2500Vdc and is tested at 250Vdc, whilst ZBC2000 is tested at 500Vdc. Tests on a sample PCB made with 10µm thick ‘Faradflex’ found that it withstood 500V. The most likely concerns for voltage withstand with such thin layers concern cleanliness in the PCB manufacturing process and (when using pre-preg layers instead of cores) the accuracy of the alignment of the layers.

It was recently claimed that techniques that achieve 50nF/sq. cm will soon be commercialised, and Fujitsu say that their new ceramic powder technique [29] should cost 40% less than ceramic/polymer composite coatings. So it seems likely that the use of buried capacitance will
soon eliminate the use of discrete decouplers (below 4.7µF), using spacings of 25µm (1 thou) or less, and high k. In such PCBs, ‘parallel decoupler’ resonances will only tend to occur below 10MHz, and at such frequencies most sizes of PCBs are very inefficient radiators. For more on embedded capacitance see [30] and [31].

4. Field solvers for power bus impedance simulations

Part 1 of this series showed, it is very important for commercial success to get to market very quickly, and this implies that the EMC needs to be correct-by-design. But the above shows that decoupling modern ICs is an inexact science, the available components are inadequate (or costly), and the result is that two or more PCB iterations (re-spins) may be required to achieve the desired EMC performance at low cost. It would be wonderful if we could simulate the decoupling of our PCB, from an EMC point of view, so as to get the design right in the virtual world before laying out an actual PCB.

Computer-based simulators using field-solving techniques that simplify Maxwell’s equations have always been able to be used for calculations of power bus impedance, but they have usually required a lot of expertise on the part of their operator, very powerful computers, and their results did not always correspond with real-life behaviour of the simulated PCB assembly.

But developments in EMC simulators are proceeding apace, and user-friendly simulators that run on standard PCs and give reliable answers cannot now be far away. At the IEEE International EMC Symposium in Santa Clara, California, this year a company called EMS-PLUS was advertising what it claimed was an inexpensive simulator for real-world power bus impedances, called EZ-PowerPlane, which it said was easy to use. Another product that claims to help design PCB decoupling is called EMI Stream, from ScanCAD International.

Neither of these products claim to calculate the emissions from the simulated PCB at a
10 metre distance, but anything that helps achieve good decoupling and the avoidance of high-impedance resonances that are close in the frequency spectrum to the expected problem frequencies, must be of help in reducing time-to-market.

5. EMC-competent QA, change control, cost-reduction

See section 8 of Part 3 [32] for a discussion of this important issue.

6. Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques - but in real-life there are a great many design trade-offs (compromises) to be made, and this is where the circuit and PCB designers really earn their keep.

Designers are often put under cost or time pressure by managers who don’t understand the technical trade-offs, and so don’t understand that their actions could have the opposite effect to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of this series [6], plus the final section of part 2 [13].

7. References


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[11] For example the on-line inductance calculators kindly provided by the EMC Laboratory at the University of Missouri-Rolla at http://emcsun.ece.umr.edu/new-induct


[27] Sanmina webpage on PCB fabrication including brochure on Hadco buried capacitance and a licensee list: http://www.sanmina-sci.com/Solutions/pcb_fab.html


I would like to reference all of the articles, papers, application notes and textbooks that back-up the techniques described in this series, but the reference list would take longer to write than this series! However, I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing and his staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National
Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

Some other useful textbooks are:


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Advanced PCB design and layout for EMC
Part 6 - Transmission lines (and any traces carrying high-speed signals or noises)

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the sixth in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm chip processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues

A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC.

Like the above articles, this series will not spend much time analysing why these techniques work, it will focus on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1 Matched transmission lines on PCBs

1.1 Introduction

Matched transmission lines allow digital and analogue signals to be interconnected over long distances without excessively distorting their waveforms, closing their eye patterns, causing significant emissions, or suffering from poor immunity. Modern electronic products, especially those using digital processing or wireless technologies, would find it impossible to even function without the use of matched transmission lines.

A matched transmission line is a conductor that maintains a fixed ‘characteristic impedance’ – which we call $Z_0$ – from its source to its load, and then its source and/or load ends are terminated (matched) in a resistance having a numerical value equal to $Z_0$. More than thirty different types of transmission line can easily be created on a PCB simply by controlling trace geometry, and some of them are shown in Figure 6A.

PCB transmission lines can easily be extended off a PCB, or between PCBs, using ‘controlled-impedance’ connectors and cables. Controlled-impedance connectors and cables
Transmission line techniques can be used in PCB design to achieve signal integrity (SI) so that the assembled board functions correctly. They can also be used to improve the EMC of a PCB, helping to reduce products' costs of manufacture.

Cost of product manufacture is reduced because improving a PCB's EMC performance reduces the specifications for shielding and filtering at the next higher level of assembly – where the cost of achieving the same EMC performance is typically 10 times higher. The financial and commercial benefits associated with achieving good EMC performance from the PCB itself were discussed in some detail in [6] and will not be repeated here.

There is a very great deal of information on using transmission line techniques in PCBs available in textbooks, articles, papers and presentations – but most of it concerns signal integrity (SI), not EMC. Also, most of the computer-aided tools for helping with transmission line design are also concerned with SI and not EMC.

However, all this SI information is helpful for EMC because high-speed or high-frequency SI issues are simply a subset of EMC, for the reasons described in [7]. Designing a PCB for good EMC automatically achieves excellent SI, so we can turn this around and use SI design techniques and tools but set much tougher SI specifications. For example: if we could accept a signal overshoot of (say) 30% for SI reasons, we would achieve better EMC at the level of the PCB assembly by ensuring that the maximum overshoot is, say 10%. Less than 10% overshoot would give even better EMC, but below 3% it becomes hard to say whether a lower specification would be worthwhile.
The only high-frequency SI issue that might not always correlate with good EMC design is crosstalk between traces and devices in the same area of a PCB. However, the segregation techniques described in [8] will reduce crosstalk between different areas (zones) of a PCB and thus contribute to SI.

Some of the design techniques described in this article (e.g. on changing PCB layers) can be used to improve the EMC of any traces, even those that are not matched transmission lines. There is a great deal of mathematics and theory associated with transmission-line design, and designing transmission lines often runs up against real-world constraints so that the resulting design may not be ideal for SI. SI issues (including crosstalk) are not discussed in any detail here, as they are very adequately covered in a number of good textbooks and relevant standards (see the lists at the end, and [12]).

The usual discussion of EMC aspects of transmission lines focuses on their emissions, but it is important to understand that anything that allows some of the wanted signal to escape as electromagnetic emissions represents an ‘accidental antenna’ – and these antennas will also pick up electromagnetic fields in their environment and convert them into noise signals in their circuits, causing immunity problems. The ‘principle of reciprocity’ is usually invoked here – but without going into theory we can simply note that any circuit that has excessive emissions at frequencies related to its wanted signals will also tend to be susceptible to external electromagnetic fields at those frequencies. So, by reducing emissions by careful PCB layout, we also improve immunity and reduce the amount of space and cost required by filtering and shielding.

1.2 Propagation velocity, $V$ and characteristic impedance, $Z_0$

The dielectric constant of ($\varepsilon_R$) of the glass-fibre FR4 material used in typical PCBs is around 4.2 at frequencies between 1MHz and 1GHz. Another common glass-fibre PCB material is
G-10, which has an εR of about 5.0. This article will focus on FR4, but apart from the differences in εR it applies equally well to G-10 and similar materials. The ceramic material used in some hybrid circuit devices and PCBs has a εR of about 10, and most homogenous plastics and resins have an εR between 2 and 3.

Every conductor in the real world has inductance \( L \) and capacitance \( C \) per unit length. These parameters depend on the conductor’s shape and its geometry with respect to the conductor(s) carrying its return current. They also depend on the relative permeability \( \mu_R \) and the εR of the materials associated with the conductor (in the case of a typical PCB trace: copper, tin/lead alloy, FR4, solder resist and air) and on its proximity of other conductors and insulators. In PCB design the expression εr is usually replaced with \( k \) – so that is what will be used in the rest of this article when referring to PCB substrate materials.

The \( L \) and \( C \) per unit length of a conductor have two effects on the electrical signals and noises it carries –

- they control their velocity of propagation \( (V) \): \( V = \frac{1}{\sqrt{LC}} \)
- and they determine their characteristic impedance \( (Z_0) \) – the ratio of the voltage to the current in the conductor: \( Z_0 = \sqrt{\frac{L}{C}} \)

It is important to remember that the \( L \) and \( C \) parameters above are ‘per unit length’, and that the unit length employed must be very much smaller than the wavelength \( (\lambda) \) at the highest frequency of concern for EMC. It is usually more meaningful for digital design to say instead that the unit length employed in analysing \( V \) and \( Z_0 \) must be very much smaller than \( V \pi \tau_r \), where \( \tau_r \) is the actual rise time of the signal (use the actual fall time \( \tau_f \) instead if it is shorter).

Normal PCB traces have \( L \) and \( C \) values that vary from section to section along their length, and even within a section. Consequently their \( V \) and \( Z_0 \) vary along the length of the trace.
Variations in $V$ can cause skew problems, and increase emissions from differential signals (see later). Traces used as transmission lines must maintain a fixed value of $Z_0$ from their start to their finish, and more than thirty different types of transmission line can easily be created on a PCB simply by controlling trace geometry (see Figure 6A).

All discrete components have inductance and capacitance, and when these are connected to a trace they alter its $V$ and $Z_0$ at that point. So circuit details are also important when designing matched transmission lines.

1.3 The effects of impedance discontinuities

Changes in $Z_0$ and errors in the line matching resistors reflect the leading and trailing edges of digital signals or transient noises, and they also reflect RF sinewave analogue signals and noises. The greater the impedance error – the greater the percentage of the signal reflected. We can calculate the ‘coefficient of reflection’ at an impedance error as: $(Z_1 - Z_0)/(Z_1 + Z_0)$, where $Z_1$ is the characteristic impedance of the discontinuity.

Reflection coefficients can take any value between +1 and −1. When $Z_1$ is larger than $Z_0$ the reflection coefficient has a positive value, which means that the reflected proportion of the signal adds to the original signal level, on that part of the line. So a voltage step of 2V hitting an impedance discontinuity with a reflection coefficient of +0.5 would result in a step-up to 3V passing backwards along the signal’s previous path.

When $Z_1$ is smaller than $Z_0$ the reflection coefficient has a negative value, which means that the reflected proportion of the signal subtracts from the original signal level, on that part of the line. So a voltage step of 2V hitting an impedance discontinuity with a reflection coefficient of −0.5 would result in a step-down to 1V passing backwards along the signal’s previous path.

In the case of the line terminating resistors, we replace $Z_1$ in the above equation with $Z_S$, the impedance at the signal’s source to find the for reflection coefficient at the trace’s driven end.
And for the other end of the trace (receiver) we replace \(Z_1\) with \(Z_L\), the impedance of the load (receiver) to find the reflection coefficient at the trace’s load end.

When a PCB trace is not intentionally designed as a matched transmission line, reflections can occur at many places: at either or both of its ends, and along its length. Reflected signals and noises will flash backwards and forwards along the trace (or parts of it) many times before eventually subsiding to a steady state. This effect is easily seen with a very fast oscilloscope, or with a very long trace. Figure 6B shows two examples where a trace has a constant characteristic impedance along its length, but is not correctly terminated with matched values of resistors at either of its ends.

Waveforms like the upper one in Figure 6B are obviously capable of crossing a logic threshold twice, which can lead to the misbehaviour of digital circuits. Avoiding this is one of the key goals of SI design.

Notice that Figure 6B shows the waveforms experienced at the ends of the trace. Different waveforms will be experienced by devices positioned along the trace, between its two ends. The ‘rules’ used to draw Figure 6B are given in [13] and the various textbooks, standards and
other references listed at the end, and they can also be adapted to determine the waveforms at any point along a trace.

Reflections make mismatched conductors act as ‘accidental antennas’ and emit a proportion of their reflected signals into the air as radiated emissions, which is bad for EMC. If the distance between a pair of impedance discontinuities happens to be the same (or near to) a quarter or half of the wavelength of a significant spectral component of the signal or noise – that part of the conductor will resonate, making it a much more efficient accidental antenna, as shown by Figures 6C and 6D. Whether the resonances occur at quarter or half wavelengths depends on the type of the discontinuities at each end.

![Figure 6C](image)

**Figure 6C**
The ‘accidental antenna effect’ of an idealised 200mm (8 inch) PCB trace
(On FR4, no reference plane, very low impedance drive, very high impedance load)

Antenna efficiency in dB

-60  -40  -20  0  λ/4  3λ/4  5λ/4  Etc...

6dB/octave region

Resonant region

The typical antenna efficiency of a correctly matched PCB transmission line that uses ‘microstrip’ construction, for comparison

MHz

20  50  100  200  500  1,000  2,000  λ/2
The accidental antenna efficiency of a real trace, and the real-life drive and load waveforms, will not be exactly the same as the idealised sketches in Figures 6C and 6D. These sketches are simply trying to communicate how ignoring matched transmission line design can lead to excessive emissions. However, it is surprising how many clock waveforms end up looking very much like the red curve in Figure 6D.

When traces act as accidental antennas, this is not only bad because of their unwanted emissions, it is also bad for immunity because they are more effective at picking up electromagnetic fields from their environment and converting them into conducted noises in the traces.

1.4 The effects of keeping $Z_0$ constant

Keeping $Z_0$ constant along a conductor from the source to the load, and terminating the ends of the conductor in matched resistances, prevents reflections and communicates almost 100% of the signal. This is very good for SI and also very good for EMC. As was said above, many modern products that employ digital processing and/or wireless technologies could not even work without matched transmission lines, much less meet their EMC requirements for reliability and compliance.
Where a signal needs to pass from one transmission line to another with a different characteristic impedance, this may be achieved by the use of an impedance-matching transformer which does not cause a significant impedance discontinuity. The frequency response of such transformers can cover three decades but cannot extend down to d.c., so they are not suitable for all applications.

1.5 Time Domain Reflectometry (TDR)

The PCB structure and its trace routing is becoming a great problem for impedance matching as digital signal or noise rise and fall times decrease below about 150ps, or as analogue signals or noise increase above 2GHz. For such signals or noises PCB trace routing structures that used to be able to be ignored, such as via holes, now need to be treated as impedance discontinuities along a transmission line [9].

An important tool for simulating and visualising this problem, and for measuring real PCBs to discover if they have been designed correctly or to trace errors, is Time Domain Reflectometry (TDR). Signals are input to a simulated or real PCB structure and the timing and amplitude of the reflections simulated or measured, and the results analysed and displayed as a graph of impedance versus time [10] [11]. The usefulness of the TDR graphs is that they show the designer where, along a trace, an impedance problem is occurring and how serious the problem is. Figure 6E shows an example of a TDR measurement made with three different rise/fall times, and was developed from Fig 4 of [9].
Figure 6E shows how digital signals with rising and falling edges of 1ns see the averaged impedance of a PCB trace. The effects of connectors and via holes on the characteristic impedance are 'smoothed out' by the slow rise and fall times. But as a signal's rise/fall times reduce the effects of the impedance discontinuities due to connectors, via holes and other details become more apparent, as shown by the TDR curves for rise/fall times of 300ps and 150ps.

Serial data at 2.5Gb/s uses non-return-to-zero (NRZ) coding to employ a fundamental frequency of 1.25GHz, implying a maximum rise (and fall) time of under 200ps to achieve a reasonably open ‘eye pattern’. Since the intention is to increase the serial data rate to 5 and 10GHz in the next few years, we clearly need to be concerned about maintaining transmission line matching with rise and fall times of 150ps or less – so connectors and via holes are going to present significant problems. Techniques for dealing with some of the issues are discussed below.

In the 150ps curve of Figure 6E the TDR feature corresponding to the location of impedance matched connector shows that its impedance is around 60Ω, and the rounded top of its curve suggests that this impedance would not change much if signals with even shorter rise/fall
times were employed instead. 60Ω is not a perfect match for the 50Ω transmission line, and creates a reflection coefficient of +0.09, but it is much better than the connector that connects the signal cable to the PCB.

But the TDR feature that corresponds to a via hole is still quite sharp even with the 150ps rise/fall time signal. A via hole is too short for this signal to show any flattening or rounding off of the curve that which would imply that its actual impedance was no longer being ‘smoothed out’ by the risetime. So in the case of the via hole we should expect that signals with rise/fall times shorter than 150ps would experience even lower impedances, higher reflection coefficients and worsened SI and EMC.

1.6 When to use matched transmission lines

The crude guide for SI is to use matched transmission lines when the propagation time \( tp \) along the entire trace from the source to the final load equals or exceeds half of the signal’s real rise time: \( tp \geq \frac{tr}{2} \). If the real fall time \( tf \) of a signal is shorter than its real \( tr \), the value for \( tf \) should be used instead.

When \( tp \geq \frac{tr}{2} \) it is usually considered that transmission line techniques are required so that waveform distortion and eye-pattern closure will be acceptable for SI. But some engineers are a little more careful and prefer to use transmission line techniques for SI when \( tp \) exceeds \( tr/3 \), or even less.

The aim of these crude guides is to ensure that the first reflection due to a mismatched trace occurs during the rise (or fall) time of the signal, where it will (hopefully) be masked by the rising edge and cause no problems for the receiver. If the trace was so long that its first reflection occurred after a logic transition had finished, the result could easily be double clocking or other digital glitches, so it becomes necessary to use matched transmission line techniques. Significant overshoot and ringing could still occur and so these guides might not
be good enough for SI for some devices, and they do not control EMC as well as is often
required for greatest cost-effectiveness in product design. Always read all the application
notes for a device carefully to see if it has more stringent requirements than the above guides.
If the length of a trace is \(\ell t\) and the velocity of propagation along the trace is \(V\), then that trace’s
\(t_p\) is given by: \(t_p = \ell t / V\). So we can modify the above guidance to say that: for SI, transmission
line techniques are necessary when \(\ell t \geq V \cdot tr / 2\) or less.
For example, a stripline in an FR4 PCB with \(k = 4.2\) has a bare-board \(V\) of 6.8ps/mm (see a
later section), so a digital signal with a rise/fall time of 2ns (actual values, not data sheet
specifications, see later) would need to use matched transmission lines for any traces that are
longer than 147mm, for acceptable SI (98mm for the ‘more careful approach).
We all like to use simple arithmetic to save time, but it is important to be aware that the above
guides really are very crude indeed. Their assumptions about logic thresholds, eye patterns
and EMC may not be true for other types of devices. And they take no account of the effects
on \(V\) and \(Z0\) of the capacitive loading of vias and devices (see later) or of the return path
inductance caused by via holes or imperfect planes (also see later).
Engineers who take account of these complicating issues can achieve good designs in less
time than those that merely follow the crude guides above. In fact, for good SI, a final design
might require the use of transmission line techniques when \(t_p\) exceeds a value that lies
between \(tr/3\) and \(tr/10\).
Figure 6Fi) shows these various guides on a graph of rise/fall time against trace length.
From Figure 6C we can see that when a plain trace on a bare FR4 PCB has a length of about one-fortieth of the wavelength at the highest frequency of concern, it has an ‘accidental antenna efficiency’ of about –20dB. To prevent traces becoming more efficient antennas than this, the equivalent of the crude $tp \geq tr /2$ guide is that we should use $tp \geq tr /8$ to determine how long a trace can be before we need to use matched transmission line techniques for good EMC. In frequency terms (see a later section) we can write this instead as $tp \geq 1/8\pi f$, where $f$ is the highest frequency of concern.

Of course, using transmission line techniques for even shorter traces should improve EMC even more. The EMC equivalent of the ‘more careful’ approach is to use transmission line techniques when $tp$ exceeds $tr /12$. Continuing the example used above for SI, for good EMC a matched transmission line should be used where the trace length exceeds 37mm (or 25mm when using the ‘more careful’ approach).

But the above EMC guides are based on crude assumptions, and it may even be that good EMC requires the use of matched transmission lines when $tp$ exceeds a value that lies between $tr /12$ and $tr /40$.

Figure 6Fii) shows these various guides on a graph of rise/fall time against trace length.
To avoid the uncertainties in the above guides, simulation techniques are recommended. For good SI these should simulate the final design (the full details of the final PCB layout, plus all of its device loads) for all traces for which the bare-board $t_p \geq tr/10$, or $t_p \geq 1/10\pi f$.

For good EMC the final design should be simulated – at least for all traces carrying ‘aggressive’ or ‘sensitive’ signals (see later) – for which the bare-board $t_p \geq tr/40$, or $t_p \geq 1/40\pi f$ ($f$ being the highest frequency of concern).

Simulation is becoming increasingly affordable – and increasingly necessary in modern PCB layouts (a section on simulation is included later in this article). Where simulation is not an option, but good line matching is nevertheless required, the references given later provide some simple formulas that allow the effects of vias, stubs, load capacitance and imperfect return current paths to be taken into account. These calculations are not as accurate as simulation, so add an ‘engineering margin’ of at least 25% to their results.

1.7 Increasing importance of matched transmission lines for modern products

Some modern high-speed interconnections can launch two or more data bits before the first edge of the first bit has even reached the end of the trace. Reflections at impedance discontinuities along the trace and at mismatches at its ends cause data-pattern-related noise
on the line – as well as overshoot and ringing on rising and falling edges. The increasingly short real rise/fall times of modern sub-micron ICs are less tolerant of PCB layout, as Figure 6E shows.

So it is becoming more important to more accurately match and maintain \( Z_0 \) along the whole length of a transmission line. Even via holes are becoming significant. Microwave design techniques (e.g. adding ‘stubs’ of certain lengths) are increasingly needed to maintain \( Z_0 \) within close tolerances for every millimetre along a trace.

1.8 It is the real rise/fall times that matter

When designing a PCB, the focus is naturally on the traces carrying signals with high edge-rates or the high frequencies, but even signals with a low frequency can cause excessive emissions. For example, a 1kHz clock generator with extremely short rise and fall times has caused emissions test failure all the way up to 1GHz; and a pulse-width-modulated (PWM) drive for a brushless DC motor has interfered with 6GHz radio communications, despite the switching rate being just a few tens of kHz.

Data sheet rise/fall time specifications (where they exist at all) are almost always just the maximum for the temperature range concerned – but actual rise/fall times are (almost) always shorter than data sheet specs, often a half or a quarter of the specified maximum.

In addition, older devices may have gone through a die-shrink or two, to put them on smaller silicon processes that make more money for their manufacturers – if so, their rise/fall times will be very much less than their data sheet specifications. Examples include HCMOS and ‘F’ series TTL ‘glue logic’ devices, the data sheets for which still quote the same rise/fall times as they did in 1985. But the actual silicon features used in current distributor stock of these IC types could now be ten times smaller than in 1985, and their rise/fall times could be at least ten times shorter than the maximum figures in their data sheets. HCMOS ICs are specified as
having rise and fall times no longer than 5ns – but experience at the time of writing shows they can cause significant emissions at up to 900MHz, implying that their real rise/fall times might be as low as 300ps.

Another issue, mentioned briefly above and covered in more depth later, is that the capacitive loading of a trace, for example by connecting a number of devices along its length, reduces $V$ even further. So it could very easily be the case that a well-established type of IC with data sheet rise/fall times of 2ns (e.g. ‘F’ series TTL) – driving a multidrop bus – may need to use matched transmission lines for SI when trace length exceeds 20mm.

It is vital to know the actual rise/fall times of the digital signals that will be used in a PCB. It is impossible to do transmission line design using data sheet specifications for the vast majority of ICs. But few manufacturers even seem to know the rise/fall times of the devices they are currently manufacturing (and they care even less). To try to encourage manufacturers to supply this essential design data, we should all make sure we always ask for real rise/fall time data, including their maximum and minimum values (see “Ask For It” in [12]).

Given the lack of hard data on rise/fall times it is often necessary to use a high-speed oscilloscope with high-frequency probes and probing techniques (the ‘scope manufacturer will advise) to measure real circuits. An oscilloscope/probe combination with a bandwidth of $BW$ has a rise/fall time of about $1/(\pi BW)$ ($BW$ in GHz gives rise/fall time in ns). So a $BW$ of 1GHz would imply that a ‘scope/probe combination has a rise/fall time of 320ps – making it difficult to accurately measure signals of less than 1ns. With such a scope, if a digital signal was measured as having a rise time of 330ps, the actual rise time of the signal could be anywhere between 10 and 200ps. To measure rise times of 100ps typical of PCI Express needs an oscilloscope/probe combination with a $BW$ of around 7GHz – not a trivial requirement.
Luckily, there are an increasing number of ICs that are designed with slew-rate-controlled
driver outputs. These have been produced to make it easier to send fast data over
transmission lines, and sometimes to improve EMC as well. Such ICs are always to be
preferred over the more usual type that switches as fast as its silicon processing allows,
whether the user needs such short rise/fall times or not. There is more discussion of drivers
later.

In some industries it is normal for design to be progressing on the basis of an IC that is not yet
available for testing. Where these are ASICS or FPGAs, and if data on real rise/fall time is not
available (even from IBIS or SPICE models) it may be possible to obtain another type of IC
made using the same types of drivers, and measure their rise/fall times in a test board. Where
it is impossible to obtain a good estimate of the real rise/fall time data for an IC that will be
using a sub-micron silicon process, it is often best to lay the PCB out with filters on all the
driver outputs that could toggle at more than 1kHz, but only fit the filter components if SI or
EMC tests show they are necessary. Filtering is covered later.

If the ICs used will always have rise/fall times of at least 1ns (despite possible die-shrinks in
the future) or else are filtered (see later) to achieve the rise/fall times – transmission line
design is not very difficult, and much of this article will be redundant.

1.9 Noises and immunity should also be taken into account

Designers usually only consider using transmission line techniques for signals that have high
data rates or high sinewave frequencies, but as was mentioned above it is the rise/fall times
that matter for digital signals – not their clock or data rate. But reducing the emissions caused
by unwanted noises, and/or improving immunity, can also be good EMC reasons for using
transmission lines.
Digital ICs suffer from ‘ground bounce’ noise, and its equivalent ‘rail bounce’ noise (sometimes called rail collapse noise). A large part of this noise is what is known as simultaneous switching noise (SSN) or simultaneous switching output (SSO). Whenever an output pin changes state, the current it draws from its ICs 0V and power rails eventually flows through the interconnections to the PCB’s 0V and power rails. The inductance in these paths causes voltage drops that make the IC’s internal 0V and power rails ‘bounce’ with respect to the PCB rails, according to the activity of the output ports. This process is shown by Figure 6G for ground bounce, but rail bounce is caused in the same way.

This means that the logic high and low levels from a device’s output pin, that we often assume to be static levels, can be very noisy due to the operations of the other outputs on an IC. Some device manufacturers include SSN/SSO specifications on their data sheets – obtained by measuring one static output whilst all of the other outputs are toggled at a specified rate when driving specified load impedances. For SI reasons it is important that SSN/SSO noise is less than the logic threshold of the device the static output is connected to, but this is not always achieved – sometimes it is necessary for reliability reasons to alter a product’s software to reduce the number of outputs on a device that can change state at once.
The ‘core logic’ processing in digital ICs is not connected directly to any output pins, but its operation modulates the power supply current drawn by an IC and so adds to the ground and power bounce noise. The core logic of some Xilinx FPGAs (and probably those of many other manufacturer’s ICs too) can have power current demands with 50ps durations – equivalent to a noise frequency spectrum that extends to at least 13GHz.

All this means that even ‘static’ digital signals can be very polluted by very high frequency noise. When this noise travels on traces that are not properly matched transmission lines, their ‘accidental antenna’ effects can make them a source of emissions. So it may be necessary to either filter out this noise (see later) or else treat the lines as matched transmission lines to reduce their accidental antenna efficiency.

Immunity is also a topic hardly ever discussed in connection with transmission lines. But reducing a trace’s ‘accidental antenna efficiency’ by making it a matched transmission line (especially a stripline) can be a big help in improving the immunity of any signals, analogue or digital.

For instance, a reset line on a PCB is considered to be a static line, only changing state very occasionally. But it can be a long trace and hence a very effective ‘accidental antenna’ (if not
treated as a transmission line) and so it can be a significant emitter of the very high frequency 
ground-bounce noise created inside the ICs it is connected to. Its long length and good 
accidental antenna characteristics also make it an easy route for interference to get into an IC 
and cause it to misoperate or even be damaged. A later section goes into these topics in more 
detail.

Filtering ‘static’ traces at each IC they are connected to easily prevents these EMC problems 
(see later). But filtering may not be a viable solution for all of the non-transmission line traces 
on a PCB, so it may prove necessary to treat them as transmission lines just to reduce their 
efficiencies as accidental antennas.

1.10 Calculating the waveforms at each end of a trace

Knowing the source impedance of a driver chip when pulling up or down (they are different), 
plus the characteristic impedance and tp of a trace designed as a transmission line, and its 
load impedance, makes it easy to hand-calculate the waveforms and timing at the driving and 
receiving ends of the trace (and any point in-between). The “Lattice Diagram” is a graphical 
method of keeping track of these calculations and what they represent.

This process is complicated by the fact that actual driver output impedances vary according to 
the voltage and current they are outputting, and whether they are pulling up or down.

“Bergeron Plots” using device manufacturers’ data make it easy to discover what their actual 
impedances are. Sometimes they can have higher impedances than the Z₀ of the traces they 
drive, so their actual output voltage is severely attenuated at first.

Rather than describe the above process in this article, the author instead refers the reader to 
the excellent Motorola (now called Freescale) application note AN1051 [13]. This document 
assumes that the characteristic impedance is constant along a trace, but as Figure 6E shows
this may not be a safe assumption when real rise/fall times are under 1ns, as many now are unless they have been filtered to slow them down.

A small mismatch along a line, or in its resistive terminations, might make very little difference to the voltage waveform. But mismatches of under ±10%, that are often perfectly acceptable for SI reasons, can cause large overshoots in the trace’s current waveform, significantly increasing emissions from the PCB.

1.11 Examples of two common types of transmission lines

Figure 6J shows an example of a commonplace type of PCB transmission line – the *symmetrical stripline* – which is a trace on an inner layer of a PCB that is spaced half-way between two reference planes. The reference planes are assumed to extend a great distance on all sides of the trace, and beyond its ends. A simple formula that provides an estimate of its characteristic impedance \( Z_0 \) in \( \Omega \) is:

\[
Z_0 = \frac{60}{\sqrt{k}} \times \frac{\ln \left( \frac{1.9H}{0.8B + C} \right)}
\]

– where \( k \) is the dielectric constant of the PCB’s substrate (typically 4.2 for FR4 above 1MHz); \( B \) is the trace width; \( C \) is the thickness of the copper material used; and \( H \) is the substrate thickness. Note that it does not matter which length units are used in this equation: millimetres, inches, miles or whatever – as long as they are consistent, the answer is in ohms.

The propagation velocity \( V \) for a stripline in ns/metre (or ps/mm) is:

\[ 3.335 \sqrt{k} \] (approx. 6.83ns/m or 6.83ps/mm for FR4).
Figure 6J also shows the second example of a commonplace type of transmission line – the *surface microstrip*. This consists of a trace on an outer layer of a PCB over a large reference plane (on an inner layer of the PCB). The reference plane is assumed to extend a great distance on all sides of the trace, and beyond its ends. A simple formula that provides a guide to its characteristic impedance $Z_0$ in $\Omega$ is:

$$ Z_0 = \frac{87}{\sqrt{k + 1.41}} \times L \frac{5.98H}{0.8B + C} $$

The propagation velocity $V$ for a microstrip in ns/metre (or ps/mm) is:

$$ 3.335\sqrt{0.475k + 0.67} \text{(approx. 5.5ns/m or 5.5ps/mm for FR4)}. $$

$V$ in microstrip is a little faster than $V$ in a stripline, because in a stripline all of the electric field lines around the trace travel in the dielectric, so its $C0$ is higher than in a microstrip, where some of the electric field lines travel in the air outside the PCB. But the electric field lines in the air mean that microstrip is a bit ‘leakier’ than stripline, so when we consider emissions we always prefer striplines for good EMC.

Formulae for calculating $Z0$ of a large number of types of PCB transmission line geometries are given in the standards IEC 61188-1-2:1998 from http://www.iec.ch/webstore, IPC-2141.
and IPC-2251 from http://www.ipc.org. IPC-2251 replaces IPC-D-317A. These standards also include a great deal more useful information on designing with PCB transmission lines.

But it is now easier, and more accurate to use computer-aided design tools to calculate $Z_0$ and other aspects of transmission lines. The types of tools available include numerical solvers and field solvers. They provide much more accurate analysis, are now easy to use, and allow quick ‘what if’ assessments. A number of free transmission line calculators can be downloaded from the Internet (see the references at the end), but better ones can be purchased, for example from companies that provide CAD packages for PCB design.

Many of the available tools assume ideal transmission lines (e.g. with infinite reference planes), but some are real field solvers, and some can now deal with real, complex PCBs including capacitive loading – see the section on field solvers below.

1.12 Coplanar transmission lines

These can be useful when a transmission line needs to be routed without a reference plane on an adjacent layer. Routing signal traces run side-by-side with return (0V) traces is a good EMC practice, even when not using transmission lines, but for a coplanar line over a plane the 0V traces should be via’d to an unbroken (solid) 0V plane every $\lambda/10$ (or less) at the highest frequency of concern.

1.13 The effects of capacitive loading

It was mentioned above that capacitive loading on a transmission line reduces the velocity of propagation of signals along it ($V$) and also reduces its characteristic impedance ($Z_0$). Many transmission line equations, calculators, articles, papers and textbooks assume ideal PCBs, with no via holes, connectors or ICs. Their omissions are a common cause of additional PCB design iterations – some traces may need to be treated as transmission lines, when the bare-board calculations had shown they would not; some traces may need their geometry or
termination resistors modifying to achieve better matching. To improve time-to-market we must design real-life transmission lines, which means taking capacitive loading into account.

One cause of capacitive loading is the pins of the ICs or other devices (diodes, transistors, etc.) connected to a transmission line. There is always such a device at each end of a trace, where their capacitance will have some effect on the quality of the line termination but will not alter the line’s $Z_0$ or $V$. It is the pins of devices that are connected along a line, such as a typical multidrop bus (e.g. microprocessor memory and address busses) that will reduce the line’s $Z_0$ and $V$.

We must not overlook the effects of stray capacitances either. There is a stray capacitance at every via hole (typically in the range 0.2 - 2pF) causing a local reduction in impedance (see Figure 6E). A transmission line trace with a lot of vias in it will have lower than expected average $Z_0$ and $V$. More detail on via capacitance is given in “Via Capacitance” and other articles in [12].

“Resonances in Short Transmission Lines” in [12] describes how capacitive loading at the end of a line can cause huge amounts of ringing and overshoot in traces that would be ignored when following the crude guides given earlier.

If a metal object such as a heatsink or a sheet of metal such as the wall of an enclosure is placed close to a microstrip transmission line it will also add stray capacitance to the trace. Plastic objects or sheets, cables or condensation close to a microstrip line will also increase its stray capacitance. The only thing that should be within 5mm of a microstrip line is air or a similar gas, or vacuum.

The reference planes on both sides of a stripline shield it from the stray capacitance of nearby metal or plastic, but it is still affected by the capacitance of device pins that connect along its length.
In some cases, the effects of capacitive loading can be compensated by reducing the width of the trace in the effected region, and "Potholes" in [12] provides some calculations appropriate for 'point' capacitances such as vias or device connections.

It may be practical to use a technique used by microwave RF designers – adjusting the diameters of vias and their pads and the clearance holes ('antipads') in the planes they penetrate, to maintain the desired value of Z0 through the via holes. But some RF design techniques are bad for EMC in general – in this case making large holes in reference planes can cause problems for return currents. They can also increase plane impedance, leading to higher levels of CM emissions and poorer immunity.

Simple formulae for the effects of capacitive line loading are given in [13], as follows:

\[
Z_0(\text{loaded}) = \frac{Z_0}{\sqrt{1 + C_d/C_0}}, \quad V(\text{loaded}) = \frac{V_0}{\sqrt{1 + C_d/C_0}}
\]

where: 
- \( C_d \) is the load capacitance per unit length 
- \( C_0 \) is the intrinsic (bare-board) line capacitance per unit length 
- \( V_0 \) is the intrinsic (bare-board) line velocity 

\( C_d \) is easy to calculate from a PCB's circuit design. For example: if a 150mm long section of trace is connected to one pin each on ten ICs, and the capacitance for each via hole, pad and IC pin totals 10pF, then we have 100pF spread along 150mm of trace, making \( C_d \) equal to 100/150 or 0.667pF/mm (667pF/m).

\( C_0 \) and \( V_0 \) can be found from formulae given in IEC 61188-1-2:1998. Where a line’s \( V_0 \) and \( Z_0 \) are already known, its \( C_0 \) can be found from: \( C_0 = \sqrt{k/(V_0xZ_0)} \). So, for \( C_0 \) in pF/mm: \( C_0 = \sqrt{k/(0.3xZ_0)} \).

But it will generally be better and more accurate to extract \( C_0 \) and \( V_0 \) from draft PCB layouts, using a field solver (see later), for each individual section of a trace.
The length of trace to which the above expressions should be applied depends on the rise/fall times (or highest frequencies of concern) of the signals or noises to be controlled. Where the rise/fall time is so long that the whole length of a trace and its capacitive loads (due to IC pins, via holes, or other physical features) can be treated as one average value, the above expressions can be applied to the whole trace. (For example, see the 1ns curve on Figure 6E.)

But where the rise/fall time is short enough for significant impedance discontinuities to arise within the length of a trace (for example, see the 300ps curve of Figure 6E) the above expressions can be used over trace sections short enough to be treated as an average impedance value. The trace width can then be varied within each section, depending upon the capacitive loading of that section, so that every section has the same impedance.

But where rise/fall times are very short (or frequencies very high), even features as short as 1mm may create unacceptable impedance discontinuities (see the 150ps curve on Figure 6E.) and the above expressions may no longer be useful. If these signals or noises cannot be low-pass filtered, the only solution may be to design the circuit differently, for instance by using point-to-point serial data busses instead of multidrop parallel ones (circuit design is discussed in a later section). A useful technique is to route the trace on a single layer, so that it has no via holes along its length.
Because the rise/fall times of digital devices based on modern silicon processes are naturally so small, and getting smaller [6] – and because the frequencies of the ‘core noise’ that leaks into their I/O pins are naturally so high, and getting higher [6] – the problems of trying to create transmission lines that are well matched along their entire lengths are getting much harder, unless the signals can be low-pass filtered (see later).

1.14 The need for PCB test traces

Process quality variations in PCB bare-board manufacturers can cause out-of-specification batches of assembled boards to be made. It is very important that such boards do not have value added to them (by assembly) before their dire nature is exposed. So it can be important to include ‘test traces’ (sometimes called ‘test coupons’) on the PCB, so that PCB batches can be checked for $Z_0$ and $V$ upon delivery, before they are accepted into the company’s stores. Appropriate test instruments, suitable for use by non-specialists in a production environment, are required for testing the coupons, and one manufacturer of such instruments is Polar Instruments [14]). The design of the test coupons so that a PCB can be fully characterised at Goods Receiving is covered by [15].
An example of a process issue is variations in trace width, caused by under- or over-etching. In a modern PCB manufacturing plant, the variations from batch to batch are usually less than 13 microns (0.5 thou) and the effect of this on \( Z_0 \) is usually only considered to be significant when trace widths are less than 0.13 mm (5 thou). But differential lines are very sensitive to this problem (discussed in detail later).

1.15 The relationship between rise time and frequency

Digital hardware engineers work in the time domain, and for them a digital signal is a different voltage level bracketed by rising and falling edges. But EMC and RF engineers work in the frequency domain, using spectrum analysis tools. For them, a digital signal is a ‘comb’ of harmonics starting at the fundamental frequency: the data rate. When trying to design PCBs for good EMC, it often helps to be able to relate the time domain to the frequency domain, and vice-versa. Doing this properly requires Fourier transforms, and some digital oscilloscopes are fitted with Fourier post-processing options allowing a captured waveform to be viewed in the frequency domain. The author is not aware of any spectrum analysers that offer inverse Fourier transforms, converting measured spectra into waveforms.

The spectrum of the harmonics of a digital signal continues to infinity, but the frequency \( f \) at which its harmonics start to diminish rapidly and very soon become negligible is given by: \( f = \frac{1}{\pi \cdot tr} \). (This relationship can be seen in the two vertical axes of Figure 6F, the real rise time on the left and the equivalent ‘highest frequency of concern’ on the right.) So a signal with 1ns rise and fall times when viewed on a spectrum analyser or EMC receiver has a ‘comb’ of harmonics that have significant amplitudes to at least 318MHz.

The guidance given earlier said that, for good EMC, accurately matched transmission line techniques are strongly recommended when \( \frac{lt}{V} \geq \frac{V.tr}{8} \), although a more careful approach
would use them whenever $lt \geq V.tr/12$, or less). Simulation of the final design (including device loading) is recommended when $lt \geq V.tr/40$.

Now we can convert this into guidance for sinewave signals or noises: accurately matched transmission line techniques are strongly recommended when $lt \geq V/8\pi f$, although a more careful approach would use them whenever $lt \geq V/12\pi f$. Simulation of the final design is recommended when $lt \geq V/40\pi f$.

The broadband sinewave signal designer’s equivalent of overshoot and ringing is the flatness of the amplitude versus frequency response, whereas for a narrowband (fixed frequency) sinewave designer it is just a matter of gain. Using the SI guides above could result in several dB of ‘flatness’ variation, or a few dB gain error. Using matched transmission line techniques for traces longer than $V/12\pi f$, or even shorter traces, may be required where amplitude flatness or gain specifications are tight.

Hopefully, this section will allow readers who prefer to work in the frequency domain to quickly convert from the frequency to the time domain (e.g. from millimetres to GHz), and vice-versa.

12 References


Volume 4 - Safety of Electrical Equipment ISBN 1-902009-08-8


13 Some useful sources of further information on PCB transmission lines (These are not referenced in the article.)


Brian Young, “Digital Signal Integrity Modeling and Simulation with Interconnects and Packages”, Prentice Hall, 2001


California Micro Devices: http://www.calmicro.com/applications/app_notes.html or go to: http://www.calmicro.com then click on ‘Applications’ then click on ‘App Notes/Briefs’


UltraCAD: http://www.ultracad.com

LVDS: http://www.national.com/appinfo/lvds/


Note: On the Intel and IBM sites, to find application notes you must first choose a type of device.


Cypress Semiconductor Corporation, many useful application notes at: http://www.cypress.com

IEEE Transactions (www.ieee.org) on…

– Electromagnetic Compatibility
– Advanced Packaging
– Components, Packaging and Manufacturing Technology
– Microwave Theory and Technology

IEEE (www.ieee.org) Conferences and Symposia on…
– Electromagnetic Compatibility
– Electrical Performance of Electrical Packaging

Printed Circuit Design magazine http://www.pcdandm.com/pcdmag/

CircuitTree magazine: http://www.circuitree.com

IMAP Symposia

DesignCon Symposia

Some free PCB transmission line calculators

http://www.emclab.umr.edu, click on ‘PCB Trace Impedance Calculator’

http://www.amanogawa.com, click on ‘Transmission Lines’, then ‘Java Applets’

http://www.mwoffice.com/products/txline.html

http://www.ultracad.com/calc.htm

Relevant Standards


IPC-2141 and IPC-2251 from http://www.ipc.org

I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than the series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of
Missoura-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; Howard Johnson of Signal Consulting, Inc., http://www.sigcon.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

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NOTE - Due to the length of Part 6, this will be split over 3 issues of the journal.
Advanced PCB Design and Layout for EMC
Part 6 - Transmission Lines

Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

Due to its length we have had to split Part 6 between three issues. This issue contains Section
2 - Terminating transmission lines and Section 3 - Transmission line routing constraints.

This is the sixth in a series of eight articles on good-practice design techniques for
electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This
series is intended for the designers of any electronic circuits that are to be constructed on
PCBs, and of course for the PCB designers themselves. All applications areas are covered,
from household appliances; commercial, medical and industrial equipment; through
automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm chip processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC.

Like the above articles, this series will not spend much time analysing why these techniques work, it will focus on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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2 Terminating transmission lines

A transmission line must be terminated at its ends with resistors that match its characteristic impedance. Only then does it become a ‘matched transmission line’, and only then do all of the SI and EMC benefits arise.

Where the rise/fall time is long enough – or the highest frequency of concern low enough – the entire length of a trace with all of its low impedance discontinuities (e.g. due to capacitive loads) and high-impedance discontinuities (e.g. due to perforation of the reference plane) can be treated as one averaged impedance. This is then the impedance that must be matched by the terminating resistors.

But where the rise/fall time is short enough for one section of a trace to have a significantly different characteristic impedance from another section (see the 300ps curve on Figure 6E), it will be impossible to match the transmission line. The characteristics of the trace and its loads, reference planes and other physical features must be modified so that each section has the same characteristic impedance as is desired, then this is terminated in matched resistors at the ends of the line.

Variations in impedance that are considered acceptable for SI purposes may be too high for good EMC. So, for good EMC, take more care in matching the impedances along the length of a trace, and at its terminating resistors.

2.1A range of termination methods
RF and microwave designers use very narrow frequency ranges, so they can terminate their transmission lines in complex impedances that are carefully designed to do exactly what they want them to over that small range. But SI and EMC require termination to be effective over a wide range of frequencies – so resistors that maintain their resistive behaviour from d.c. to the highest frequency of concern are required. Ideally, this requires using very small surface mounted ‘chip’ resistors (but not MELF types, because they are too inductive).

Very short and direct connections between the terminating devices and the reference plane(s) are required. Ideally ‘via-in-pad’ techniques should be used, where practical. Crosstalk between termination resistors can occur, so where there are two or more close together they should be arranged in a neat line, with their 0V ends (or other reference plane connections) at the same end.

When choosing a resistor network or array for termination: to be effective at frequencies above 100MHz they must have reference plane connections at both ends of the device, at least. For effective termination above 1GHz they will probably need to have as many reference plane pins as signal pins. Some PCB manufacturers can laminate high-resistance metal foils as internal layers in PCBs, which are then etched to provide termination resistors.

‘Classical RF’ termination, where the transmission line is resistively matched at both ends, is the best method for both SI and EMC, but attenuates the signal voltage by 50%. This type of termination is often used for RF and datacommunications over cables, and for very high-speed backplanes, and it is the best termination method for both SI and EMC. But digital ICs will not work with half-height input signals, so for digital circuits on PCBs single-ended resistive termination is traditionally used instead [13]. Some types of ICs may soon be available with drivers that use internal voltage boosters so that classical RF termination can be used whilst providing the full signal voltage that the receiving ICs require.
There are a variety of single-ended termination methods available, divided into ‘reflected wave switching’ and ‘incident wave switching’ types, as shown in Figures 6L, 6M and 6N. Designing classical RF termination combines both reflected and incident wave methods – so will not be discussed here as a separate topic.

Reflected wave switching is sometimes called ‘series’ or ‘source’ termination, and is shown in Figure 6L. The driven end of the transmission line is terminated with an overall resistance equal to the line’s $Z_0$, and – when perfectly matched – launches a half-height signal voltage transition into the trace. When the signal transition reaches the end of the trace, the very high impedance there creates a reflection coefficient of almost +1, reflecting the transition back down the line – but this time with a voltage that is almost the full height of the wanted signal. The reflected transition travels back along the trace, establishing the correct signal voltage along it as it goes. When it reaches the driver termination the reflection coefficient is zero (if the line is perfectly matched), so the signal voltage transition does not reflect again.

Reflected wave switching is good for point-to-point interconnections. If used for a multidrop bus there is the possibility that the devices along the line will be ‘double clocked’ because they will see half the signal amplitude some time before they see the full signal. Such devices need
to be slow enough when responding, when compared with the propagation time along the line, to ensure that the reflections along the line will not confuse them. Alternatively, ensure that all of the load devices are located at the far end of the transmission line, separated from each other by traces for which \( t_p \geq t/10 \) or \( t_p \geq 1/10\pi f \) for SI, or for good EMC: \( t_p \geq t/40 \) or \( t_p \geq 1/40\pi f \).

The series terminating resistors used in reflected wave switching must be located very close to the driver, and, as shown in Figure 6L, the value of the resistor is chosen so that the combination of driver impedance and external resistance equals the line’s \( Z_0 \). With ‘ordinary’ digital ICs (not designed for transmission line matching) it may be hard to achieve good matching when pulling-up and when pulling down, and this is discussed later.

Figures 6M and 6N show the variety of incident wave switching methods. They all use a single-ended resistive termination at the furthest end of the transmission line from the driver. An idealised driver with a 0Ω source impedance launches a full-amplitude signal voltage transition onto the trace, which then travels along the trace until it reaches the very end, where a ‘parallel’ or ‘shunt’ terminating resistor is installed. Assuming matching of this resistance with the \( Z_0 \) of the trace, the reflection coefficient will be zero so there will be no reflections.

There will be reflections at the launching point, but these are all contained within the driver and not seen outside its IC. If the impedance of the load is less than 100 times \( Z_0 \), the value of the termination resistor should be chosen so that the parallel combination of load and the termination resistance equals \( Z_0 \). Parallel termination resistors are usually connected to the 0V plane, but some logic families use other reference planes (e.g. ECL uses the positive power plane) so these are where the termination resistors should connect to, instead.
Incident wave switching allows multidrop busses to be used at much greater data rates than reflected wave switching. Using shunt resistor terminations consumes a lot of power, and may exceed the d.c. current limits of some drivers, so a variety of alternative termination circuits have been developed to reduce power consumption and d.c. current (hopefully without compromising the line matching too much at the highest frequencies). Alternative types of incident wave switching termination include ‘RC’, ‘Thévenin’ and ‘Active’.

RC termination (Figure 6M) uses a resistor value equal to the line’s $Z_0$, and capacitor values that are usually between 10 and 620pF. It only terminates the line at high frequencies, and the idea is that it will consume less power, and because it consumes no d.c. current it should be easier to drive with ‘ordinary’ devices.

But the effectiveness of RC termination depends upon the randomness of the data and the length of the trace, so it is not a universally applicable technique as the other three incident wave methods are. The power saving is only achieved when the RC time constant is less than the duration of the signal level. Also, the RC time constant must be larger than twice the loaded line’s delay time for it not to cause SI problems. For more on this see “AC Terminators” in [12].
Because of the self-inductance of capacitors [16] it may be more difficult for an RC termination to equal the highest frequency performance of a purely resistive termination methods. Some component manufacturers offer single or array devices that package the R and C together to save PCB area, and these can be designed to have better high-frequency performance than discrete components.

Thévenin termination (Figure 6N) uses resistor values designed so that their parallel resistance is $Z_0$, and their ratio minimises the power consumption and the d.c. loading of the driver. Ideally, this means choosing the resistor ratio so that the d.c. voltage at the transmission line, with the driver disconnected, would equal the average line voltage when it has data on it. Thévenin termination needs a properly decoupled power plane at all frequencies of concern, refer to [16] for how to achieve this.

![Figure 6N ‘Incident Wave Switching’ using Thévenin and Active transmission line termination methods](image)

Active termination (Figure 6N) uses a voltage regulator to drive an additional power rail (or reference plane) at the nominal average value of the digital signals, or some other suitable voltage. A parallel terminating resistor with a value of $Z_0$ connects to this plane, which must be properly decoupled for the frequencies of concern (see [16]). Electrically equivalent to the
Thévenin method, active termination can save overall power consumption by running the voltage regulator (which needs to be able to source as well as sink current) in Class AB mode.

Where a transmission line passes through a connector, a common problem is an intermittent or failed connection. The undriven line will still have crosstalk and other noises on it, which can lead to random data activity of the device the line connects to. Finding such faults can be made much easier when Thévenin or active termination methods are used, by biasing their ratios or voltages so that when the driver is disconnected the load device is guaranteed to go to a logic high or low. Choose the ‘connector failure’ logic level on the basis of which causes the fewest operational problems or best aids fault diagnosis. Where safety is a factor, this should influence the choice of logic level too.

Where a ‘stub’ trace connects to the trace that is the main transmission line, two consequences are possible, depending on the length of the stub and the capacitance or any load connected to it. Where the stub’s propagation time is very short compared with the signal’s rise/falltimes (or wavelength at the highest frequency of concern) it, and any device capacitance, will appear as a point capacitive load, and should be treated as discussed in the earlier section on capacitive loading.

But where the stub’s propagation time is not insignificant (compared with the signal’s rise/falltimes or wavelength at the highest frequency of concern) the effect is more complex. The $Z_0$ at the junction will be the parallel combination of the main line plus the stub (for example: if both have the same $Z_0$, the result will be $Z_0/2$), and reflections from both the stub junction and the end of the stub will propagate in the main transmission line and distort the signal.

Ideally, the end of such a stub would be terminated correctly in an accurately matched resistance, but this still leaves the reflections at the junction. Correctly terminating a
transmission line with stubs can be a complex task, and sometimes the only practical solutions may be less than ideal. Some of the references at the end of this article provide some guidance on this, especially the textbooks and the IPC standards.

2.2 Difficulties with drivers

Matching a trace’s characteristic impedance at the driver end can be difficult for devices that are not carefully designed for driving transmission lines. For most ‘ordinary’ digital ICs, their pull-up impedance is higher than the trace’s $Z_0$, and their pull-down impedance is lower than $Z_0$, so correct series termination at the source end – whether for classical RF or reflected wave switching – is impossible. [13] gives several worked examples of this situation.

When using incident wave switching, the non-zero driver impedance means that the full signal voltage can not be initially put on the line. The driver will eventually charge the line to the correct voltage, but this might take a while so could result in data timing problems. One common solution to this is to terminate the line in a value that is higher than $Z_0$, so that there is some reflection at the end that will compensate for the lack of initial driving voltage, and [13] gives a worked example of this. But this solution may mean that point-to-point connection is required instead of multidrop bussing (unless the devices along the line are slow in responding when compared with the trace’s propagation time).

The above situation is further complicated by the fact that digital ICs have a dynamic output impedance that depends upon their output voltage. Calculating what voltages will result from driving transmission lines becomes iterative, which is why [13] describes the Bergeron Plot method for avoiding endless calculations.

Further complications arise from the fact that there can be wide variations in driver output impedances from one batch to another, of the same device from the same manufacturer. The
variations between different batches of the ‘same’ device from different suppliers can be even greater.

Some drivers cannot source enough d.c. current to drive an incident wave terminator if it just a single shunt resistor. RC, Thévenin or active terminations may be required. If these cannot be used either, reflected wave switching using a series resistor at the driver end may be the only solution.

But many ICs are now designed with output drivers suitable for driving transmission lines properly, especially where high clock or data rates are required. These devices can be recognised by the transmission line matching data provided in their data sheets, or from the specifications for their output impedances. A driver designed for driving transmission lines will have a low output impedance, say around 10Ω; when pulling up or down, making it much easier to correctly match to a transmission line. Such devices are much preferred over ‘ordinary’ or ‘glue logic’ digital ICs when transmission lines are to be driven. Even so, these devices will have small differences between their output impedances when pulling up or down, so some types may be better than others for EMC reasons.

Note that ECL devices have an output impedance of around 10Ω (pulling up or down) and have always been excellent for driving transmission lines.

2.3 Compromises in line matching

Termination techniques recommended by device manufacturers, such as [17], are usually based on SI requirements not EMC. Some techniques will be necessary because others won’t work (e.g. Thévenin or active termination is usually required for CMOS ‘glue-logic’), but others will often be a compromise between component cost and PCB area; power consumption and battery life; shielding, filtering and number of PCB layers; use of ‘terminating plugs’; EMC, etc.
Reflected wave switching and higher values of trace $Z_0$ both tend to cause lower levels of emissions (all else being equal) because their signal currents are lower, so they emit lower levels of magnetic fields.

Small impedance discontinuities along a trace and small mismatches in its resistive terminations might be considered unimportant for SI, and yet be very important for EMC. SI considerations usually ignore mismatches of ±10% or less, because they make very little difference to the voltage waveform. But measuring the trace current waveform can reveal large overshoots caused by the discontinuities or mismatches, significantly increasing the emissions from the PCB. For good EMC it is important to terminate a transmission line in an accurately-matched resistance, as shown by the brief article “Reducing Emissions” in [12]. Trace current can be easily measured without having to cut the trace or lift an IC leg – using current probes supplied by oscilloscope manufacturers or magnetic close-field probes supplied by spectrum analyser manufacturers (or made by yourself [18]) and used to measure trace current without contact. To detect individual traces they should be made very small, usually less than 5mm diameter (although square shapes are often easier to use). Don’t forget that magnetic field probes respond to the differential of the current. The use of classical termination (at both ends) helps reduce the effect of reflections caused by changes in $Z_0$ along a trace, such as are caused by stubs and vias. As mentioned earlier, one effect of this is to attenuate the signal by 50% – so the receivers used should have an adequate input range.

2.4 ICs with ‘smart’ terminators

Some ICs incorporate ‘smart’ output drivers (for example: Vertex-II FPGAs and Rocket I/O, both from Xilinx) that can be programmed to various impedances so that they match the PCB transmission lines, with no need for any series resistors for reflected wave switching. Some ICs include on-chip voltage doublers for their output drivers, so they can use classical
termination without losing 50% of the signal voltage. These are likely to give the best EMC (all else being equal). These smart driver technologies are usually available as IP for designing into FPGAs or ASICs.

But CMOS processes do not create very accurate resistors, so designers should always ask about the tolerance of the matching resistors built into their drivers or receivers, then take the worst-cases into account in their transmission-line design. Prototype ICs with integrated output drivers that automatically adjust their output and input impedances to optimise SI have been demonstrated – but it is not yet clear if they will achieve as good EMC as accurate matching with a discrete resistor.

In July 2004 a company called Adiabatic Logic Ltd claimed (EPD Magazine, page 43) to have developed “adiabatic” digital drivers. These were said to use reflected wave switching, but instead of terminating the reflected signal edge in resistance they put its energy back into the local power supply. The aim is to reduce power consumption, especially for battery-powered products. The author does not yet know of any EMC measurements made on devices using drivers based on this new technology.

2.5 Bi-directional terminations

Many modern busses don’t have a single bus master and one or more slaves – some or all of the devices can be drivers or receivers, and they are called bi-directional busses. The PCI Bus used in PCs (until its replacement by PCI Express) is an example of a bi-directional bus. Bi-directional transmission lines require reflected or incident wave termination at both of their ends, and maybe at some/all of the stubs along their route as well. In the case of reflected wave termination all of the line’s drivers are fitted with series-terminating resistors. The only problem that this causes is to create a small delay for a receiver that can also be a driver. But
in the case of incident wave termination, each driver must now be powerful enough to drive the Z0 of the transmission line plus a nearby parallel termination resistor.

Terminating multidrop bi-directional buses can be very difficult, and is briefly described in “Bi-directional Terminations” in [12]. Compromises are often required – for example “Bi-directional Alternatives” in [12] describes the PCI Bus as requiring its signals to make three or four ‘round trips’ of the line before settling down to a stable enough value (see Figure 6B).

2.6 Non-linear termination techniques

Diode termination prevents device damage or latch-up due to overshoots beyond the power rails, but it doesn’t terminate a transmission line’s Z0 properly. So the only significant EMC benefit from diode termination may be that they might help prevent transient damage as a result of a nearby electrostatic discharge (ESD). The diodes are not rated for handling ESD energies so should not be relied upon to protect an IC whose interconnections are directly exposed to ESD events. A correctly specified ESD protection device would be required for this.

![Figure 6P](image)

Diode termination techniques use Schottky diodes for the best clamping of overshoots, but even these become ineffective at the low values of IC voltage rails used these days (e.g.
1.2V) because their diode voltage drop is too large in comparison. At least one company has developed ‘active clamping’ devices that use transistors to clamp an overshooting signal to the PWR or 0V rails with very small voltage offsets. It has been claimed that they achieved SI as good as resistor termination, but the author is not aware of any data on EMC performance and suspects that it would not be good. Where multi-drop and/or bi-directional busses are used with variable populations of receivers (and/or drivers), achieving correct resistive or RC termination of all possible loading situations can be very difficult indeed, especially if users cannot be trusted to fit ‘terminating plugs’ in the unused positions. Using non-linear terminators such as the above active clamp devices would be a solution as far as SI was concerned, because they would not all appear in parallel (as shunt terminating resistors would). They are only in circuit when the signal tries to overshoot one of the rails. However, as mentioned above, the EMC of such a system is not expected to be very good.

2.7 ‘Equalising’ terminations

As mentioned earlier, for good SI and EMC (emissions and immunity) digital and analogue signals generally require resistive terminations for their transmission lines, using resistors that behave resistively up to the highest frequency of concern. And, also mentioned earlier, the complex impedance of a load (usually its capacitance) can cause a local reduction in \( V \), hence a local reduction in \( Z_{>0} \), possibly causing problems.

But when using incident-wave switching there are methods for making line terminations that use complex impedances (networks of resistors, inductors and capacitors) that compensate for the load’s impedances. For more on these techniques read “Constant-Resistance Termination” and “Constant-Resistance Equalizer” in [12].

3 Transmission line routing constraints
3.1 General routing guidelines

Transmission line routing should follow the guide below. These ‘rules’ are very important for traces carrying signals or noises with rise/fall times under 1ns, or carrying sinewave signals or noises above 300MHz. These rules are also useful for any high-speed signals.

- Route power supply decoupling first of all. These traces should be very short (see [16]) so won’t restrict routing elsewhere on the PCB. This will probably require hand routing, not autorouting.
- Next, route the most ‘aggressive’ and most ‘sensitive’ signal nets. Aggressive nets include all clocks, write strobes, output enables and chip selects; sensitive nets include edge-triggered clocks, interrupts, asynchronous presets/resets/sets, and all resets.
- Make the most aggressive (or most sensitive) nets as short as possible, moving components as required (within component placement constraints). This will probably require hand routing, not autorouting.
- Route the most aggressive (or most sensitive) nets on the PCB layer that is closest to the 0V plane of a 0V/power plane pair.
- Route data busses and other transmission lines next, and keep them well away from the above lines to minimise crosstalk.
- Route all transmission lines (and any high-speed traces) on one PCB layer, where possible (see later). This is most important for any very aggressive (or sensitive) lines.
- Use striplines instead of microstrip (for EMC, if not for SI). This is most important for any very aggressive (or sensitive) lines.
- Don’t route any traces over breaks in their reference planes. This is most important for any transmission lines, especially very aggressive (or sensitive) lines or other high-speed interconnections.
- Don’t route transmission lines close to edges or gaps in their reference planes. Ideally route at least 5mm away, or five times the trace width, whichever is the greater.
- Don’t use mesh or grid routing, unless all the resulting ‘stubs’ are so short that they don’t create significant impedance discontinuities. Instead, it is best to route directly to use ‘daisy chain’ routing (as in Figures 6K and 6Q) or ‘star’ routing (see Figure 6R). When star connecting lines: all of the lines appear as parallel loads to their common driver (e.g. three 100Ω lines look like 33Ω), so ensure the driver can drive the resulting impedance.
- When all of the decoupling and transmission line (or high-speed) nets have been routed, the rest of the PCB can be routed.
Ensure each load on the line is much greater than $Z_0$ – except for any parallel termination resistors, of course.

Many PCB designers with good EMC experience now refuse to use autorouters at all.

3.2 A transmission line exiting a product via a cable

Where a transmission line leaves a PCB (and the reference planes in the PCB) but is carried by a shielded controlled-impedance cable, it is important that the shield of the cable has 360° electrical bonding to the reference planes used for the return currents in the transmission line. 360° electrical bonding of shields is described in Part 2 of [1] or [2], and Volume 2 of [5]. For
differential transmission lines, it may be important to use filtering at connectors even when
shielded cables and connectors are used, see later.

Where a transmission line leaves a PCB (and the reference planes in the PCB) but is carried
by an _unshielded_ controlled-impedance cable, it is important for EMC that filters are located at
the point where the signals leave their reference planes. Sections 6.2, 6.6, and 7, figure 2P
and figures 2S – 2Y of [8] are particularly relevant. The filtering should remove all the signal
and noise frequencies that are not required for the reliable communication of the wanted
signals via the cables. The best filters employ common-mode chokes, and these are
especially important for serial data communications in very noisy environments (e.g. CAN bus)
or where high data rates are required (e.g. Ethernet, USB2.0, Firewire).

The connectors and cables used when routing a transmission line off-board must maintain
exactly the same characteristic impedance as the trace(s) in the PCB. We are all familiar with
the venerable BNC connector, available in 50Ω and 75Ω versions, and the 50Ω and 75Ω
coaxial cables used to connect to them, but there are many more types of
controlled-impedance connectors and cables available. In general, for good EMC, avoid
coaxial cables and connectors and instead use types that route the return current path in its
own conductor, so that there are always two wired conductors per transmission line, such as
shielded twisted pairs. Cat 5, 5e, and 6 unshielded twisted pairs are good cables for SI, but
their shielded versions are much better for EMC.

When using a shielded cable, the shield should always be 360° terminated at both ends
wherever the signal carries RF signals or noises – as even low-frequency analogue signals do
these days, due to the common-mode noise from switch-mode power converters and digital
electronics. Also use 360° termination at both ends whenever there are RF electromagnetic
fields in the environment – as there always are. Of course it is possible for low-frequency
analogue signals to be heavily filtered, at their inputs and outputs from a product, so that they do not need cable shielding for good EMC.

Where a transmission line exits a metal (or metallised) enclosure (or chassis), there should be at least one very short electrical bond between the 0V plane of the PCB and the metalwork of the enclosure or chassis. This is normal good practice for EMC [19]. Where the shield of a shielded cable is bonded to the PCB’s 0V plane, it can also provide the necessary 0V plane – chassis bond at the chassis by 360° electrical bonding in the chassis-mounted connector or cable gland.

3.3 Interconnections between PCBs inside a product

It is by far the best solution for EMC to use a single PCB for each product, so that there is no need for any interconnections between PCBs. Even mezzanine boards, daughter boards, and plugging boards into a backplane are not ideal from an EMC point of view, because of the difficulty of effectively routing the reference plane(s) through the connectors and cables between the PCBs.

Non-EMC advantages of the single-PCB-per-product solution include…

- Saving the costs of the connectors and cables
- Saving the costs of assembling the cables and connectors
- Saving the costs of rework (connectors are usually the most unreliable part of a product)
- Reducing warranty costs (connectors are usually the most unreliable part of a product)
- Improving product quality and customer perception (because of the increased reliability through using fewer connectors)

Flexi-rigid PCBs can sometimes be used in place of separate PCBs connected by connectors and cables. Their use is often not even considered, because of the higher costs of their bare boards, but this can be short-sighted because they may be able to reduce the overall cost-to-make, and the warranty costs, of a product.
Wherever a transmission line (or other conductor carrying high-speed data or high-frequency signals or noises) exits a PCB – even if it is only travelling a short distance to another PCB – it may need to be treated as if it were leaving the product (as described in the section above). This is vital for products that are intended to be enclosed in unshielded enclosures. Ribbon cables can generally only be used for data communications in unshielded products if their signals are filtered to remove high frequencies from signals, and high-frequency noises.

Where a serial data bus connects between PCBs, a twisted-pair or shielded cable can be used. But it has been common practice in some areas to route parallel data busses between numbers of PCBs in a product, usually using ribbon cables. The EMC of such a design is very difficult without good shielding, even when the signals are filtered as described earlier. The SI and EMC of such product designs can be significantly improved by ensuring that each signal pin or conductor has an adjacent pin or conductor to carry its return currents. Where more than one reference plane is carrying return currents, more than one adjacent pin or conductor will be needed. In a ribbon cable, the outermost conductors should always be 0V or PWR, not signal.

The same guide applies to inter-board connectors where PCBs plug together. Figure 6S shows an example of a ‘backplane bus’ system, using a parallel data bus in which each conductor is a transmission line, and plug-in boards or modules. This is a very common type of product in some areas of industry, but the maximum data rate of the bus is limited by the lengths of the ‘stubs’ created by the connectors and traces of the plugged-in cards. A short stub looks like a capacitive load at a point on the line, whereas a long stub will create its own reflections if not terminated, and the point where it connects to the main line will have an impedance of half the line’s $Z_0$. 
High-speed busses in backplane systems like this might transfer data at up to a 50MHz clock rate. Some designers have managed to get such busses to run at 100MHz, and even 200MHz has been achieved with heroic design efforts. The problems of getting parallel busses to work at speeds as high as 200MHz or above is one reason why point-to-point serial busses are becoming so popular. A single 2.5Gb/s serial differential transmission line carries more data than a 16-bit parallel bus clocking at 100MHz, and the design of its transmission line is much, much easier.

Figure 6S also shows how important it is to place the data buffers as close as possible to the backplane connectors, to minimise stub lengths. The backplane connectors will be controlled-impedance types that match the line’s impedance, and they must have very short signal paths if high-speed is required. As was mentioned earlier, the connectors must also make numerous connections for all of the reference planes associated with the signals that pass between the boards. These reference plane connections must be spread over the whole length of the connectors – and if the connectors are very wide (for example, some backplane connectors have five or more rows of pins), they should also be spread over the width of the connector.
3.4 Changing plane layers within one PCB

Ideally, transmission lines (and high-speed signals) should be routed on a single layer in the PCB, over solid (unbroken) reference planes that extend a very great distance on both sides of their traces and well beyond both ends. But sometimes there is no alternative but to change layers along a trace.

Above about 10MHz, the plane return currents associated with traces are forced by ‘skin effect’ to flow in the surfaces of the reference planes or traces that are closest to the path of the opposing current (send or return). When traces change layers, their surface RF return currents simply cannot flow through the thickness of the plane to follow the route of trace. It may seem odd that electricity cannot flow through a metal plate, from one side to the other, but at high frequencies this is just what happens. (It is the same effect that allows thin sheets of metal to be used as RF shields – so we can think of it as one side of a plane shielding its return currents from the other side.) This self-shielding creates difficulties for transmission lines (and for any traces carrying high-frequency signals or noise).

Where a trace is routed against the other side of the same plane, its return current has to flow to the other side of the plane around the rim of the antipad in the plane created by the via hole for the trace. This forces the return current to be concentrated at the hole’s location, which increases the inductance and alters the characteristic impedance at that point.
Where a trace is routed against a different plane at the same voltage (usually 0V) the interplane capacitance is insufficient to make a good connection – so two via holes, one on each side of the trace should be added to link the two planes together. These via holes should be in a line with the via carrying the signal, perpendicular to the trace direction, and within 2mm of the trace via. (Where this is not possible, make sure that there is at least one plane-linking via as close as possible to the trace via.)

The inductance associated with the return path current as it flows in the via(s) will affect the local value of $Z_0$, (see “Via Inductance" and “Via Inductance II" in [12]), and this can be important where signals (or noises) have rise/fall times under 1ns or frequencies above 300MHz.

But where a trace becomes routed against a reference plane with a different voltage, it is important to connect a capacitor between the two planes, very close (i.e. < 3mm) to the trace’s layer-change. Two capacitors, one on each side of the trace, are better than one. The return current will pass through the capacitor(s), so the value and type of capacitor and its self-resonant frequency, should be chosen to suit the part of the spectrum that needs to be well controlled.
For transmission lines carrying signals with rise/fall times of 300ps or less (or sinewaves of 2GHz or more) it can be difficult to maintain the desired $Z_0$ over any portion of a transmission line for which the signal and its return currents are carried by vias. But it will be almost impossible to maintain the correct $Z_0$ where capacitors are used in the return path. For such signals it can be very important to have no layer changes at all, or to only allow layer changes that are either side of the same plane.

When changing layers near to a break or edge in a reference plane, the layer changes should be located at least 5mm from the nearest edge of the plane, preferably even further away.

Where there is more than one plane in a PCB, there are noise voltages between the planes. Via holes couple strongly with interplane voltage noise – so signals passing through via holes tend to add to the noise between the planes. The noise between the planes also tends to couple noise into the signals passing through the vias. Higher frequency signals and noise couple more strongly, so this is more of a problem for signals or noise with fast rise/fall times or high frequencies. This is another reason for referring all critical traces to either side of the same plane – and (better still) for not changing layers along their route.
For traces routed on internal layers in a PCB, there will always be a layer change (or a joint or ‘spur’ in the trace) at each point where the trace must connect to a device mounted on an outer layer. For signals with edges shorter than, say, 150ps there are significant problems in dealing with the mismatches caused by these layer changes or ‘stubs’ (see later). This is the main reason why high-data-rate PCB interconnections are now abandoning traditional parallel multidrop bus technology (e.g. PCI) – and using point-to-point LVDS serial data communications (e.g. PCI Express) instead.

These design constraints can lead to an increase in the number of plane layers – but the signal integrity requirements may leave the designer no choice but to increase the number of layers. Where achieving adequate EMC at PCB-level requires an increase in the number of PCB layers and hence the bare-board costs, the usual temptation is to hope for the best and use the lowest number of layers that will permit functionality. But this is usually a false economy – increasing the number of layers in a PCB is usually the lowest-cost and quickest way to deal with EMC.

When changing layers, don’t forget to change the trace width as required to maintain the same $Z_0$ for each section of the trace. Particular care is needed when using both stripline with microstrip sections along the same trace (see later).

### 3.5 Crossing plane breaks or gaps within one PCB

Ideally, no traces should ever cross plane breaks or gaps unless some kind of common-mode isolation (or at least filtering, see figure 4P of [20]) is applied at the location of the break, to both the send and return paths of the signal. Transmission-line traces that cross plane breaks or gaps should be closely-coupled coplanar types, with return traces on either side of the signal trace. Closely-coupled coplanar differential transmission lines (see later) are the best type for this purpose.
If there is no choice but to cross a break or gap in a reference plane with a type of transmission line that employs a reference plane, fit a ‘stitching capacitor’ on both sides of the trace – within 3mm of the trace on each side. Take care to minimise the inductance of the capacitor (e.g. by using a very small surface-mounted type, such as an 0201) and also to minimise the inductance of its interconnections to the planes on either side of the split.

Where a reference plane break changes from a 0V plane to a power plane, the stitching capacitors are effectively part of the power decoupling system and could be called ‘decaps’ (see [16]) – but this does not mean they can be moved further away from the trace.

As above, it will be almost impossible to maintain the correct $Z_0$ where capacitors are used in the return path to cross a break in a reference plane. So, where signals (or noises) must cross a plane break, they should be ones with very long rise/fall times, or where the highest frequencies of concern are not very high.

As was mentioned above, when routing transmission lines close to edges or gaps in reference planes, or when changing layers near to an edge or a gap - the routing and/or layer changes should be located at least 5mm from the edge or gap (preferably even further away).

3.6 Avoid sharp corners in traces

A sharp corner in a trace creates an impedance discontinuity due to the stray capacitance from one part of the trace to another, around the corner. Some studies have shown that 90° corners in a trace only have a significant effect on SI where rise/fall times are 10ps or less.

Nevertheless Intel and National Semiconductor recommend keeping the number of corners (and vias) in high-speed traces to a minimum, and ‘chamfering’ using two 45° bends to achieve a 90° bend (for example), or using smooth curves instead.

But PCB techniques for achieving adequate high-frequency SI are much less demanding than when those same techniques are used to achieve adequate EMC at PCB level. So even
where sharp corners are acceptable for SI reasons – it is best for EMC to chamfer or curve them where real risetimes could be under 1ns.

Of course, a via hole also represents two sharp 90° corners in a trace, which is another reason why transmission lines, and any traces carrying high-speed signals or noises, should ideally be routed on a single layer with no vias along its length, even if this means increasing the number of PCB layers. As has been mentioned many times in this series, increasing bare-board PCB costs to improve EMC is almost always much more cost-effective and quicker than any other EMC measures (other than those applied to the silicon die in the ICs).

3.7 Linking return current planes with vias or decaps

To prevent cavity resonances from occurring in the frequency range of concern for EMC, all the 0V planes (including any small or broken plane areas) should be /10 at the highest frequency of interconnected with via holes at least every λ concern, taking the dielectric constant of the PCB into account as described above. So, for example, to prevent cavity resonances in a plane pair in an FR4 PCB at frequencies up to 1GHz, plane-linking vias should be located at least every 15mm all over the planes’ areas.
Where the planes forming a cavity have different potentials, they should be linked by decoupling capacitors (decaps) instead of vias. These issues were discussed in more depth in Parts 4 and 5 [18] and [16] of this series. Linking planes together with vias or decaps is especially important when striplines are used. For a stripline, the return current flows in both of its planes, above and below the trace, and it is important to link these currents together at distances less than \( \lambda/10 \). However, the close proximity of via holes or decaps along the route of the trace can add capacitive loading and affect its \( Z_0 \) and its \( V \).

3.8 Effects of via stubs

The ‘unused length’ or stub of each via hole acts like a microwave designer’s ‘tuned stub filter’ that looks like a short circuit at resonance when its length is \( \lambda/4 \), \( 3\lambda/4 \), etc. Signals with frequencies that are within about \( \pm 30\% \) of the resonant frequency will also suffer significant attenuation [21] [22]. The extra capacitance of a via hole decreases the local propagation velocity when compared with a normal PCB trace, so in real-life the frequency of maximum attenuation will be significantly lower than that calculated from \( \lambda/4 \), \( 3\lambda/4 \), etc. using the normal values for FR4.

Considering the \( \lambda/4 \) stub resonance for example, via stubs with the following lengths can be expected to resonate and strongly attenuate signals over the following frequency ranges:

- 5mm (typical of a 22 layer backplane): 3 - 6 GHz (maximum attenuation around 4.5GHz)
- 4mm: 4 - 7 GHz (maximum attenuation around 5.5GHz)
- 3mm: 5 - 9 GHz (maximum attenuation around 7.3GHz)
- 2mm: 8 - 13GHz (maximum attenuation around 10.5GHz)

For signals that have their third or fifth harmonics in the above ranges (especially near the frequency of maximum attenuation) the result is waveform distortion and a more closed eye pattern, in other words a degraded SI. At the same time emissions are increased due to the
poor transmission line mismatching and increased reflections occurring over these frequency ranges.

So, when using Through-Hole-Plate (THP) PCBs it is best to keep PCB thickness to a minimum, ideally so that the problems caused by the length of the stub occur at higher frequency than is cared about. Alternatively, counterbore the PCB to remove the unused lengths of their vias (their stubs). This sounds like a costly exercise, but it can use the same machines as are used to drill the PCB in the first place, and Teradyne engineers have estimated that the bare-board cost would increase by about 7% [22]. They also found that it was possible to back-drill vias without harming PCB quality.

But microvia/HDI PCB technology (see Part 7 of this series) uses via holes that are just as long as needed for a signal to change layers, so does not suffer from via stub problems like THP technology does [22].

3.9 Effects of routing around via fields

When using THP PCB technology, arrays or fields of via holes such as those associated with ball grid array (BGA) devices and multiway connectors cause high levels of perforation in reference planes. It is very important to ensure that at least a thin ‘web’ of copper remains
around all the via holes’ antipads in each plane layer, but even so an impedance error is introduced in transmission lines that pass over such perforated areas. As BGA pin pitches reduce below 1mm even retaining a thin copper web between via holes becomes increasingly difficult – ultimately impossible.

This plane perforation reduces the shielding provided by the planes – increasing crosstalk and degrading SI. Also, a perforated plane has a significantly higher inductance, which increases the $Z_0$ of traces routed over such areas and can also create SI and EMC problems due to reflections at the resulting impedance discontinuities [23] when rise/falltimes are short enough. From an EMC point of view a perforated plane does not behave as an image plane as well as a solid plane does, so emissions are increased and immunity worsened.

The best solution to this problem is to use microvia/HDI PCB technology. This does not require every via to pass through every layer on a PCB, and so it can enjoy unperforated reference planes (see Part 7 of this series). But when THP technology is used the problems of reference plane perforation in via fields should be taken into account in the design. If the signal and noise rise/fall times are much more than twice the propagation time it takes to cross the perforated area, the effect of the perforation will be ‘smoothed out’ and should be easier to design around. But where rise/fall times are shorter, more detailed design analyses and TDR measurements on prototype board assemblies will probably be required, for optimum SI and EMC.

3.10 Other effects of the PCB stack-up and routing

FR4 has a nominal dielectric constant, $k$, of 4.7 at the usual measurement frequency (100kHz), but it can vary between 4.0 and 5.5 at that frequency, and it reduces as frequency increases so that is nominally 4.2 at $\geq 1$MHz. Grades of FR4 with controlled $k$ are readily available (e.g. 4.7 $\pm 0.1$ measured at 100kHz), cost very little more than the regular material, and should
always be used for FR4-based PCBs using matched transmission lines. When not using FR4, it is still important to use dielectrics with specified worst-case limits for their $k$ values. See a later section for a discussion of PCB dielectrics.

The PCB manufacturer uses the following types of materials in a PCB’s ‘stack-up’…

- **Caps.** Dielectric layers laminated with single-sided copper foil ready for etching to create the top and bottom layers of the PCB.
- **Cores.** These are cured flexible dielectric layers laminated with double-sided copper foil ready for etching to create internal layers for traces and planes.
- **Prepregs.** These are simply layers of uncured dielectric. They are used as insulating spacers between the copper foil layers of the cores, and of course they glue the PCB together when cured.

Only a limited range of dielectric thicknesses are available to the PCB manufacturer for caps, cores and prepregs – and this places limits on the ranges of trace widths that a designer can use to achieve the desired $Z_0$s. So PCB designers should always work closely with their PCB manufacturers, to design trace geometries that they can make at low cost that will achieve the desired $Z_0$s.

The dielectric constant $k$ of FR4 varies with resin content and thickness (as well as with frequency, temperature and humidity). Because it is a mixture of high-$k$ glass fibre and lower-$k$ epoxy resin, the usual assumption of 4.2 is only true for the bulk material. In the stack-up of a real PCB, resin-rich areas can be found close alongside each trace and in-between closely spaced traces on the same layer, such as differential pairs. The resin has a $k$ of around 3.0, so these resin-rich areas tend to cause $Z_0$s to be lower than expected.

When designing a PCB stack-up, designers tend to choose round numbers for the thicknesses of the ‘prepreg’ layers. But the finished thicknesses of caps, cores and prepregs – and hence the actual characteristic impedance achieved – depends upon the PCB construction, lamination pressure, heat input rate and border damming (to stop resin being
squeezed out) during lamination. It even depends on the copper patterns etched into the foils opposite the traces concerned.

For example: when a PCB is laminated but before it is cured, the ‘core’ layers are already cured and the prepreg layers are not. So the etched copper layers on the cores press into the prepreg layers, displacing a small amount of their material and reducing the thickness of the dielectric over the copper traces. When thin prepreg layers are employed, the difference in their thickness can have a significant effect on $Z_0$. But the wider the area of copper, the less is this effect, so that for two large planes facing each other the reduction in prepreg thickness can be negligible even with the thinnest prepregs. This issue, and other similar ones, are discussed in “Offset Stripline – Construction Matters” in [24].

When all of these effects are considered alongside the need for very good impedance matching to improve EMC and avoid adding cost to the product by improving its shielding and filtering – we find that manual calculations are impossible and ‘trace tuning’ board iterations are too time-consuming. We need to use PCB design tools that can handle these issues, and tools such as the SB200 stack-up tool and SI8000 impedance solver from Polar Instruments [24] [25] can help.
A later section discusses the use of computer-aided design tools to help reduce unit manufacturing cost and time-to-market. TDR is also a very valuable tool for these purposes (see above).

An increasing number of PCB manufacturers are becoming very skilled with transmission line PCBs (also known as ‘controlled-impedance’ PCBs) and some of them are equipped with sophisticated simulators and measuring equipment. The simulators help them help designers achieve what they need, and the measuring gear confirms that what was required is actually been achieved. These manufacturers can be a great help to a novice transmission line designer, as well as a good ‘technology partner’ for experts.

But some PCB manufacturers, especially at the low-cost end of the market, may not be very helpful, and/or may not be very well equipped for reliably manufacturing controlled-impedance PCBs. Some may not have much of a clue. Their salespeople may nevertheless manage to create the impression that they will be able to work with you to easily get up their learning curve and still produce cost-effective and reliable controlled-impedance PCBs on time. Do not even imagine that you can employ such companies to make a PCB using modern sub-micron devices and transmission line technology. Since manufacturing buyers naturally prefer to use the cheapest possible PCB suppliers – the project manager (or someone else with sufficient authority) should always keep an eye on who they are buying from to prevent them ‘saving money at any cost’.

3.11 Some issues with microstrip

Microstrip traces (those that are routed on the top or bottom layers a PCB) have FR4 or other PCB dielectric material on one side, and air on the other side. The result is that the effective $k$ value they experience is less than that of the bulk PCB material itself. All electrical signals and noises are propagating electromagnetic waves, and in the case of microstrip traces some of
the electric waves and half of the magnetic waves travel through the air, whilst the rest of the wave energy travels though the PCB dielectric. The wider the microstrip trace, the greater the proportion of electric waves travelling through the PCB dielectric – so for a microstrip, the effective $k$ value depends on the trace width. As a result, the $Z_0$ and $V$ of a microstrip line depend upon its width.

Another issue for microstrip traces is that they are usually coated with a solder resist layer, and sometimes conformally coated to prevent moisture ingress. Sometimes PCBs are encapsulated in silicone or resin or submerged in containers filled with special oils, to improve their reliability in harsh environments. Such layers, coatings or encapsulations have a $k$ that is very different from air ($k = 1$) and can have a significant impact on a trace’s characteristic impedance and the accuracy of its matching (see later). Sometimes beads of condensation or even films of water can occur on a PCB’s solder resist, and since the $k$ of water is 80 this can have a very significant effect indeed on the $Z_0$ and $V$ of microstrip traces. Where a trace changes layers so that part of its route is stripline and part is microstrip, these different parts will have different velocity factors and see different values of $k$. Unless care is taken over such mixed-type striplines, SI and EMC can be degraded by skew and mismatches.

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13 Some useful sources of further information on PCB transmission lines

(These are not referenced in the article.)


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California Micro Devices: http://www.calmicro.com/applications/app_notes.html or go to: http://www.calmicro.com then click on ‘Applications’ then click on ‘App Notes/Briefs’


LVDS: http://www.national.com/appinfo/lvds/


Note: On the Intel and IBM sites, to find application notes you must first choose a type of device.


Cypress Semiconductor Corporation, many useful application notes at:

http://www.cypress.com

IEEE Transactions (www.ieee.org) on…

– Electromagnetic Compatibility

– Advanced Packaging

– Components, Packaging and Manufacturing Technology

– Microwave Theory and Technology

IEEE (www.ieee.org) Conferences and Symposia on…

– Electromagnetic Compatibility

– Electrical Performance of Electrical Packaging

Printed Circuit Design magazine http://www.pcdandm.com/pcdmag/
CircuiTree magazine: http://www.circuitree.com

IMAP Symposia

DesignCon Symposia

Some free PCB transmission line calculators

http://www.emclab.umr.edu, click on ‘PCB Trace Impedance Calculator’

http://www.amanogawa.com, click on ‘Transmission Lines’, then ‘Java Applets’

http://www.mwoffice.com/products/txline.html

http://www.ultracad.com/calc.htm

Relevant standards


IPC-2141 and IPC-2251 from http://www.ipc.org

I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than the series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

Eur Ing Keith Armstrong C.Eng MIEE MIEEE

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Advanced PCB Design and Layout for EMC
Part 6 - Transmission Lines (Sections 4 to 11)

By Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

Due to its length we have had to split Part 6 between three issues. This issue contains Section 4 to Section 13.

This is the sixth in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm chip processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues

A previous series by the same author in the EMC & Compliance Journal in 1999 “Design Techniques for EMC” [1] included a section on PCB design and layout (“Part 5 – PCB Design and Layout”, October 1999, pages 5 – 17), but only set out to cover the most basic PCB techniques for EMC – the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC.

Like the above articles, this series will not spend much time analysing why these techniques work, it will focus on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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4 Differential matched transmission lines

4.1 Introduction to differential signalling

All the above has assumed signals use ‘single-ended signalling’ – that is: they are all generated and received with respect to 0V (sometimes with respect to some other voltage reference instead). But differential signalling is increasingly required for clocks and communications (e.g. USB2.0, Firewire, Ethernet, PCI Express [26]) for SI and EMC reasons. LVDS (low voltage differential signalling) technology is becoming increasingly commonplace, and PCI Express LVDS drivers have rise/fall times around 100ps.

Differential signalling uses two conductors driven in antiphase with each other. The result of a well-realised differential interconnection is better SI, lower emissions, increased immunity, and the creation of lower levels of ground and rail bounce noise.

Strictly speaking, and in an ideal world, there would be no need for any electrical connection between the reference voltages for the driver and receiver (but in the real world such connections help reduce common-mode emissions caused by imbalances, see later). Figure 6Y shows two examples of differential signalling. The first one is typical of digital differential signalling, which uses two single-ended signals with one of them being an inverted version of the other. Sometimes + and – symbols are appended
to the signal name to indicate a differential pair, instead of using a bar above one of them. Other names for differential signalling include ‘symmetrical’ and ‘balanced’.

Digital devices and operational amplifiers can only handle signals within a certain voltage range, limited by their power supply rails. Making the differential signals referenced to 0V ensures that the signals remain within the optimum range for the devices, and the common 0V reference plane connection provides a nearby return path for common-mode currents caused by the imbalances in any real-life differential signalling scheme. Imbalances and the common-mode noises they create are discussed later.

Where signals start or end as single-ended, we need devices that convert them into differential signals, and back again, somewhere in our circuits. But many transducers, such as moving-coil microphones, platinum resistance thermometers and dipole antennas, actually generate differential signals directly. Digital and analogue ICs that employ differential signalling can include the single-ended to differential (and vice-versa) converter circuitry within themselves. Another technique, shown in Figure
6Y, is to use a transformer to covert from one mode to the other (see the section on line matching, later).

When the propagation delay along a differential conductor exceeds half the rise time of the signal \((t_p \geq t_r/2)\) a differential transmission line is required for SI and EMC, just as it is for the signals discussed in the previous sections. As before, some more conservative designers prefer to use \((t_p \geq t_r/3)\) and the author recommends \((t_p \geq t_r/8)\) for improved EMC. A wide variety of differential lines can be constructed on or in PCBs, as shown by Figure 6Z.

All of the discussions in the earlier sections on transmission lines for single-ended signals apply equally well for differential lines – but to obtain all the benefits of differential lines there are a number of additional considerations, and these are covered below.

4.2 CM and DM characteristic impedances in differential lines
The \( Z_0 \) of each trace in a differential line depends on how each trace is driven with respect to the other. The even-mode \( Z_0 \) (sometimes called the common-mode or CM \( Z_0 \)) of a differential line applies when both lines are driven in phase with each other. This is different from the odd-mode \( Z_0 \) (sometimes called the differential-mode, or DM \( Z_0 \)) when both lines are driven in antiphase to each other. Yet another type of \( Z_0 \) arises when one trace in each pair is driven on its own, with the other held static. [11] gives an example of designing, simulating and measuring differential lines in a backplane-based product, including TDR simulations and measurements of the actual even and odd mode impedance achieved in practice.

So differential \( Z_0 \) only exists for differential-mode (DM) signals – but in real life no signals are ever perfectly balanced, and imperfections in the traces themselves also disturb their balance and give rise to common-mode (CM) voltages and currents. Unavoidable noises on traces, such as ground bounce and rail bounce, are also usually CM. So there are always CM signals and noises on differential transmission lines. Even when the DM \( Z_0 \) is perfectly controlled along the traces, and perfectly matched by the resistors at the ends, the CM \( Z_0 \) (which has a different value) also needs to be controlled and terminated. If the CM \( Z_0 \) is not controlled along the trace to minimise impedance discontinuities, and if both traces are not terminated correctly by the resistors at their end(s), CM voltages and currents will be reflected – distorting both
signal waveforms and possibly causing SI problems, but much more likely to cause significant EMC problems.

Until a few years ago the numerical formulae for calculating the various $Z_0$s associated with differential transmission lines were disputed. There now appears to be good agreement between the various calculation methods and field solvers – but when using formulae make sure they are taken from documents that were written after 2000, or use software applications that have issue dates of 2000 or later. Anyway, it is best to use a field solver to calculate differential line $Z_0$s (see later).

When routing traces carrying different signals on a PCB, they should be spaced far enough apart that their ‘stray’ capacitive and inductive coupling doesn’t cause crosstalk problems for SI (not discussed further here). But when routing a differential pair of signals they should be spaced as close together as is practical, to maximise the coupling between their traces. Such ‘closely coupled’ differential transmission line traces provide the best performance for both SI and EMC.

A differential transmission line that (for example) consists of two 50Ω transmission line traces that are so far apart that there is very little coupling between them, has a DM $Z_0$ of 100Ω and a CM $Z_0$ of 50Ω. But when the lines are close enough to couple with each other, their DM $Z_0$ decreases (e.g. to 67Ω) while their CM $Z_0$ remains unchanged.

So always minimise the spacing between the traces to maximise their mutual inductance and the capacitance between them. And control the geometry of the trace pair along its entire route to minimise impedance discontinuities in the DM and CM $Z_0$s. This helps to minimise imbalances in the differential line (see later) and is very
important for EMC. When routing a section of a differential line on one PCB layer against a solid reference plane (or planes) this almost always requires that the traces’ widths and spacing remains constant along the section. (Ideally the whole length of a differential line would be one such section.) For a lot more information on routing differential transmission lines see [27], [28] and [29].

Figure 6AA shows some examples of terminating differential lines when using incident wave switching (see earlier, and Figure 6M). Using the above example, the resistors (R1A and B) from the traces to 0V would each be 50Ω, and the differential resistor (R2) would be 200Ω. The CM $Z_0$ of 50Ω and is matched by R1A and B, whereas the DM $Z_0$ of 67Ω is matched by R1A in series with R1B (100Ω), in parallel with R2.

When using reflected wave switching (see earlier, and Figure 6L), both of the traces must be fitted with series resistors very close to the pins of their drivers. But it is impossible to match both the CM and DM characteristic impedances of closely-coupled transmission lines with just these two serial resistors. Another resistor will be required, connected between the two traces, to match the DM $Z_0$, just as is required when
terminating closely-coupled incident-wave switching differential transmission lines, as in the above example.

It is common to see differential transmission lines terminated with a single resistor between the two lines at the receiver, but this is only acceptable for EMC where CM chokes or other methods have been used to reduce the flow of common-mode (imbalance) current (see later) to negligible amounts.

It is also common to see differential lines terminated as if they were two independent single-ended lines, using series or shunt techniques. But this is only acceptable for EMC when the lines are so far apart that the coupling between them is negligible – and this is usually not the best type of routing for EMC anyway (although it may be the best possible when routing through a via field that does not permit two traces between pads, see later).

The important thing to remember where EMC is concerned, is that differential lines need to have all of their $Z_0$'s terminated in matched resistors one or both ends, so that problems are not caused by reflections in either their DM or CM signals.

Differential traces can be routed coplanar, on the same PCB layer or broadside, on adjacent PCB layers. Broadside traces are generally poorer for SI and EMC, for a variety of reasons (see “Asymmetry in Broadside Configuration” in [12]) so are not generally preferred. However, the broadside configuration can sometimes help achieve the least-worst EMC, see later.

4.3 Exiting PCBs, or crossing plane splits with differential lines
Closely-coupled differential transmission lines are the best type of transmission line to use if a signal has to leave its reference plane – for example when exiting a board to leave a product; when connecting to a different board in the same product, or when a signal must become referred to a different reference plane in the same PCB. They are also the best types of transmission lines to use when a split or gap in the same reference plane has to be crossed – with coplanar differential lines being the very best for this. But the routing guidelines listed earlier should always be applied as far as is practical: differential lines are not a universal panacea. (Note that splits in planes are no longer generally recommended, either for SI or EMC, despite what semiconductor manufacturers’ application notes or older textbooks might recommend [20].)

Where a differential line must exit its reference plane, whether to exit a product via a cable, or to connect to another board, filtering may be needed at the point where it leaves its plane, just as was described above for single-ended lines. X2Y Attenuators LLC (http://www.x2y.com) have recently developed a new type of capacitor that is very suitable for filtering differential signals or power. It has three electrodes arranged symmetrically, with the centre electrode being the reference plane connection. [16] described using such capacitors for PCB decoupling, where their reduced self-inductance makes them effective at much higher frequencies than normal discrete decaps, but they behave even more like ideal capacitors when used with balanced signals (or power). Figure 6AB shows an example PCB layout using the X2Y® devices.
4.4 Controlling imbalance in differential signalling

To maximise the benefits of differential lines for SI and EMC, it is important to maintain their ‘balance’ along their entire routes. Some guidance on this is given in [29], and in [26] (for PCI Express). Where planes suffer from gaps, or where shielded cables do not use true 360° termination at both ends, just 150ps of skew between the + and – signals can degrade the EMC performance of a differential line so that it is no better than using a single single-ended trace instead. There are numerous possible causes for differential signal skew, and these are the subjects of this sub-section.

The reason for this degraded EMC performance is shown in Figure 6AC. Line imbalance causes the relative timing (skew) of the differential signals to worsen, which directly results in CM currents. These must flow in a common connection between the driver and the load, usually the common reference plane. Where this common
connection isn’t very low impedance at the highest frequency of concern and where it is not in intimate physical proximity with the differential traces (or connectors or other conductors) along their entire route: just 150ps of skew causes DM to CM conversion (and vice-versa) that can cause problems for emissions (and immunity).

The CM voltage associated with a differential signal is related directly to the skew – a differential skew of X% of a signal’s rise/falltime results in a CM voltage that is X/2% of the differential signal voltage (see “Common Mode Analysis of Skew” in [12]).

There are a number of sources of imbalance that can affect the differential skew and hence compromise the emissions and immunity, including…

- Unequal stray coupling to the traces (e.g. one line is closer to the edge of the PCB, or to a gap or edge in the reference plane, or closer to a metal object, than the other; variations in trace spacing).
- Differences in trace widths.
- Propagation time differences for the + and – signals, caused by line length differences between the two traces; and/or differences in their propagation velocity.
- Driver timing asymmetry.
- Different driver impedances, pull-up to pull-down.
Each of these contributions is discussed in more detail below. It is recommended that a ‘differential skew budget’ is set, and the contributions from all of these different issues assessed to ensure that the majority of the PCBs will not have EMC problems due to this cause.

But following all the EMC guidance in this article, for example: routing using striplines on only one PCB layer, with uninterrupted reference planes that extend well beyond the traces on all four sides, would make differential skew less of an EMC problem. It is rare that designs are completed without some compromises somewhere, so field solver simulations (see later) may be required to discover just what the differential skew budget should be for a given interconnection.

**Unequal stray coupling to the traces**

When differential traces pass near metal, plastic, epoxy, ceramic or glass objects; plane gaps and edges; other traces; mounting screws, etc, one trace will have different ‘strays’ than the other, and the resulting line imbalance causes emissions to increase (because more of the wanted DM signal is converted into unwanted CM noise). Figure 6AG shows some typical examples of this.
Keep each trace well away from edges, gaps or holes in any planes, and any large vias or metal fixings. Ideally keep both traces more than $D/10$ away from the edge of a plane of dimension $D$. Recommended layouts for such situations can be found in application notes, articles and papers, (for example, the guidance on “avoiding differential pair routing violations” in [29]) – but most of these are only concerned with what is acceptable for SI. Good line balance for good EMC is much harder to achieve than acceptable SI, but (as mentioned at the beginning) setting tougher SI specifications than are necessary just for SI will generally help achieve better EMC.

Choose connector pins that have identical stray capacitance and pin length, which usually means they are symmetrical with respect to the shell and the other pins. Tests have shown that using the wrong pins for a differential line in a 15-way shielded D-type can increase emissions by 20dB.

Using stripline routing can help maintain differential line balance. Stripline between two unbroken planes is best, with vias or decaps linking the two planes at least every $\lambda/10$ over the whole PCB (at the highest frequency of concern), because the two traces are...
better ‘shielded’ from stray external capacitance and mutual inductance, and this reduces the unbalancing influence of lumps of metal or dielectric that are mounted on or near to the PCB.

Keep the differential line’s trace spacing constant, and try (wherever possible) not to split them when passing vias or other gaps in their traces’ reference plane. Avoid splitting differential traces as they pass through a field of vias such as under a BGA IC or a dense multiway connector – this often means using smaller ‘track and space’ layout widths than are offered by the lowest-cost PCB manufacturers [30]. Alternatively, use microvia/HDI PCB techniques instead of THP – discussed in more detail in Part 7 of this series.

**Difference in trace widths**

Variations in trace width during PCB fabrication can be a cause of imbalance. These can be caused by variations in the rate of copper foil etching, and/or variations in any subsequent plating, over the length or width of the PCB. Errors in trace width and spacing can also occur, depending on where they land on the virtual grid produced by the natural resolution of the Gerber phototool [31].

For single-ended transmission lines the effect of erroneous trace widths caused by the above is usually only considered to be significant when trace widths that are less than 0.13 mm (5 thou). But for differential lines, the effect on line balance (and therefore on DM-CM conversion and hence emissions) can be significant. To control process variations it is important to include test coupons at two or more widely-separated
locations on a PCB, so that manufacturing quality can be checked at the Goods Receiving department as part of a goods acceptance procedure [15].

It is quite possible that PCB test coupons would not detect trace width errors caused by the Gerber resolution, so the usual way of overcoming this problem (without using non-woven dielectrics, see below) is to route all narrow differential lines at angles of between 20° and 70° to the grid of the Gerber digitiser, so any effects due to digitisation cancels out sufficiently well on average along the traces.

Testing differential line test coupons requires the use of a 4-port vector network analyser, which used to be a very specialist and expensive piece of scientific equipment, but versions are now available suitable for testing at Goods Receiving, from manufacturers such as Polar Instruments [14].

**Propagation time differences for the + and – signals**

Where the signal route includes connectors and/or cables, note that 150ps of skew (see above) can be caused by about 20mm of path length difference in a stripline PCB trace in FR4, or 30 to 40mm of path length difference in a connector or cable (depending on their dielectrics). So, where reference planes or cable shields are not perfect along an entire route, to obtain significant EMC benefits from differential signalling when path length differences are the sole cause of differential signal skew – we should aim for path length differences to be no more than one-tenth of these figures.
But there are other contributions to skew too, so we probably need to aim for path length differences that are one-twentieth of the above figures, or less.

Differences in their propagation velocity $V$ between the two traces can be caused by trace routing on woven glass-epoxy substrates (such as FR4 and G-10). This has the same effect as a difference in the trace lengths. Routing differential lines at an angle of between $30^\circ$ and $60^\circ$ to the warp or weft of the fibreglass layers is usually enough to ‘average out’ the effects of the woven substrate [32] [33]. This issue is discussed in more detail in a later section.

**Driver timing asymmetry (between $+$ and $-$ signals)**

Better driver timing symmetry means that the $+$ and $-$ signals switch more nearly at the same instant (or in the case of sinewave signals, have less phase difference). The result is lower differential skew, which in turn means lower CM emissions from this cause.

So always check data sheets for maximum differential skew data. If it isn't in the data sheet, assume the specification is too poor. Even if a device measures correctly in a test rig, the manufacturer may at some point in the future ship devices that explore the entire ‘specification space’ permitted by his data sheet (see Chapter 15 of [34]) – so unless the maximum specification in the data sheet (or in a letter from the manufacturer) is good enough for a design, choose a device with a better specification.
For example, the data sheet for the DC90C031 LVDS Quad CMOS Differential Line Driver specifies its typical rise/fall time as 350ns and its differential skew as 80ps typical but 900ps maximum. Clearly, when using such a device, attention to the detail of the CM current return path is going to be important for good EMC performance from the PCB and the lowest cost products.

**Different driver impedances, pull-up to pull-down (driver output asymmetry)**

Unequal output impedances between pulling up and pulling down can make square waves rectangular. A real-life CMOS driver example has an output impedance of 44Ω when pulling up, but 11Ω when pulling down. Since the transmission line has a real impedance (typically somewhere between 50 and 120Ω), the result (in this example) is that the positive-going transitions propagate with different timing from the negative-going transitions.

Where the signal was intended to be a squarewave clock, the result is a rectangular wave and one effect of this is emissions at even-order harmonics of the clock frequency. (A pure squarewave only has odd-order harmonics in its Fourier spectrum.) But for differential lines it contributes to driver skew asymmetry, increasing CM noise emissions.

Adding some series resistance at the driver end of the transmission line can help a little. For example, adding 22Ω at the output of the driver should – in the above example – reduce even-order emissions by around 6dB. However, it is much more effective to use
devices containing drivers that are designed for driving transmission lines. These will usually have a low impedance (e.g. 10Ω) when pulling up or down, but always check the data sheet (or ask the manufacturer) for the worst-case difference between the pull-up and pull-down impedance, and use the devices for which the specifications prove they will be good enough in the actual PCB, taking all the other sources of differential skew into account.

4.5 Routing asymmetry

The importance of symmetrical routing of the traces in a differential pair was mentioned earlier, and of course routing the lines differently will alter the stray capacitances and inductances each is subject to and cause imbalance. Each trace in the differential pair couples to its nearby plane(s) and to the other trace, so asymmetrical routing varies the proportions of the DM and CM $Z_0$s associated with a differential transmission line.

It is sometimes recommended that a deviation in one trace can be compensated for by widening or thinning one of the traces – but this can only compensate one of the $Z_0$s. Where the differential pair are routed close enough to couple significantly, it is impossible to use compensation ‘tricks’ to maintain both the DM and CM $Z_0$s despite asymmetrical routing.

The best EMC is created by very closely-coupled differential lines routed totally symmetrically along their entire route, with their DM and CM $Z_0$s terminated at one (preferably both) ends. When using LVDS it is often possible to use classical
termination (both ends termination) on a PCB when using types of LVDS receivers that accommodate a wide range of input levels.

But in practice symmetrical routing can run into difficulties where there is a field of vias or pads, such as underneath a BGA device, or at connector pins. The ideal situation would be to route each pair symmetrically between the routing impediments, with a sufficient width of plane(s) on adjacent layer(s) to carry their return currents (see [20]) symmetrically located beneath the pair. Ideally, as shown in Figure 6AH, this would be achieved by using trace widths and plane spacings that were as small as they needed to be, given the spacing of the pads or via holes they were routed between – but where this requires traces and spaces of less than what is normally available at lowest-cost (18 microns, or 7 thousands of an inch, at the time of writing) the additional cost may not be commercially acceptable and alternatives may need to be found.

One alternative is simply to make the rising and falling edges of the wanted waveforms (and unwanted noises) so slow that the discontinuity caused by the asymmetry...
becomes negligible (see Figure 6E for examples), but this may not be practical where high data rates or high frequencies are needed for the desired functionality.

Another method that is sometimes proposed is to space the differential pair so far apart that they don’t couple significantly to each other (in which case the CM $Z_0$ is simply twice the DM $Z_0$), then route them as individual traces through the field of vias or pads, as shown in Figure 6AH. When using this method with high-speed or high frequency signals (or noises) it can be important to achieve an identical routing pattern for each trace, to maintain the line’s balance.

Where traces are close enough to couple (i.e. their CM $Z_0$ is less than twice their DM $Z_0$) splitting the traces around a via or a pad may be possible, as described in “Breaking Up a Pair” in [12]. But be aware of the difficulty of compensating for both the DM and CM $Z_0$s mentioned earlier.

Broadside routing of differential pairs is generally considered a bad idea (see “Asymmetry in Broadside Configuration” in [12] but in a field of vias or pads it at least allows the traces to maintain their relationship whilst routing only one trace between each pair of vias or pads – as shown in Figure 6AH – so it may turn out to be the least-worst alternative.

5 Choosing a dielectric

5.1 Effects of woven substrates (like FR4 and G-10)

The glass fibre used in popular PCB substrates such as FR4, G-10, Nelco 4000-13SITM, Rogers 4350B and Polyclad FR-406, has a much higher dielectric
constant than the epoxy resin (about 5.6 compared with about 3.2). So far in this article, we’ve assumed that for FR4 \( k \) has a nominal value of 4.2 (above 1MHz), but this is the average of the high \( k \) of the glass fibre and the low \( k \) of the epoxy.

The glass fibres used in PCBs are woven like ordinary cloth, with a warp and a weft (or ‘fill’) direction. Routing a trace along the warp or weft direction can result in a \( Z_0 \) that is lower than calculated assuming a \( k \) of 4.2, if it happens to lie predominantly over a glass-rich area [32] (see Figure 6AJ). But if the trace happens to lie predominantly over an epoxy-rich area, the characteristic impedance will be higher than calculated. The effect on the impedance imbalance of a differential line (and hence its DM to CM rate and hence its EMC) can be very significant [33].

Also, a trace route that lies over a glass-rich area will have a slower \( V \) than the average for the PCB, whereas a route over a resin-rich area will have a higher \( V \) than the average. This will cause a skew between the two signals in the differential line that will tend to close their ‘eye pattern’ and increase emissions. The amount of skew can be as much as 5% of \( t_p \), the propagation time along the trace (sometimes called ‘flight time’
flight) and can ruin attempts to minimise skew by trace length matching, especially important for EMC for differential pairs.

Of course, where the actual glass fibres will run in a PCB is unknown, and will vary between otherwise identical PCBs cut from the same FR4 panel and delivered in the same batch. Batch sampling using 'test traces' (see earlier) cannot deal with this problem. The usual way of overcoming this problem (without using non-woven dielectrics, see below) is to route all critical transmission lines – and all differential lines – at angles of between 30° and 60° to the warp or weft of the glass fibres in the PCB, so that the effect of the woven substrate cancels out sufficiently well [32].

Another technique is to make the spacing between traces whose propagation time is to be matched equal to the spacing between the glass bundles in the PCB material. Maybe someone will develop a non-woven glass-fibre PCB material that uses short lengths of glass randomly dispersed throughout the epoxy. [33] shows that PCBs based on glass fibre will have seriously difficulties with signals at 10Gb/s or more on traces longer than 600mm (e.g. in a backplane) even when using the above techniques. It is proposed that electronic deskewing should be used for higher data rates if woven glass-fibre is to be used for low-cost, but this would not help EMC.

Non-woven substrates are preferred, but such dielectrics are usually more costly than woven glass-fibre types. A way of obtaining the benefits of non-wovens whilst keeping costs low is discussed next.

5.2 Other types of PCB dielectrics
The death of FR4 and similar glass-fibre materials has long been predicted, but the alternative homogenous materials (such as pure polymers) are so much more costly that people keep on finding new ways of continuing to use them. Suppliers of homogenous dielectrics, often called microwave substrates, include WL Gore and Rogers Corporation.

One recent technique is to use one or two layers of a less lossy dielectric than FR4 (e.g. WL Gore’s “Speedboard C” prepreg in [35], GETEK in [11]) as a part of a stack-up that is predominantly FR4, as shown by Figure 6AK. This only adds a little extra cost compared with the traditional alternative of using all polymer layers, but not all PCB manufacturers may be able to successfully laminate different materials to create reliable PCBs. Accelerated life testing may be required to feel confident that such stack-ups will last the expected life of the product.

Figure 6AK Example of a low-cost stack-up that uses homogenous (non-woven) layers

6 Matched-impedance connectors
Transmission line traces that must connect to a device, or exit one PCB to connect to another (or to a cable) must retain the same characteristic impedance if excessive reflections are to be prevented, and good SI and EMC achieved. The effects of a poor mismatch can be seen in the TDR plot of Figure 6E, where the initial connection between the cable and the PCB can be seen to have a very much lower impedance than the 50Ω trace being tested.

This mismatch does not matter to TDR measuring equipment, but in a real system it would cause significant SI problems for signals or noises with rise/fall times under 300ps (or sinewaves over 1GHz) and EMC problems with even slower (or lower frequency) signals or noises. [11] describes using Teradyne VHDL-HSD connectors in a backplane system using LVDS at up to 5Gb/s. It includes TDR simulations for 100ps rise/fall times and real measurements of eye patterns and impedances.

A great deal has been written about the design of matched-impedance PCB connectors (such as the type shown in Figure 6AD) and their development (for example [23]) but further discussion is outside the scope of this article.
As well as having the correct $Z_\text{0}$s the connector pins used for differential signals should maintain the same path lengths for the + and – signals, which may mean buying connectors specifically designed for that purpose. Notice that differential transmission line connectors are all specified by $Z_\text{0}$, but this is only their DM $Z_\text{0}$ – their CM $Z_\text{0}$ is not part of their specification, and is almost certain to differ from the CM $Z_\text{0}$ of the differential traces on the PCB. This will create an impedance discontinuity for CM currents which could be bad for EMC and may even be bad for SI, especially if CM currents are high due to poor line balance.

This is a reason for at least making provision for filtering when differential traces must leave a PCB and pass through a connector and/or a cable – whether the connectors/cables are shielded types or not. Filtering transmission lines at off-board connectors was discussed earlier, and Figure 6AB gave an example of a layout for a filtered differential line and unshielded cable.

7 Shielded PCB transmission lines
7.1 ‘Channelised’ striplines

A stripline can be ‘channelised’ by running a ‘wall’ of via holes along both sides of the trace to create what is almost a shielded conductor inside a PCB, as shown in Figure 6AL. Sometimes designers route return traces either side of the signal trace on the same PCB layer to make a ‘shielded coplanar line’, otherwise described as a coplanar stripline. The via walls would follow the route of these coplanar traces, making it a channelised coplanar stripline.

![Figure 6AL](image)

This can be a very useful technique when crosstalk from a high-threat trace (such one carrying the output signal from an RF power amplifier to an antenna) into a nearby trace needs to be reduced. To be effective at reducing crosstalk, the via holes must be spaced no further apart than $\lambda/10$ at the highest frequency of concern ($= 1/\pi \tau$, where $\tau$ is the real risetime, not the data sheet specification) – and preferably a lot closer.
Channelised coplanar stripline techniques can also be used for differential lines, taking great care to maintain the line balance within the shielded coplanar channelised structure. As well as reducing crosstalk, such structures help prevent external influences (such as a mass of metal, PCB edge or a nearby gap in a plane) from affecting the characteristic impedance or unbalancing a differential line. The author doubts whether there are any equations for working out the $Z_0$ of a channelised transmission line, or a coplanar channelised line, and because its structure is not the same from point-to-point along the length of the trace a 3D (rather than 2D) field solver would probably be required.

7.2 Creating fully shielded transmission lines inside a PCB

Some PCB manufacturers can now create linear trenches between layers in a PCB, plate them with copper and fill them back up with epoxy. As Figure 6AE shows, these can be used to create well-shielded transmission line traces inside a PCB that have much lower crosstalk and much better EMC than ordinary transmission lines [36].

[37] gives a formula for calculating the characteristic impedance of such PCB structures, but it suffers from the simplifying assumptions required to create any EMC formulae, so might not achieve good enough matching for modern high-speed PCB interconnections.
8 Miscellaneous related issues

8.1 Impedance matching, transforming and AC coupling

Networks of resistors can be used to connect a line with one $Z_0$ to a line with a different $Z_0$. These are usually called 'matching pads' and their design is described in the short article "Matching Pads" in [12]. Transformers can also be used to transform the $Z_0$ of one transmission-line to match the $Z_0$ of another, by varying the ratio of the windings between primary and secondary. These impedance transformers are sometimes called baluns because they can also be used to convert from single-ended to differential transmission, or vice-versa (balun = balanced-to-unbalanced transformer).

As mentioned earlier in the section on terminating a transmission line, accurate matching is necessary when connecting two lines with different values of $Z_0$. Matching which gives an acceptable waveform for SI purposes might not be accurate enough for
good EMC. The use of a magnetic close-field probe (see earlier) on a simple trial PCB will help prove how accurate the matching needs to be.

Transformers can be used to ‘float’ a differential signal so that it is not connected to any reference voltage in either the driver or receiver. This is used in long cable-based transmission lines (such as Ethernet) to ‘break the ground loop’ caused by differences in the ground potential between widely separated parts of an installation, so the signal is less corrupted by ‘ground noise’.

Galvanic isolation by transformers (floating) is also used to help prevent overvoltage damage and electric shock hazards due to the ‘ground lift’ caused by electrical faults and thunderstorms – but the transformers should be tested and approved to the appropriate ‘withstand’ voltage according to appropriate safety standards, such as EN 60950.

When using transformers in a signal path it is important that the average d.c. content of the signal is close to zero. Any d.c. content will magnetise the transformer’s core, and if the d.c. content is enough the magnetisation will be sufficient to distort the signal as it passes through the transformer. A similar problem arises when a series capacitor is used to a.c. couple signals or data. In this case, if the d.c. content is not zero the capacitor will charge up (or down) and it is possible that its voltage will exceed the common-mode range of the receiver and impair signal quality.

There are numerous protocols for encoding serial data so that its d.c. content averages to zero, refer to “When to use AC coupling” in [12].

8.2 A ‘safety margin’ is a good idea
Real rise/fall times of around 300ps are not unusual at the time of writing, and they are heading inexorably downwards as 90nm silicon processes are starting to appear in volume-produced devices, and as developments promise devices based on in 65nm and 45nm processes in just a few years. As Figure 6E above shows, the rise/fall times of such signals is small enough that a single via hole can create an impedance discontinuity that can cause reflections that distort waveshapes, close eye patterns, increase emissions and worsen immunity.

‘Die shrinks’ by IC manufacturers during a product’s production lifetime can reduce driver rise and fall times. So where a new design is initially acceptable but doesn’t have a large margin, poorer EMC and even increased unreliability could occur after a year or two’s production due to die-shrunk ICs being provided in place of the expected parts.

Die-shrunk ICs are supplied with exactly the same part number and packages as the original slower parts – only the batch numbers reveal their true nature – and only then to someone who knows at what batch the die shrink was implemented. Some IC suppliers have agreements with their customers to provide samples of die shrunk parts 6 months before they appear in normal shipments, so that any design modifications found to be needed can be done in time.

But 6 months is not a long time, and the author knows of one large manufacturer who used tens of millions of a particular microprocessor in a very wide range of products which each had production lifetime of over 4 years. A die shrink in that particular device
resulted in all of their products having to be redesigned for EMC compliance, which took over two years to complete at a cost to the manufacturer of tens of millions of US Dollars.

So it is a good idea to try to find out what die shrinks are likely to occur in the IC’s being designed into a new product, over its likely production lifetime, then use the likely die-shrunk values for rise/fall time when designing the circuit and the transmission lines for its PCB.

It is better to use ICs whose drivers have a specified slew-rate – instead of the more usual ‘switch as fast as the silicon allows’ types. Die shrinks will have no effect on their rise/fall times – although the amplitude and frequencies of their core noises might be increased.

8.3 Filtering

Where the fastest rise/fall times or highest data rates or frequencies are not really required, it is usually possible to use low-pass filtering on the signals or noises – slowing down their transitions and/or reducing their highest frequencies. It might be practical to filter a driver output so much that transmission line techniques are not required at all, even for good EMC. This is a common technique for ‘static’ digital lines such as resets.

If matched transmission lines are required, the aim of filtering would be to make the rise/fall times of the signals or noises long enough to ‘smooth out’ the impedance discontinuities along a transmission line, making design much easier and improving SI and EMC (compare the impedance discontinuities seen by the 1ns and 150ps rise/falltime signals in Figure 6E). If rise/fall times can be limited to no less than 1ns (or
maximum sinewave frequencies to 320MHz) much of the finer detail about designing transmission lines in this article can often be ignored.

Capacitors should not be used alone as filters for signal traces. Observing the voltage waveform on a trace with an oscilloscope it will be seen that adding capacitance at a device pin will slow down its rise/fall times and/or reduce its high frequency content. But what the 'scope doesn't show is that the added capacitor draws very high transient currents, increasing the magnetic field emissions from a PCB. These currents also increase the voltage noise between planes and so increase the emissions of electric fields from the plane edges. They also increase the levels of ground bounce and rail bounce noise that occur in the driver ICs.

So capacitors in filters should always be used with series resistances or ferrites to limit any increase in transient current. The values of the resistances or ferrites should be chosen taking the $Z_0$ of the line into account.
Some designers use filter capacitors with reflected wave switching – placing capacitors of between 4.7 and 22pF between the trace and the 0V plane immediately after the series resistors (on the load side) [39]. These capacitors can be left unpopulated, and if EMC problems arise various values can be experimented with to see which achieves good EMC without compromising SI by filtering too much.

8.4 CM chokes

Where the CM return path for a differential signal is not as good as it could be, CM chokes can be used to raise the CM impedance – reducing the CM currents, and so reducing the CM emissions. These chokes take up quite a lot of PCB space, and are not low-cost components, so they tend to be used where a differential line exits a PCB into an unshielded cable such as UTP, and so loses its reference plane (which is the current path for its CM noise).

CM chokes are also very important where coaxial connectors and cables are used for high-speed signals. Coaxial interconnections actually work in triaxial mode, with the wanted signal’s RF return currents flowing on the inside of the cable shield (due to skin effect) and the external RF noise currents flowing on the outside of the shield (also due to skin effect).

But all flexible coaxial cables suffer from leakage through the thickness of their shields which gets worse as frequency increases (some types more than others – expensive “superscreened” coaxial cables can be very good). It is generally found in practice that
when using any types of flexible coaxial cables (other than superscreened) with data rates above 50Mb/s a CM choke is required to aid triaxial working and improve EMC. Part 1 of [1] and [2], especially its figure 11, show some relevant simplified schematics.

**8.5 Replacing parallel busses with serial**

Where the fastest edges or highest data rates or frequencies really are required for functionality, there is no choice but to deal head-on with all the imperfections in transmission lines and their terminations discussed in this article. Using classical line termination (see Figure 6J) helps a great deal, but if signal amplitude is not to be halved the driver circuit itself, inside the IC, must have pull-up and pull-down impedances that match the $Z_0$ of the transmission line and output the full signal levels required by the load.

There are clever ‘microwave design’ tricks that can sometimes be used, such as adding a small stub to a trace to add inductance or capacitance (at a particular frequency) to compensate for an imperfection in the trace impedance, but these are limited in their scope and only work over narrow frequency bands.

The general way to deal with impedance discontinuities along a trace is to design them out. This is why the current trend is to replace multidrop parallel busses with point-to-point serial busses using low voltage differential signalling (LVDS) techniques, which use matched differential transmission lines. [9] shows that increasing the size of the antipads in the plane layers that the via hole passes through will reduce their
capacitance so that they match the $Z_0$ of the line better, but this is achieved at the expense of increased perforation of the 0V plane(s) – not a good thing for EMC. So when using signals with very fast edges or very high frequencies, for good SI and EMC we usually need to minimise the number of vias along a trace, ideally routing each such trace on a single PCB layer along its entire route.

If our differential lines are striplines routed completely on one layer, and their reference planes are unbroken for a large distance around the trace – then the only capacitive loading on the line will be from traces routed nearby on the same layer, and from nearby metal features that penetrate through the PCB, such as via holes and fixing screws. A number of other issues can still arise, such as the characteristic impedances and stub filtering effects of the via holes at the ends of the line, and the effects of routing variations and the warp and weft of the glass fibres, resin rich areas, etc.

Careful design of the layout and stack-up, and the use of computer-aided design tools, can reduce the significance of all these details and achieve serial data interconnections that will run at very high data rates with good EMC.

8.6 The lossiness of FR4 and copper

Copper traces laminated into FR4 PCBs have an increased surface roughness due to the woven glass fibres in the FR4 substrates. FR4 itself is a lossy dielectric, with approximately 10 times the ‘loss tangent’ of other PCB materials such as the microwave substrates made by Rogers Corporation (and others) and ‘pure polymer’ materials such as those used in microvia/HDI PCBs (see Part 7 of this series). For
signals that are around 1GHz, these losses are generally only a problem for traces that are over 300mm long. Eric Bogatin of Gigatest Labs has a number of articles and presentations available on this topic [38], also see “Characteristic impedance of lossy line” in [12].

Pre-emphasis is often used to compensate for the low-pass filtering effects of FR4 at gigabit data rates. Pre-emphasis boosts the drive levels in such a way as to compensate for the filtering effects of extended PCB traces. For example, with pre-emphasis, serial busses such as Xilinx’s Rocket I/O claims to reliably support speeds of 3.125 Gb/s over transmission lines of at least 500mm in FR4.

At first sight, pre-emphasis appears to be solely an SI issue, not an EMC one, but pre-emphasis means boosting the amplitudes of at least the 3rd and 5th harmonics of a signal, which could lead to increased emissions at those frequencies.

8.7 Problems with coated microstrip

Figures 6A and 6Z show some examples of coated microstrips used for single-ended or differential transmission lines. The usual coatings are solder resists (solder masks) and component legends (sometimes called the ‘silk screen’ layer), although some PCBs are conformally coated to protect from moisture, and/or encapsulated to protect from shock and vibration.

But the dielectric constants and loss factors of many such coatings are not very well characterised at high frequencies, and the thickness of coating applied is often not very
well controlled [31]. In addition, most PCB specifiers only specify the solder mask by its solder-resisting qualities, leaving the PCB manufacturer free to substitute various alternatives. This can obviously cause variations in transmission line matching between different PCBs, and possibly over the width or length of a single PCB.

One way of dealing with this problem, suggested by [31], is to ensure there are no coatings or printed legends over any microstrip lines. Another way is to include a number of test coupons (see above and [15]) at widely-spaced locations on the PCBs and test them against specific performance targets at Goods Receiving before accepting each batch. Actually specifying the solder mask and legend materials by their manufacturers’ part numbers should also help maintain quality.

8.8 The effects of bond-wires and leads

In the past, it has been normal to treat the pin of a driver or receiver as the end of a transmission line. But as rise/falltimes reduce the lengths of the leads (pins) and bond wires associated with a device are becoming more significant.

With very fast risetimes, and/or devices that use very large packages (with long lengths of leads or bond wires), it is possible for a signal waveform to be measured as perfect at it’s pin’s solder joint to a PCB, but the actual waveform applied to the silicon is degraded. Conversely, the waveform at a pin can appear degraded whilst the waveform applied to the silicon is good (see “What’s that Plateau?” in [12] for an example). When a device is attached to a stub, the length of its lead and bond wire can
make the true length of the stub much greater than it appears from the PCB layout – so that it may no longer be able to be treated as a simple capacitive point load.

9 Simulators and solvers help design matched transmission lines

Part 1 of this series shows that where it is very important for commercial success to get to market quickly with low-cost-of-manufacture products – the EMC of the PCBs needs to be good and ‘correct-by-design’. It is also important to realise, as Eric Bogatin often points out in his articles and presentations on SI [38], that any equations and formulae that can reasonably be written down and worked out with a calculator are only useful for first-order approximations, initial order-of-magnitude design estimates, and ‘sanity checking’ the results from computer-aided design tools.

This article shows that designing and matching transmission lines with the accuracy required for good SI when using modern digital ICs and high data rates, and for good EMC, requires attention to a great deal of detail. People aren’t good at handling such detail – but computers are. Without appropriate computer aids (and measurement technologies such as TDR, see above) it is normal for at least two PCB iterations (re-spins) to be required to achieve the desired EMC performance at low cost, but the time this takes is becoming an increasing problem for commercial success. Many designers wind up sticking extra shielding and filtering onto their products in a panicky attempt to hit their new product’s market window – regardless of the cost.
It is probably impossible to design (for example) a PCB that uses 2.5GHz serial interconnections and get its SI and EMC right enough first time, without intelligent use of computer-aided design tools, including at least a 2D field solver (maybe a 3D one). But such computer aided design tools are now available, and getting much more useful every year. Now we can solve all (or most) of our detailed design issues in the virtual world before laying out and making the first PCB.

Computer-based simulators for calculations of PCB transmission line impedance have been available for many years, but user-friendly simulators that run on standard PCs, deal with the detail we require, and give reliable answers are now becoming available. A number of companies offer such products, but the ones that seem to be mentioned most in papers presented at EMC conferences are from Polar Instruments [23], Hyperlynx (e.g. available from Mentor Graphics) and Ansoft (Google easily finds their websites).

A new product called EMI Stream works at the component placement design stage (pre-routing), and claims to help find optimal placement locations and optimal routing for good EMC. It also claims to help suppress resonances between power and 0V [40].

Ideally, we would want to be able to extract accurate trace parameters from a simulation of a PCB layout that addresses all of the detailed issues discussed above; use those parameters in a circuit simulations, and iterate between the PCB layout and the circuit simulator until SI requirements are satisfied (as discussed in Part 1 of this series [6]). Then we would want to simulate the EMC characteristics of the whole PCB in its final assembly and predict what its emissions and immunity were going to be when measured with an antenna at 10m.
Unfortunately, not all of the tools required to do all this exist – or if they exist they don’t yet permit a fully ‘joined-up’ virtual design process. An example of good practice and use of computer tools that were current in 2001 is given in [11]. However, computer-aided design tools that exist at the time of writing do permit complete virtual design of SI. Since high-frequency SI and EMC are essentially the same issues [7], we can use SI design tools with tougher SI requirements than are needed for functionality to improve a PCB’s EMC characteristics.

At the time of writing, it is strongly recommended that – if the time it takes a signal’s edge to travel along the full length of the trace (the trace propagation time, \( t_p \), see above) is longer than 1/6th of the signal's rise/fall time (whichever is the shorter) – the entire signal path should be simulated. Simulation can use the transmission line facilities in IBIS or SPICE-based circuit simulators, or other types of simulator, to see whether a transmission line is needed for SI.

All clock and data strobe paths should always be simulated. They will almost certainly need to use a matched transmission line for good EMC, helping to reduce the need for expensive shielding and filtering.

Intel application notes recommend using a loss factor of 1.0Ω thou²/inch for copper in FR4. This is higher than the published figure of 0.662Ω thou²/inch for annealed copper, due to the additional surface roughness caused by pressure lamination and FR4’s woven glass-fibre substrate. If using non-woven substrates the standard published figure should be used instead.
10 EMC-competent QA, change control, cost-reduction

See section 8 of Part 3 of this series [19] for a discussion of this important issue.

11 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques – but in real-life there are a great many design compromises to be made, and this is where the circuit and PCB designers really earn their keep.

Designers are often put under cost or time pressure by managers who don’t understand the technical trade-offs, and so don’t understand that their actions could have the opposite effect to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of this series [6], plus the final section of part 2 [8].

12 References


August 1999, pages 185-194


Volume 4 – Safety of Electrical Equipment ISBN 1-902009-08-8


[31] John Lord, private communication, July 2002


13 Some useful sources of further information on PCB transmission lines

(These are not referenced in the article.)


Brian Young, “Digital Signal Integrity Modeling and Simulation with Interconnects and Packages”, Prentice Hall, 2001


California Micro Devices: http://www.calmicro.com/applications/app_notes.html or go to: http://www.calmicro.com then click on ‘Applications’ then click on ‘App Notes/Briefs’


LVDS: http://www.national.com/appinfo/lvds/


Note: On the Intel and IBM sites, to find application notes you must first choose a type of device.


Cypress Semiconductor Corporation, many useful application notes at: http://www.cypress.com

IEEE Transactions (www.ieee.org) on…
Electromagnetic Compatibility

Advanced Packaging

Components, Packaging and Manufacturing Technology

Microwave Theory and Technology

IEEE (www.ieee.org) Conferences and Symposia on…

Electromagnetic Compatibility

Electrical Performance of Electrical Packaging

Printed Circuit Design magazine http://www.pcdandm.com/pcdmag/

CircuiTree magazine: http://www.circuitree.com

IMAP Symposia

DesignCon Symposia

Some free PCB transmission line calculators

http://www.emclab.umr.edu, click on ‘PCB Trace Impedance Calculator’

http://www.amanogawa.com, click on ‘Transmission Lines’, then ‘Java Applets’

http://www.mwoffice.com/products/txline.html

http://www.ultracad.com/calc.htm

Relevant standards


IPC-2141 and IPC-2251 from http://www.ipc.org

I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than the series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by
Todd Hubing’s staff and students at the University of Missoura-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; Howard Johnson of Signal Consulting, Inc., http://www.sigcon.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

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Advanced PCB Design and Layout for EMC
Part 7 Routing and layer stacking, including microvia technology

By Keith Armstrong C.Eng MIEE MIEEE

This is the seventh in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to…

- Save cost by reducing (or eliminating) enclosure-level shielding
- Reduce time-to-market and compliance costs by reducing the number of design iterations
- Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
- Use very high-speed devices, or high power digital signal processing (DSP)
- Use the latest IC technologies (130nm or 90nm chip processes, ’chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
A previous series by the same author in the EMC & Compliance Journal in 1999 "Design Techniques for EMC" [1] included a section on PCB design and layout ("Part 5 - PCB Design and Layout", October 1999, pages 5 - 17), but only set out to cover the most basic PCB techniques for EMC - the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC. Like the above articles, this series will not spend much time analysing why these techniques work, it will focus on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

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1 Routing and layer stacking techniques, and microvia technology

This part of the series is concerned with the business of routing the traces on the PCB artwork, etching and plating the copper foils, laminating the etched foils with layers of dielectric, and drilling and plating the via holes. All of these can have an effect on a PCB’s EMC.

Some of the relevant issues have already been discussed in previous parts of this series, in which case they will only be briefly mentioned here, with a reference to the earlier part. If you have missed any parts of this series, you can download them from the archive at http://www.compliance-club.com/keith_armstrong.asp or http://www.compliance-club.com/KeithArmstrongPortfolio.

But please note that the last two issues of the EMC & Compliance Journal are posted in full at http://www.compliance-club.com and articles are only placed in the archives when they are not in one of these - so if the part you want is the one previous to this, it might not yet have been transferred to the Journal’s archives.

2 Routing

Previous parts of this series have described a number of PCB component placement and routing techniques, for example -

a) Part 2 [6] discusses the segregation (partitioning) of components and their associated traces into different zones, and how to route the traces that must interconnect the zones. It also covers component placement and trace routing in filter zones, and when shielding cans are used on the PCB.

b) Part 4 [7] discusses the design of planes, and the routing of traces with respect to plane edges, and also with respect to any splits or gaps in a plane.

d) Part 6 [9] discusses routing techniques for traces that carry high-speed or high-frequency signals or noises - especially its section 3.1 and figures 6T-6W. It contains a lot about controlling trace characteristic impedance and propagation velocity, and when transmission line techniques are not required this may be ignored. But note that for good PCB EMC performance, transmission line techniques are increasingly required to prevent unwanted noises from causing emissions or immunity problems.

Most of the analysis of trace routing in the literature is based on reducing emissions. But by applying the principle of reciprocity, we find that the trace routing guidance that results in least emissions from traces (e.g. section 3 in [9]) also improves a circuit’s immunity to high-frequency noise present in its operating environment.

Matched transmission line techniques [9] are also an important technique for reducing emissions from traces (by reducing the amplitudes of the standing waves, making traces less effective as 'accidental antennas'). So this technique will also, by reciprocity, make traces less liable to pick up noise from their environment - helping improve the immunity of their circuits.

The above parts have covered everything I want to say about trace routing, except for how to design traces which need to carry transient or surge overcurrents and/or overvoltages, which are covered later on.

3 Stack-ups

The 'stack up' is the name given to the order of the various etched copper foil and dielectric layers that are laminated together under pressure and heat to make a PCB. Some of the earlier parts of this series have made recommendations that affect stack-ups, for example -

f) Part 4 [7] discusses techniques for dealing with the cavity resonances between planes in a stack-up, and what to do when traces must change layers along their route.

g) Part 5 [8] discusses decoupling using adjacent pairs of 0V and power planes, and its extension into what is often called 'buried capacitance'.

h) Part 6 [9] discusses stack-up techniques suitable for traces with specified characteristic impedances, and also for any traces carrying high-speed signals or noises. As mentioned in section 2 above, the same techniques are useful for improving a circuit’s immunity to radio frequency (RF) noise in the environment, by making its traces less effective 'accidental antennas'.

The above parts have covered all the details that I wanted to cover on stack-up design, except for the benefits of closer trace-plane spacing, closer component-plane spacing, copper balancing, and how to put all the techniques together and decide on the number of layers and the spacings between those layers. These remaining issues are covered below.

3.1 The benefits of closer trace-plane spacing

The EMC benefits of closer 0V-power plane pair spacing were described in [8], but there are also EMC benefits from having closer spacing between traces and planes. A significant cause of PCB emissions is the conversion of the wanted differential-mode (DM) signals into unwanted common-mode (CM) noise. The CM noise is then radiated from traces, planes, attached cables and other conductors behaving as accidental antennas. Because of reciprocity, the reverse process (CM to DM conversion) is a significant cause of susceptibility. The resulting DM noise in the PCB traces interferes with circuit operation, either directly or via demodulation or intermodulation in semiconductors.

But when a trace’s width becomes comparable with its spacing from a substantial plane, the CM-DM conversion ratio (and the DM-CM ratio) starts to reduce, improving emissions and
immunity. Now, if the trace-plane spacing is halved, or the plane dimensions are doubled, the CM emissions generally reduce by about a half (approximately 6dB). Continuing to reduce trace-plane spacing, or increase plane dimensions, causes the CM emissions to continue to fall proportionately.

This is a most desirable situation, and since many traces on PCBs are now in the region of 0.25mm (10 thousands of an inch, called 'thou' in the UK and 'mil' in the USA) to 0.18mm (7 thou), we should now be aiming to use trace-plane spacings with the same dimensions, or less. Ideally, the trace-plane spacings should be half the trace width, and the planes as large as possible. It may even be worth making a PCB larger all around and filling the extra border space with 0V plane (and nothing else) to improve EMC. This would have the added benefit of reducing the fringing fields, improving the EMC performance of the PCB even more.

Traditional PCB stack-ups use equal layer spacings, for no good reason, so the idea these days is to use unequal layer spacings. Of course, if a PCB has so many layers that equal layer spacings results in trace-plane spacings of around 0.15mm (6 thou) or less (e.g. a 1.6mm thick PCB with ten or more layers) then equal layer spacings might be able to be used.

A possible problem with very small trace-plane spacings is their effect on characteristic impedances of traces, discussed in [9]. When using smaller trace-plane spacings it becomes more difficult to achieve higher values of $Z_0$ without using very fine-line PCB manufacture, which might cost more. For example, a microstrip using a 0.2mm (8 thou) trace in 1oz copper spaced 0.15mm (6 thou) from its plane would have a $Z_0$ of about 58Ω, and to achieve more than 80Ω would require a trace width of less than 0.1mm (4 thou) using «oz copper.

3.2 The benefits of closer component-plane spacing
Reducing the spacing between the semiconductors in the ICs and a copper plane in their PCB allows the image-plane effect (see section 1 of [7]) to reduce the emissions and improve the immunity of the devices themselves.

Also, decreasing component-to-plane spacing reduces the lengths of the via holes between an IC or decap and its 0V and power planes, and also reduces the area enclosed by the current loop created by the decap and the device it is decoupling. Both of these are beneficial for decoupling (see section 2.5 of [8]) especially when very low-inductance decoupling current loops are required for controlling the noises emitted by modern digital ICs.

### 3.3 Copper balancing

An inequality in the ‘balance’ of copper in a PCB about the centre-line of its stack-up (e.g. 0.8mm through the thickness of a 1.6mm PCB) can cause the PCB to warp when put through the high temperatures of an automated soldering machine, or during long use at elevated operating temperatures. A warped board is bad because it can cause solder joints to fail prematurely, and it can even pull the terminals off large surface-mounted devices or pull the pins out of large leaded devices.

With lead-free soldering about to happen on a large scale, it should also be realised that a warped board applies mechanical stresses to its soldered traces and devices and this encourages the growth of tin whiskers, with 1mm long conductive whiskers being possible in such circumstances. Such tin whiskers are also a possible cause of unreliability (and maybe safety hazards too, see section 7.2 below).

The copper balance of a PCB depends on the percentage of the copper left unetched on each layer (a solid plane over the whole area being 100%), the finished thickness of the copper foil (after etching and any plating), and the distance of each layer from the PCB’s centre-line.
Calculating copper balance is like taking a balance beam with a central fulcrum and placing different weights at different distances from the fulcrum, so as to get the beam to lie horizontal (i.e. to be in balance). Some PCB stack-up management applications can calculate copper balance automatically, but it isn’t too difficult to do by hand for PCBs up to eight layers by using the ‘balance beam’ analogy - because the maths is so simple to understand.

Copper balance has traditionally been achieved by using equally-spaced layers and a symmetrical PCB (symmetrical construction about its centre-line). A symmetrical PCB is one that has mirror-image stack-up either side of its centre line, for example the following equally-spaced stack-up:

Layer 1 Signal
Layer 2 Signal
Layer 3 Plane

(Centre-line)
Layer 4 Plane
Layer 5 Signal
Layer 6 Signal

The signal layers in the above example would need to have the same copper thicknesses, and the PCB designers will add hatched or filled copper areas that have no circuit function to maintain the same copper percentages and achieve uniformity over their areas. The plane layers would use the same copper thickness.
To avoid having to determine how much copper fill was required to make all of the signal layers have a similar unetched percentage, some companies use symmetrical stack-ups and automatically fill all of the areas that would have been etched with non-functional copper - on all of the signal layers. Then all of the layers (including planes) can be treated as having the same copper percentage, so that copper balance can then be achieved simply by using equal layer spacing and an even number of layers.

Unfortunately, the use of hatched or filled areas can have bad consequences for EMC, as discussed in section 4 below.

The above copper balance methods are simply ways to avoid doing any work, and perfectly good copper balance can be achieved using unsymmetrical layouts with different copper percentages, thicknesses, and unequal spacings, at the cost of a little extra design effort and time. This enables the use of closer trace-plane spacings (see 3.1 and 3.2 above) and also helps to avoid the EMC problems caused by hatched or filled areas (see later).

3.4 Single-layer PCBs

These types of PCBs provide very limited control of the EMC characteristics of their traces. So they should never be used where any degree of EMC performance is required, except for...
circuits specially designed by someone who understands how to choose the components and design the circuit to compensate for the 'accidental antenna' effects of the PCB traces. They can be acceptable where the signal bandwidths are limited by design by passive filters, to less than a frequency that depends on the size of the PCB.

Figure 7B shows some general guidance based on the wavelength of the signal or noise being larger than 100 times the length of the trace, which might be able to provide acceptable EMC performance in some general-purpose household, commercial or industrial applications. Field solvers and circuit simulators are required to predict EM performance with any reasonable accuracy (see section 4 of Part 1 of this series [10] for more on this). Of course the good old fashioned method of designing, testing and redesigning can be used instead - if there is plenty of cash and time available - or if the design is being done by an EMC circuit and PCB design expert.

![Figure 7B](image)

Note that all semiconductors (except for the very largest power devices) will respond quite happily to frequencies in excess of 100MHz, either by direct interference with the wanted signal or by demodulating or intermodulating them to cause interference at other frequencies from d.c. upwards. Even very low-cost operational amplifiers with gain-bandwidth products of...
1MHz or less and slew rates of 1V/μs or less will happily demodulate at well over 1GHz. So only passive filters may be used to limit the bandwidths or rise/fall times of the signals in the traces of single-layer PCBs. (Note that a feedback capacitor from output to inverting input on an opamp is an active filter, and not suitable for any EMC purposes above 1MHz or so, depending on the opamp.)

Modern sub-micron digital ICs and RF devices are generally unsuitable for use on single-layer PCBs.

3.5 Two-layer PCBs

Two-layer PCBs can provide much better control of the accidental antennas that we call traces, if carefully designed. But it is very hard to make them achieve acceptable EMC performance when using modern digital devices with their very short rise/fall times.

Sections 2.3 and 2.7 of [7] discuss how to make a two-layer PCB achieve the best EMC performance they are capable of, preferably by using the 'solder side' layer as a solid 0V plane, or at least by creating a 0V mesh by creating a 0V fill on both sides of the PCB and 'stitching' them together with vias. And section 2.7 of [8] describes a ferrite decoupling technique that can be very effective on two-layer boards. These techniques will not be described again here.

As for single-layer PCBs, only passive filters may be used to limit the bandwidths or rise/fall times of the signals in the traces to make the EMC performance acceptable.

RF and microwave designers have traditionally used two-layer PCBs and had excellent EMC performance, but one side was always a solid plane and the single signal layer always used well-matched transmission lines. So it is also possible that modern sub-micron digital devices could achieve good EMC performance using two-layer PCBs by using the same techniques - but only if they could fit all of their signal routing into the one signal layer available.
So sub-micron digital ICs and RF devices are not generally suitable for use on two-layer PCBs. However, there are a small number of modern microcontrollers that claim to have been designed with EMC in mind for use in very low-cost products (e.g. for the automotive industry), such as the Fujitsu F2MC-16LX family, and these may be able to be used without matched transmission lines, and without solid 0V planes so that they can be fully routed can be achieved on a two-layer PCBs.

As for single-layer PCBs, field solvers and circuit simulators are required to predict the EM performance of two-layer PCBs with any reasonable accuracy (see section 4 of [10]). Of course the good old fashioned method of designing, testing and redesigning can be used instead - if there is plenty of cash and time available - or if the design is being done by an EMC circuit and PCB design expert.

3.6 Four-layer PCB stack-ups

The state-of-the-art for the majority of commercial products during the 1980s, and still capable of providing adequate EMC performance throughout much of the1990s - the four-layer PCB can still provide adequate EMC performance (if carefully designed) with digital devices based on IC design rules at least one generation larger than 150μm.

Figure 7Ci shows a typical equally-spaced four-layer PCB stack-up of the 1980s, which obtains some decoupling benefits from the distributed capacitance of its embedded 0V/Power plane pair.
Some designers prefer to place the two planes on the outer layers, and reserve the inner layers for signal traces, as shown in Figure 7Cii. The idea is to shield the traces, but even with a via or decap wall around the PCB’s perimeter [8] (which is not usually incorporated) the plane on the component side would be badly perforated by the pads and pin-escapes for the devices, and so incapable of providing high levels of shielding.

Some useful shielding might be achieved with careful design (and a via or decap wall) but this must be balanced against the fact that when using a 0V and a power plane - they are so far apart that they no longer provide any appreciable decoupling benefits from their distributed capacitance. Whether the result would be better than the stack-up with the embedded planes would need a circuit simulator combined with a field solver to predict.

Another issue with this ‘planes on the outside’ stack-up is that it is very difficult indeed to hand-modify traces on prototype PCBs during development. Some companies would make all their prototype PCBs using an embedded pair of planes, changing to external planes for the production version once all the development was (hopefully!) complete. Of course, this stack-up change could make a significant change to the EMC performance of the PCB, and
alter the characteristic impedances of the traces, making the assumption of "no further changes required" more risky.

The traditional stack-ups shown in Figures 7Ci and 7Cii are both symmetrical, and both use equally spaced layers.

Figure 7Di shows a stack-up using unequal layer spacing to try to improve decoupling through the use of embedded capacitance. The 0V/power plane pair must be aligned on the centre-line of the PCB otherwise it is impossible to achieve copper balance and board warp can occur - but the problem is that the outer (signal) layers are now so far away from their reference planes that their EMC characteristics are not so good.

Figure 7Dii shows a stack-up recommended by Intel for low-cost PC motherboards in the late 1990s, which also has a symmetrical stack-up but uses unequal layer spacings to reduce the trace-plane spacings for the outer signal layers, so they can handle high-speed digital signals with better signal integrity (SI). This stack-up is suitable for mounting 1990s technology digital ICs and their high-speed traces on both sides, but the 0V and power planes are so far apart that their distributed capacitance provides little benefit for decoupling. Good SI and good EMC performance are closely related, as discussed in section 1.2 of [9] and [11].
It is worth noting that the typical desktop or tower PC cases in the late 1990s achieved a shielding effectiveness of about 50dB at 30MHz falling to between 15 and 35dB at 1GHz, so this four layer construction would probably not have complied with FCC or EU EMC regulations without such a shielded enclosure. It is also worth noting that high-performance servers and workstations based on PC technology in the late 1990s would have used PCBs with eight or more layers, and shielded cases. (And some people have reported them as experiencing lower levels of 'Windows crashes’ even when running the same operating systems and applications software, so maybe the SI of the four-layer boards was not the best).

3.7 Six layer PCBs

A six-layer PCB gives more design flexibility than a four-layer, but it takes some work to make it ideal in EMC terms. Figure 7E shows a traditional symmetrical stack-up with equally-spaced layers, which has no EMC advantages over the equivalent 4-layer PCB - it just has two more layers for signal routing.

![Figure 7E A symmetrical 6-layer board stack-up with equally spaced layers](image)

Using an unequally-spaced stack-up as shown in Figure 7F has the EMC and SI advantages of the Intel recommended design shown in Figure 7Dii, with the advantage of two internal
offset stripline layers. To maximise the EMC potential of this stack-up, the traces on the outer layers should be kept short and all high-speed signals or noises routed on the inner signal layers. Unfortunately, like Figure 7Dii, this stack-up has very little distributed capacitance between its 0V and power planes.

Using an *unsymmetrical* stack-up with unequally-spaced layers as shown in Figure 7G can improve the EMC of the previous design (Figure 7F), at the cost of one less signal routing layer and more effort required to achieve a copper balance. The 0V and power plane pair are placed very close together to maximise their distributed capacitance, and they are located close to layer 1 so that devices mounted on this side have less decoupling inductance (see 3.2 above). The bottom layer has been made a 0V plane so as to retain the two offset striplines.

This stack-up is best when used with components mounted on its top side only (the layer 1 side), or with double-sided assembly where the bottom side is used for passives or slower devices and/or signals. Note that the decaps for the ICs on the top side, should also be mounted on the top side, to minimise decoupling inductance.
3.8 Eight layer PCBs

The eight-layer PCB is the only symmetrical stack-up that can meet all of the EMC requirements for a stack-up without requiring a lot of design effort. It will also support fast devices on both sides, which six-layer stack-ups with equivalent EMC performance (e.g. Figure 7G) cannot do.

Figure 7H shows a traditional design using equal layer spacings, with four signal layers and two pairs of 0V/power plane pairs. The best routes for traces carrying high-speed or high-frequency signals or noises is on layers 4 or 5, the offset striplines, so traces carrying all such signals or noises on layers 1 or 8 should be kept as short as practical.
If the PCB is 1.6mm (64 thou) thick, the spacings between the layers might be small enough (0.23mm, 9 thou) to achieve enough improvement due to closer trace-plane spacing, significant distributed capacitance, and low decoupling inductance. But significant improvements are possible by using unequal layer spacings whilst retaining the symmetrical stack-up (which makes design very easy) and an example is shown in Figure 7J.

The stack-up shown in Figure 7J can be made optimal for EMC and SI, and is highly recommended as the starting point for all designs that use modern digital devices.

3.9 PCBs with more than eight layers
The eight layer design shown in Figure 7J (symmetrical, with unequal layer spacings) can be
designed to be optimal for EMC and SI, and adding extra layers does not add any extra EMC
benefits.

The two closely-spaced 0V/power plane pairs, each spaced very close to the outer layers to
aid decoupling, can provide all the decoupling that is required (apart from bulk capacitance) if
they are made into real embedded capacitors by the use of high-k dielectrics and/or very close
plane spacings (see section 3.14 of [8]).

So extra layers are simply a routing issue, and they can all be signal layers with additional 0V
planes as required, to help control trace characteristic impedance and crosstalk. These extra
layers should fit between layers 3 and 6 on Figure 7J, so as not to upset the excellent
decoupling provided by the 0V/power plane pairs for the ICs soldered to the top and bottom
layers of the PCB.

3.10 Number of PCB layers and cost-effective design in real-life

More than 50% or the world’s production of PCBs now use 6 or more layers, and they are
used in personal computers and cellphones that cost much less than equivalent products -
using simpler PCB technologies - did years ago. So when anyone complains about the cost of
extra PCB layers, or of the use of more modern PCB technologies (e.g. HDI, see later) - they
should generally be sent for re-training.

I recently used an eight-layer stack-up similar to the one shown in Figure 7J to reduce
emissions in the 700-900MHz range by over 20dB, for a PCB that originally had six layers.
The manufacturer had laboured for over 9 months to try to reduce these emissions to achieve
EMC compliance, using filters, shielding, etc. - but simply replacing the PCB with the
eight-layer version was sufficient on its own to create the required improvement. The extra
cost of the 'bare board' turned out to be minimal, especially when compared with the extra costs that the less effective filtering and shielding would have required.

It is often the case that designers don't consider increasing the number of layers in a PCB because of the intense pressure on 'BOM cost' from their managers (BOM = bill of materials). But, as explained at some length in Part 1 of this series [10], it generally makes the very best economic sense to solve EMC problems at the lowest level of assembly, and after the ICs themselves, this means solving them at the level of the bare PCB. Even if the bare board costs more in volume manufacture, due to additional layers, the real-life cost saving from a correct PCB EMC design will generally be at least ten times the bare board's extra cost. The profitable selling price of a product is not determined by simply multiplying the cost of its BOM by some pre-determined number (see section 1.2 of [10] for more on this). This issue is so important that Figure 1B from [10] is repeated here as Figure 7K.

When a company is using six or fewer layers in their PCBs and a designer is considering adding extra PCB layers for EMC or SI reasons, the designer generally asks his company's buyer to get a quotation for the bare board. The resulting quotation is often as much as double the price of the existing board, which frightens off the project manager (even though it may still
be very cost-effective in real-life) because most of them treat the lowest BOM cost as some sort of holy quest.

But it is important to realise that except for PCB manufacturers that specialise in low-volume work, all PCB manufacturers specialise in the number of PCB layers they aim to make most cost-effectively. So the PCB manufacturing plants are optimised for single-sided, double-sided, four-layer, or six-or-more layers. Each plant will only be able to give the best quotation for PCBs with the number of layers that their machines and processes are optimised for.

So now we can see why the request to the company buyer came back with such a high price for the extra layers - the buyer simply asked his existing PCB suppliers. To get the correct price for a PCB with added layers generally means discovering new PCB manufacturers whose plants are optimised for that number of layers, and asking them for a price. For example, in high volumes a bare four-layer PCB typically costs up to 25% more than a double-sided board that is otherwise identical. But most buyers do not know this, so make sure to tell them.

Adding 0V and power planes and thereby increasing the number of layers in a PCB is one of the most cost-effective EMC measures available, yet it is often ignored or denied due to buyers’ lack of knowledge of PCB manufacturing, and project managers’ short-sighted focus on BOM costs and lack of understanding of the real-life costs associated with manufacturing a product.

**4 EMC issues with copper balancing using area fills or cross-hatches**

As mentioned earlier, a copper imbalance in a PCB can cause it to warp when put through the high temperatures of an automated soldering machine, or during long use at elevated ambient temperatures. This is bad because it can cause solder joints to fail prematurely. It can also
encourage the growth of tin whiskers when using lead-free components and soldering - another cause of unreliability (if not safety hazards, see section 7.2 below).

Hatched or solid-filled copper areas, that are non-functional, are generally used to create a more uniform copper balance over the area of a PCB layer, and also used to increase the total unetched percentage of copper in a layer. These are usually called ‘poured grounds’ or ‘ground fills’, when they are connected to the 0V. Because planes are solid (mostly unetched) copper their copper percentage is close to 100%. Because it has been traditional to create symmetrical PCB stack-ups with equal layer spacings, in some companies the practise has arisen of automatically performing a copper fill on every layer so that they all have a similar overall percentage to that of the plane layers. Then copper balance is automatically achieved without anyone having to think about it.

Apart from the fact that any PCB design practices that are used without understanding and regular review are potentially bad practices - automatic copper fills can be bad for EMC.

One EMC problem is that the hatched or filled (poured) areas can resonate and increase emissions and/or worsen immunity. This can be solved by connecting each hatched or filled area directly to the PCB’s solid 0V plane (or power plane) by at least one via every λ/10 - where λ is the wavelength of the highest frequency of concern, taking the dielectric constant of the PCB’s dielectric into account.

For example, if the highest frequency of concern is 1GHz, and the PCB is using FR4 dielectric (relative dielectric constant above 1MHz = 4.2), the λ of the 1GHz signal or noise inside the PCB is 150mm, so the hatched, filled or poured copper areas should be via’d to a solid 0V plane at least every 15mm. More frequent 0V via connections will be better for EMC.

Sometimes the hatched or filled areas are intended to reduce crosstalk, but they will only do that effectively if they are via’d to the PCB’s solid 0V plane as described above for EMC.
The other EMC problem with hatched and filled non-functional copper areas is their effect on the characteristic impedance of nearby traces - which can be bad for both SI and EMC. I've seen examples where traces travelled into PCB areas where there were more areas of copper fill nearby, and their $Z_0$ fell by about 30% as a result. In the case of differential traces, differing amounts of copper fill on each side causes imbalances in the line, which is also bad for SI and EMC (see figure 6AG of [9] and its associated text).

The copper hatching and filling is usually the very last thing to be done to the layout before being sent for manufacture, and sometimes it may not have been present on the layouts that were reviewed by the circuit designer, or tested in prototypes. The assumption seems to be that the copper hatching or fill has no electrical effects, it is just a device to prevent board warp - but this is very far from correct.

Howard Johnson says that he doesn't use copper fills at all in multi-layer boards [12]. But they can be used, if their EMC and SI effects are understood and accounted for.

5 HDI PCB technology

5.1 What is HDI?

High Density Interconnect (HDI) PCB technology is also known as: 'microvia', 'sequential build-up' or simply 'build-up'. In this series I shall call it HDI, following [13]. It is based on the use of via holes of 6 thou (0.15mm) diameter or less, which can go between layers in a PCB without needing to go through all of the layers. These are generally called 'microvias', and they can be 'buried' or 'blind'.

Microvias are created by drilling and through-plating the vias between each adjacent pair of copper layers separately, before they are laminated together to create the finished PCB.

When the end result is a via that only connects between internal copper layers, it is called a buried microvia. When the result is a via that connects to one outer layer of the PCB and not
to the other, it is called a blind microvia. Traditional drilled and plated all the way through the PCB vias can also be used along with buried and blind microvias. These basic features are shown in Figure 7L.

The way that microvias are created, they are always closed off at one end, so they don’t ‘steal’ solder during reflow soldering. This allows via-in-pad layouts to be used, which saves PCB area and is very good for the PCB’s decoupling performance, because it reduces the inductance of the decoupling current loop.

HDI techniques can reduce the area of PCB required by 40%, reduce the number of layers by 33%, and be much easier to design than through-hole-plated (THP) PCBs [14]. HDI techniques help to make the smallest, lightest, and least power-hungry products, and can be found in a wide variety of common products, such as cellphones and even some toys. Some high-reliability products use HDI because microvias are more robust than vias that are drilled and plated right through a PCB. A comprehensive review of HDI and its benefits can be found in [14], and the basic standard for the design of HDI PCBs is IPC-2315 [13].

5.2 The EMC benefits of HDI

These include…
- via-in-pad reduces decoupling inductance and increases decap resonant frequencies
- the shorter traces become efficient 'accidental antennas' at higher frequencies
- the shorter traces might not need to be treated as matched transmission lines
- the smaller PCBs resonate at higher frequencies
- HDI 0V planes aren’t as heavily perforated as those of THP PCBs so they have lower impedances (hence lower PCB emissions and better immunity); they provide a more constant return path inductance for improved Z₀ control of transmission-line traces. They also achieve more benefits from the image plane effect, and provide better shielding between the circuits on the top and bottom sides of a PCB (lower crosstalk).

The above are all very valuable for modern sub-micron ICs, especially where ball grid array (BGA) devices are used - when the use of THP PCB technology results in severe plane perforation under and around the device - exactly where good EMC and good SI require the most

HDI technology makes it easier to use modern small IC package styles, such as ...

- Miniature or Micro BGA
- DCA (direct chip attach)
- Flip-chip
- CSP (chip scale packaging)
- Tape Automated Bonding (TAB)

These small ICs, and the smaller PCBs they allow, can generally be made to have excellent SI and EMC because their thinner packages place them in closer proximity to the 0V plane in the PCB, so the image plane effect is more powerful. Also, the smaller bond wires and lead frames means they are less effective as accidental antennas at frequencies below their first resonance, and their first resonance is at a much higher frequency, so these devices tend to emit less from their bodies.

However, a problem with these very small devices is that they allow much higher switching edges and higher-frequency noises to be conducted into the PCB’s power distribution and signal traces, which can worsen emissions considerably. But they can generally be made to have better EMC than the larger devices they replace, if all of the recommendations in this series of articles are followed.
5.3 HDI suppliers and costs

The usual complaint when HDI is mentioned is that the BOM will cost more, making the products uncompetitive, but this is hardly ever true these days, for two reasons.

The first reason is that HDI PCBs in reasonable quantities should now cost less than their THP equivalents. A survey by the IPC in May 2000 found that HDI PCBs could be purchased for the same bare-board price as a ‘traditional’ THP PCB. More recently, Happy Holden said in [14] that HDI PCBs should cost less than the THP PCB required to do the same job.

Designing without using buried vias can help reduce HDI costs even more, and since HDI PCBs are smaller than THP and tend to consume less power - cost savings may be able to be made in other areas of the product, such as power supply or batteries, enclosure, etc.

The second reason is that focussing on the BOM cost instead of the real-life cost of manufacture is a commonplace economic error (this was discussed section 3.10 above).

I remember the same complaint about BOM costs being raised when double-sided PCBs were first proposed, then again when through-hole-plate (THP) was developed, then again when 4-layer THP PCBs were starting to become necessary, and yet again when 4 layers were no longer enough. The change to HDI from THP is no different. Where miniature BGAs with less than 1mm pitch, or when chip-scale, DCA, TAB or flip-chip devices are to be used - HDI is probably an essential technology for getting EMC-compliant products with low warranty costs to market quickly, and selling them at competitive prices.

5.4 HDI PCD design issues

HDI requires a different approach to PCB layout, and some PCB design techniques may not always be able to be used. There are now many PCB manufacturers using HDI (there were at least 62 in May 2000) and because many of them developed their machines themselves, their manufacturing techniques can vary and may need different PCB layout techniques. So always
ask the HDI PCB supplier you are thinking of using what PCB design rules and restrictions they require to be followed.

5.5 More information on HDI

Describing HDI PCB manufacturing technology and all of its ramifications is beyond the scope of this article. Useful and informative references include [13] - [29].

6 Current capacity of traces

6.1 Handling surge and transient currents

EMC is not only about radio frequencies, it is also about transients and surges. One of the issues that often arises is the ability of PCB traces to handle the transient and surge currents that flow in the various circuits or protection devices. When a conductor (wire or PCB trace) is required to handle a transient or surge current, we can use the following guide to calculate its maximum current.

\[ I = \frac{290 \times \text{CSA}}{\sqrt{t}} \]

Where...

- \( I \) = current in amps
- \( \text{CSA} \) = cross-sectional area of copper in sq. mm
- \( t \) = time (in seconds) to fusing (melting)

This guide is only valid for values of \( t \) up to 5 seconds. When the duration of the overcurrent is longer than 1 second, thermal convection and conduction effects start to become significant. These increase the current rating for the same temperature rise, but require a very much more complex equation.

Note that 1/2oz (finished) copper foil has a thickness of 17.5μm, 1oz copper 35μm, 2oz copper 70μm and 3oz copper 105μm. Multiplying the finished thickness of the copper foil by...
the trace width gives us its copper cross-sectional area (CSA), which can then be used in the above equation.

For example, a trace that is 0.18mm (7 thousandths of an inch) wide in 1oz (finished) copper (35μm), subjected to a rectangular current surge lasting 40μs, would have a maximum transient or surge current (before melting) of around 290A. The normal 'double exponential' unidirectional surge test waveforms used (e.g. in IEC 61000-4-5) specify their decay time at the 50% point - doubling this time approximates to a rectangular surge waveform with equivalent heating effect.

Underwriters Laboratories (UL) carried out some tests of their own [30], resulting in some guidance on the maximum current handling that would not result in an open-circuited trace. The guidance given by figures 7 and 8 in [30] seems to correspond pretty well with the above formula (but note that the horizontal axes of the graphs in its figures 7 and 8 say they are trace thickness, when in fact they are trace width).

But the above only considers the copper's transient or surge current carrying capacity. Copper can get very hot indeed before it starts to melt, and such high temperatures will damage wire insulation and PCB dielectrics, possibly causing delamination with consequent reliability problems.

Some suppliers publish transient current data for wires, typically for current surges with a 1s duration. A typical 1s rating for wire with a 0.5mm2 CSA and standard PVC insulation, with a normal operating temperature of 25øC, is 55A. This current will not raise the copper temperature above the standard PVC insulation's 160øC short-term temperature rating (standard PVC is rated 70øC for continuous use).
The transient current rating (for \( t < 5s \)) is proportional to the conductor’s CSA and inversely proportional to the square root of the duration, i.e. the current rating for duration \( t = (1s \text{ rating})/\sqrt{t} \).

In the absence of suitable guidance for PCBs we might choose the same guidance for PCBs made of FR4 and similar materials, since their continuous and maximum operating temperatures are similar to those of PVC.

Applying this guide to our example trace above - 0.18mm (7 thou) wide in 1oz (finished) copper (35μm), subjected to a rectangular current surge lasting 40μs - we find that when the normal operating temperature is 25°C it suggests that repetitive transient or surge currents of up to 100A should not cause damage to an FR4 PCB. Of course, this assumes that the transients or surges occur at a rate that allows the trace to cool down to 25°C after each one.

To protect a trace or PCB from an overcurrent that exceeds the values given by the above guides, we might want to use a fuse. But even the fastest fuses cannot respond in less than 10ms (which is a very slow transient or surge in EMC terms), and all fuses have tolerances on their operating speeds so it is important to design for the slowest one of the chosen type that might be fitted, as shown by the example in Figure 7M (which is for a wire and not a PCB trace, but the principle remains the same).
The melting temperature of copper is so high that any operating temperature up to 100°C would have little effect on the melting current rating. But the same is not true when we want to know the maximum current that will not damage plastic insulation or PCB dielectric.

When calculating the maximum permissible current for normal operating temperatures above 25°C, remember that the current allowed when the trace is at the maximum temperature of the insulation (e.g. 160°C) is zero, and that the heating effect of a current is proportional to the square of its value in Amps. So, in the above example, if the operating temperature was 60°C instead of 25°C, the maximum current that could be permitted before the trace temperature exceeded 160°C would fall from around 100A to around 86A.

High-temperature grades of FR4 and other dielectrics are available, and using them would allow traces to carry higher transient or surge currents than the above guide suggests. On the other hand, some types of PCB dielectrics have lower short-term temperature ratings than FR4, so they would require lower transient or surge currents than the above guide if they are not to be damaged by hot traces.

It is best to use 'UL Recognised' or 'UL Approved' PCB materials, especially to prevent safety hazards from fire, smoke and toxic fumes, so always obtain and check the UL Approval
certificate for the basic PCB material used (or other evidence). Some suppliers don’t always deliver what they said they would, so check that all delivered PCBs have the appropriate UL logo stamped all over them.

6.2 Maximum continuous d.c. and low frequency current handling

Like surge and transient current handling discussed above, the continuous current handling of PCB traces is far from being an exact science. MIL-STD-275 [31] and IPC-2221 [32] are the published guides most often referenced for the continuous current capacity of a trace versus its temperature rise, trace width; PCB structure; ambient temperature; etc., but they are now considered inaccurate and incomplete [33]. The IPC has a project underway to create a new set of guidelines in IPC-2152 [33] [34], but it is not yet published.

John R Barnes provides guidance on PCB trace ‘ampacity’ on pages 31-87 to 31-92 of his excellent reference book [35]. Other useful references are [36] [37] [38] and [39]. This issue is not discussed further here; see the references below for how to deal with them.

6.3 Voltage drops in the PCB’s power distribution

The voltage drop created as the d.c. current flows in the resistance of the power distribution system on a PCB (often called the IR drop) is also an important consideration in the design of a PCB. If a chip is operated on lower than nominal voltages, its noise performance can suffer and this can cause problems for EMC immunity and SI.

[40] says that for modern high-current low-voltage designs, it is becoming critically important to include package and board IR drop into the total noise budget of the system. This issue is not discussed further here.

6.4 Handling continuous RF currents
The traces associated with filters may have to cope with continuous levels of RF currents, with consequent heating effects. RF currents travel near the surfaces of conductors, due to the skin effect. The higher the frequency, the thinner is the thickness of the copper that is carrying the current. So as frequency increases the effective CSA of the copper decreases and the resistance increases, leading to a greater heating effect for a given RF current at a particular frequency.

Because they are continuous currents, the heating is dominated by conduction and convection losses (e.g. stripline gets hotter than microstrip (all else being the same) because microstrip benefits more from air convection). The proximity of a 0V or power plane in the PCB can make a big difference to the heat lost from a trace. So it is very complicated to calculate the maximum current of a PCB trace at a given RF frequency.

However, we can use the continuous d.c. rating of a trace (section 6.2) as a guide. If the skin depth at the frequency concerned exceeds the thickness of the copper trace, the d.c. current rating applies. But if the skin depth is less than the trace thickness, it is probably best to assume that the trace is only as thick as one skin depth.

The skin depth in plain copper is given by \( d = \frac{66}{\sqrt{f}} \) (\( d \) in \( \mu m \), \( f \) in MHz), for example: at 160MHz \( d = 5\mu m \), (much less than the thickness of 1oz copper at 35\( \mu m \)) - so we would apply the d.c. calculations above assuming a copper trace thickness of 5\( \mu m \), to calculate the temperature rise for a given current at 160MHz, or to calculate the maximum trace current at 160MHz.

6.5 A note on accuracy

Do not expect the above guides on current handling to be very accurate! It is probably best to limit the maximum currents to no more than 50% than they indicate, preferably less. When this current is not enough and a 'calibrated' simulator is not available, it is best to make a 'test
PCB’ with a representative trace structure and test and modify it until satisfied. EMC laboratories will be happy to provide surge or continuous RF test facilities. The test PCB should be made and tested very early in a project, to reduce project risks.

Where transient or surge currents lasting less than 1 second are concerned, heat conduction and convection are insignificant so the test PCB could consist of a single trace on the surface of the PCB. But this test PCB should use the correct copper thickness and trace width, and have a length similar to the final trace. Connecting the high currents to the trace needs to be done carefully to avoid problems at those points, so the trace should fatten to at least twenty times its width at both of its ends, and these wide ends soldered directly to connectors that suit the type of lead used by the transient or surge generator.

Where continuous currents are concerned heat conduction and convection are very significant, so the test PCB needs to have the correct structure (trace thickness, width and length; stack-up and dielectrics; spacing of all 0V or power planes, or embedded heatsinks; etc.), and the airflow and PCB operating temperature needs to simulate what is expected in the final product. The tested trace should have a similar shape (e.g. duplicating any sharp bends) but the layouts of the untested traces themselves don’t need to have any resemblance to the final PCB.

7 Transient and surge voltage capacity of layouts

7.1 Trace-trace and trace-metal spacing

The spacing between traces must be sufficient to handle the high voltages that arise due to transient and surge events. There is useful information on this in [30], but the definitive references are clause 2.10 and annexes G and S of EN 60950:2000 [41], which describe the minimum creepage distances and clearances permitted between traces for safety reasons.
Clause 2.10 of EN 60950 does not make it very clear that the surge voltages it assumes for mains supplies are based on equipment being installed in an area for which 'Overvoltage Category II' applies. Annex G gives the levels of surge voltages that are assumed for the various Overvoltage Categories, allowing us to relate transient and surge overvoltages to the minimum creepage distances and clearances specified by clause 2.10 of EN 60950:2000.

If you are not sure what levels of transient or surge voltages might occur on a mains supply, note that EN 60950’s assumption of Overvoltage Category II might be appropriate for most information technology equipment, but it is not necessarily true for equipment in general. Overvoltage Categories I, III or IV may be more relevant, and III and IV are associated with much higher levels of surge overvoltages (up to 8kV), for a given nominal mains supply voltage.

Note that compliance with the surge test requirements in EMC Directive immunity standards does not necessarily mean that equipment will actually withstand the surges it is exposed to in real-life use. 6kV surge voltages can be expected on all single-phase mains outlets between 3 and 300 times a year in the UK (depending on geographical location and on whether the mains supply is provided by underground or overhead cables) - and other countries are generally as bad or worse - so if you want to make reliable products and reduce warranty costs it will generally be necessary to test mains inputs with surges of at least 6kV, using the IEC 61000-4-5 or (better still) the IEC 61000-4-12 test methods.

6kV is approximately the voltage at which single-phase mains sockets throughout the world generally spark-over, acting as spark-gap protectors for the equipment they power. Mains distribution systems that are only fitted with three-phase sockets will probably have a ‘spark-gap’ effect at a higher voltage, due to the increased spacing of their terminals, so
equipment connected to such networks might need to withstand 10kV surges or more. For more on the real-life surge environment, see [42].

7.2 The EMC and safety problems caused by compliance with the RoHS directive

All the guidance on the voltage withstand ability of the gaps between traces, and between a trace and any other metal, is based on the use of '60/40 eutectic' tin/lead solder. But the RoHS Directive [43] bans the use of such solders in all equipment sold in the European Union from mid-2006. Many other countries are also planning to ban the use of lead in solder. Most companies are treating this simply as a supply-chain issue - just making sure that all their components and PCB soldering processes are 'lead free' - but the problem is that lead-free solders are based on tin, and they grow 'whiskers' over time. Lead was originally added to tin-based solder many decades ago to prevent the growth of 'tin whiskers', but now that it is being removed components and conductors will grow these conductive whiskers. Tin whiskers can short out conductors such as PCB traces, and can reduce the air gap between traces so that they will no longer withstand their rated voltages or transient or surge overvoltages.

A number of manufacturers have applied to the RoHS committee for exemption on the grounds of poor reliability caused by tin whisker growth, but as far as I know no-one has ever commented on the effect of tin whiskers on creepage distances and clearances required for compliance with safety standards such as EN/IEC 60950, EN/IEC 61010-1 or EN/IEC 60335-1 (see [41]) - or on their effect on the ability of a PCB to withstand transient and surge overvoltages for EMC purposes.

Tin whiskers can easily grow to 0.1mm long, and in certain conditions where mechanical stresses are involved, they can grow to 1mm. Since they grow from both conductors across a
creepage distance or clearance their net degradation of the voltage withstand of the air gap between conductors is doubled.

The iNEMI report [44] and various other documents show that using a solder based on an alloy of tin, silver and copper (SnAgCu) can - when using controlled manufacturing processes - restrict tin whisker growth to 0.01mm. Unfortunately, it is not known why SnAgCu alloy works so well, which is worrying because it has not yet been proven in all the various physical and climatic environments that equipment (and their PCBs) may be subjected to.

Tin whiskers have the potential to cost manufacturers a very great deal of money, so this article recommends that manufacturers ensure that -

i) all of the 'lead-free' components and 'lead-free' soldering processes they employ only use the SnAgCu alloy and processes recommended by [44]

ii) the minimum spacings between PCB traces (and any other conductors) recommended by [30] or required for safety compliance by the relevant safety standards (e.g. [41]) are increased by at least 0.02mm - preferably 0.05mm or more. If not following item i) - increase them by at least 2mm.

Note that the above applies not just for EMC, but also for safety compliance. (Complying with the minimum creepage and clearance requirements of the relevant safety standards will not protect your company from prosecution under safety directives or product liability if tin whiskers cause a safety incident.)

Where explosive atmospheres may be present, the increased possibility of sparking caused by tin whiskers compromising the air gaps between conductors is also a concern.

8 EMC-competent QA, change control, cost-reduction

See section 8 of Part 3 of this series [19] for a discussion of this important issue.
Note that PCB layouts should always be reviewed by the electronic designer, who should take all the responsibility for ensuring the layout is good for EMC. The only exception to this rule is when the person doing the PCB layout is competent in understanding EMC in PCBs and applying that knowledge effectively. As discussed in [10] - good modern PCB design for SI and EMC requires a great deal of knowledge and technical expertise and the ability to understand and use computer applications such as field solvers. The level of expertise required can be equal to, or greater than, what is required to design electronic circuits or write software.

9 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques - but in real-life there are a great many design compromises to be made, and this is where the circuit and PCB designers really earn their keep. Designers are often put under cost or time pressure by managers who don’t understand the technical trade-offs, and so don’t understand that their actions could have the opposite effect to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to part 1 of this series [6], plus the final section of part 2 [8].

10 References

[1] "Design Techniques for EMC" (in six parts), Keith Armstrong, UK EMC Journal, Jan - Dec 1999


Volume 4 - Safety of Electrical Equipment ISBN 1-902009-08-8


[18] "Microvias in Printed Circuit Design", Kevin Arledge and Tom Swirbel of Motorola Land Mobile Products Sector, available via the IPC website: http://www.ipc.org

[19] "EMI suppression using next generation PCB/MCM technologies", Darrel Webb of
Zuken-Redac, Electronic Engineering, March 1998 pp 84-86.

[20] "The HDI Challenge - there is more to consider than just microvias", Kevin O'Leary, Electronic Engineering, October 1999 pp 81-84


[27] "Microvias and RF - ready for 10GHz?", Ron Neale, Editor, Electronic Engineering, August 2000 pp 59-62


http://www.ce-mag.com


standards bodies in their national language (e.g. in English from BSI: http://www.bsi-global.com). Note that IEC 60950:1999 "Safety of Information Technology Equipment" and other versions of EN or IEC 60950, EN or IEC 61010-1 "Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements", and EN or IEC 60335-1 "Safety of household and similar electrical appliances - General requirements" also include similar requirements for creepage distances and clearances between PCB traces.

[42] "Handbook on EN 61000-4-5 - Testing and measurement techniques - Surge immunity test", REO UK Ltd, request a copy or download from the 'knowledgebase' at: http://www.reo.co.uk, or by going direct to: http://www.reo.co.uk/guides

[43] EU Directive 2002/95/EC on the "Restriction of the use of certain hazardous substances in electrical and electronic equipment" generally known as the RoHS Directive, download via the link at:
http://europa.eu.int/comm/environment/waste/weee_index.htm

[44] "Recommendations on Lead-Free Finishes for Components Used in High-Reliability Products, Version 3 (Updated May 2005)", iNEMI Tin Whisker User Group, download:

11 Some useful sources of further information on PCB transmission lines,
(These are not referenced in the article.)

Hall, Hall and McCall, "High Speed Digital System Design, a Handbook of Interconnect Theory and Practice", Wiley Interscience, 2000


Brian Young, "Digital Signal Integrity Modeling and Simulation with Interconnects and Packages", Prentice Hall, 2001


Also, the Xilinx Xcell on-line journal often carries relevant articles:

California Micro Devices: http://www.calmicro.com/applications/app_notes.html or go to: http://www.calmicro.com then click on 'Applications' then click on 'App Notes/Briefs'

Mentor Graphics: http://www.mentor.com, click on 'Technical Publications' UltraCAD:
http://www.ultracad.com

LVDS: http://www.national.com/appinfo/lvds/


Note: On the Intel and IBM sites, to find application notes you must first choose a type of device.

Cypress Semiconductor Corporation, many useful application notes at:

http://www.cypress.com

IEEE Transactions (www.ieee.org) on.

- Electromagnetic Compatibility

- Advanced Packaging

- Components, Packaging and Manufacturing Technology

- Microwave Theory and Technology

IEEE (www.ieee.org) Conferences and Symposia on.

- Electromagnetic Compatibility

- Electrical Performance of Electrical Packaging

Printed Circuit Design magazine http://www.pcdandm.com/pcdmag/

CircuiTree magazine: http://www.circuitree.com

IMAP Symposia

DesignCon Symposia

I would like to reference all of the academic studies that back-up the practical techniques described in this series, but the reference list would take longer to write than the series! But I must mention the papers presented at the annual IEEE International EMC Symposia organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing’s staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose
Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; Howard Johnson of Signal Consulting, Inc., http://www.sigcon.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.

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Advanced PCB Design and Layout for EMC - Part 8 - A number of miscellaneous final issues

By Eur Ing Keith Armstrong C.Eng MIEE MIEEE, Cherry Clough Consultants

This is the last in a series of eight articles on good-practice design techniques for electromagnetic compatibility (EMC) for printed circuit board (PCB) design and layout. This series is intended for the designers of any electronic circuits that are to be constructed on PCBs, and of course for the PCB designers themselves. All applications areas are covered, from household appliances; commercial, medical and industrial equipment; through automotive, rail and marine to aerospace and military.

These PCB techniques are helpful when it is desired to:

• Save cost by reducing (or eliminating) enclosure-level shielding
• Reduce time-to-market and compliance costs by reducing the number of design iterations
• Improve the range of co-located wireless datacomms (GSM, DECT, Bluetooth, IEEE 802.11, etc.)
• Use very high-speed devices, or high power digital signal processing (DSP)
• Use the latest IC technologies (130nm or 90nm chip processes, ‘chip scale’ packages, etc.)

The topics to be covered in this series are:

1. Saving time and cost overall
2. Segregation and interface suppression
3. PCB-chassis bonding
4. Reference planes for 0V and power
5. Decoupling, including buried capacitance technology
6. Transmission lines
7. Routing and layer stacking, including microvia technology
8. A number of miscellaneous final issues
This is the final part of this series, and I hope you have enjoyed reading it, or at least found some things in it that were interesting or useful.

A previous series by the same author in the EMC Compliance Journal in 1999 "Design Techniques for EMC" [1] included a section on PCB design and layout ("Part 5 - PCB Design and Layout", October 1999, pages 5 - 17), but only set out to cover the most basic PCB techniques for EMC - the ones that all PCBs should follow no matter how simple their circuits. That series is posted on the web and the web versions have been substantially improved over the intervening years [2]. Other articles and publications by this author (e.g. [3] [4] and Volume 3 of [5]) have also addressed basic PCB techniques for EMC.

Like the above articles, this series does not spend much time analysing why these techniques work, it focuses on describing their practical applications and when they are appropriate. But these techniques are well-proven in practice by numerous designers world-wide, and the reasons why they work are understood by academics, so they can be used with confidence. There are few techniques described in this series that are relatively unproven, and this will be mentioned where appropriate.

If you have missed any parts of this series, you can download them from the archive at http://www.compliance-club.com/keith_armstrong.asp or http://www.compliance-club.com/KeithArmstrongPortfolio. But please note that the most recent two issues of the EMC Compliance Journal are posted in full at http://www.compliance-club.com and articles are only placed in the archives when they are not in one of these - so if the part you want is the one previous to this, it might not yet have been transferred to the Journal’s archives.

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1 Power supply connections to PCBs

All PCB connectors carrying power and 0V should use adjacent pins for their power and 0V connections. If the connector is long, there should be a number of power/0V pin pairs spread along its whole length. If the connector is also wide there should be a number of power/0V pin pairs spread across its whole area.

Ideally there should be a power/0V pin pair adjacent to each signal pin, but given cost and space constraints this is usually only done for critical signals, such as high-speed (e.g. Gb/s) interconnections. Using differential pairs for Gb/s interconnections relaxes this constraint and allows one power/0V pair for every two or more signals. The lower the imbalance in the differential pairs (in their drivers, PCB traces, connector pins and external cabling, see [6]) the fewer power/0V pin pairs are required for a given number of signals, for a given level of EMC performance.
A decoupling capacitor (typically 10 - 100nF) should be placed between the power and ground very near to each power/0V pair of connector pins. Where the main power enters the PCB, a bulk decoupler should also be located. In the past bulk decoupling above 470nF was always done with electrolytics, but multilayer ceramics are now available with up to 100μF (with low voltage ratings) and they should be much more effective than electrolytics, as well as being smaller, more reliable, and reversible.

The above guide also applies to connections to cables, and also to inter-board connections. When used in a backplane type of assembly, spreading power/0V pin pairs across the whole area of each connector helps achieve a low impedance connection at radio frequencies (RF) between all of the planes in the assembly. In a mezzanine board type of assembly the same is also true, and it is also recommended to spread 0V connections all around the edges of the daughter/mezzanine boards (and maybe over their areas too). This also helps control cavity resonances (as discussed in section 6 of [7]).
Where there are multiple power supplies associated with a signal, as in some analogue designs (e.g. +/-15V), the above guide applies but instead of power/0V pin pairs they should be power/0V pin triples (e.g. +/-15V and 0V). For more on off-PCB interconnections and EMC see [8].

2 Low-K dielectrics

Homogeneous substrates (as opposed to epoxy-glass substrates such as FR4) generally have a lower dielectric constant (‘k’) than FR4, and also a lower loss tangent. Examples include pure polymer, and liquid crystal polymer (LCP). Teflon (and even foamed Teflon) substrates are sometimes used where very low k is important, but the softer the substrate the harder it is to process in a PCB assembly. The lower k makes the velocity of propagation higher than FR4, and the lower losses make it possible to send high frequency signals further and still maintain good SI.

The EMC benefits of low-k substrates mainly resides in the lower levels of imbalance that can be achieved with differential pairs, see section 5.2 of [6]. Higher impedance lines use thinner traces, but when using thin layers of substrate the trace width can be too small for low-cost manufacture. Lower-k dielectrics use wider traces for the same characteristic impedance (all else being equal) so can make it easier or less costly to use higher impedance transmission lines. As well as being useful in their own right, higher impedance transmission lines have lower currents flowing in them, so their emissions are lower.

The use of low-k substrates has been commonplace in microwave applications (e.g. satellite communications) for decades. As signal speeds increase it has been expected for a long time that the use of low-k substrates would migrate to more mainstream PCBs, particularly PC motherboards and cellphones, but so far designers have been clever enough to find ways to
keep on using low-cost FR4 and its cousins. Figure 8B shows the relationship between SI, substrate loss tangent, and trace length.

When signals are 10Gb/s or more, [9] shows that traces 600mm long or longer on glass-fibre substrates like FR4 will have serious SI and/or EMC difficulties. Section 5.2 of [6] and its Figure 6AK shows a method of using one or two layers of homogenous dielectric to gain their benefits in an otherwise low-cost PCB.

Although it is not the intention of this series to deal with SI issues, Figure 8C shows an interesting comparison of crosstalk versus trace-to-trace separation between FR4 and LCP.
3 Chip-scale packages (CSPs)

These very small IC packages [10] can generally be made to have excellent SI and EMC because their thinner packages place their silicon in closer proximity to the 0V plane in the PCB, so the image plane effect [11] is more powerful. Also, their much smaller internal interconnections means they are less effective as accidental antennas at frequencies below their first resonance, and their first resonance is at a much higher frequency, so these devices tend to emit less from their bodies.

However, a problem with these very small devices is that they allow much higher switching edges and higher-frequency noises to be conducted into the PCB’s power distribution and signal traces, which can worsen emissions considerably. I know of someone using a CSP with a clock frequency of 1kHz, that exceeded the emissions limits all the way up to 1GHz (the one-millionth harmonic of its clock). But they can generally be made to have better EMC than the larger devices they replace, if all of the recommendations in this series of articles are followed.

4 Chip-on-board (COB)
In COB, bare silicon die (chips) are glued onto a PCB and wire-bonded to gold-plated PCB pads, then 'blob topped' with epoxy resin or silicone for protection. This is a very low-cost PCB assembly technique most often used on PCBs for high-volume low-cost consumer products, or for very rugged and reliable products. But despite its small PCB footprint, low cost (in volume) and ruggedness, COB seems to be ignored by most other product designers.

The small size of COB and its close proximity to the 0V plane in the PCB means it has better EMC, but if they still need to be shielded they can use small shielding cans as described in [12]. However, it may be easier and less costly to shield a COB by printing conductive ink over the top of its 'blob-top' protection. The size of the shield formed in this way is usually so small that internal resonances only start above 10GHz, and there are no apertures in it (above the surface of the PCB), so its shielding effectiveness can be very high up to many GHz. See [12] for more on shielding on PCBs.

**Figure 8D**  
*Shielding a chip-on-board (COB) with conductive ink*  
(a cross-section through the perimeter 'via-wall')

5 Heatsinks on PCBs

5.1 EMC effects of heat sinks
The stray capacitance between a metal heatsink and the IC or power semiconductor it is cooling injects stray noise currents into the heatsink, when the voltages in the IC or power transistor fluctuate. As a result, a floating heatsink experiences a fluctuating noise voltage, giving rise to electric field emissions. Since heatsinks can be quite large, and tend to be quite high above the 0V plane in their PCB, they can be very efficient radiators of emissions.

Inside the IC or power semiconductor, the stray capacitance to the heatsink arise from its bond wires and lead frames, maybe even (at above 1GHz) from its silicon metallisation patterns. Many types of power transistors connect one of their terminals (e.g. collector, drain, anode) to their metal tabs or metal body, and the stray capacitance between these relatively large areas of metal and the heatsink they are mounted on can be as much as 100pF.

If the heatsink is connected to a reference voltage, it will inject fluctuating currents into it, and also experience a fluctuating voltage depending on the impedance of the connection and magnitude of the current. If the reference voltage is not the correct one for the purpose, the noise currents injected into it in this way can cause self-interference or give rise to more emissions.

The electric fields from the heatsinks can radiate directly, causing problems with radiated emissions, and they can also couple with conductors and metalwork to cause problems for conducted emissions. If a heatsink causes emission problems, immunity problems might arise from external electromagnetic fields coupling to the heatsink, from where it might couple into the IC or power device. So reducing heatsink emissions can also improve immunity. Low-frequency analogue circuits that have no emissions above 150kHz might nevertheless need to use the heatsink techniques described here to improve immunity.
For good EMC (emissions and immunity) it is important to connect a heatsink to the reference voltage for the semiconductors that are actually causing the fluctuating voltages in the first place. In the case of an IC this is its 0V plane, and in the case of a power transistor it is one of the voltage rails that it draws power from, usually the one that is connected to the device via the lowest impedance. It is also important that the connection method, and the plane or power rail, have low impedance at the highest frequency of concern. It will be assumed in the rest of this section that the heatsink is connected to a copper reference plane in the PCB, as this is generally what is required to control frequencies above a few MHz.

This technique can be thought of as reducing the loop area of the stray capacitive currents that originally flowed from a conductor in the IC or transistor into the heatsink. (For good EMC, it is always best to return stray currents to where they originated, using the smallest path length and smallest loop area. The path length should be much less than λ/10 at the highest frequency of concern - the shorter the better.)

For all but the simplest heatsinks (e.g. rectangular blocks of metal) accurate analysis at up to 1GHz (or more) requires computer-aided simulation, taking into account:

- The heatsink’s geometry (shape)
- The types of semiconductors and their locations
- The proximity of any 0V planes and/or chassis
- The physical structure of any connection to a reference
- The physical characteristics of the reference it is connected to
The proximity of the heatsink to the actual source of the emissions (e.g. a silicon chip and its bond wires and lead frame)

The rest of this section will discuss these design issues in more detail.

5.2 Heat sink RF resonances

[13] and [14] contain a great deal of useful information on heatsink resonances, including guidance on heatsink shapes and device locations. Resonance effects only begin to occur when any dimension of the heatsink, or of the cavity (or cavities) it creates, exceeds \( \lambda/10 \) at the highest frequency of concern. When a resonant frequency happens to coincide with a signal frequency or its harmonic, emissions from heatsinks can increase by 30dB or more. The lowest resonance frequency is given by the half-wave resonance of its longest 'three dimensional' diagonal. For example, a 60mm cube heatsink should have its first (lowest) resonance around 1.4 GHz. [7] discusses cavity resonances between PCBs and chassis, and between two PCBs, and its design guidelines can also be applied to cavities created by heatsinks.

Square or cube shaped heatsinks tend to have the highest resonant frequencies in their structure, so are good if their lowest resonant frequency is well above the highest frequency of concern. But such symmetrically-shaped heatsinks tend to have a higher Q at their lower resonant frequencies, so can be problematic if these frequencies fall within the frequency range of concern (especially when they fall on the same frequency as a clock harmonic). To avoid this problem, make them rectangular, but not too long and thin, and avoid simple ratios of length : width : height (e.g. 1 : 2 : 3), as shown in Figure 8E.

Where heatsink resonances exist within the frequency range of concern, the best place for the IC or power transistor is generally in the centre of the heatsink’s base, which is usually best for
thermal performance too. Edge locations cause greater resonant gain and higher emissions. In the centre of a channel between fins is best until the channel itself resonates (but this is generally a much higher frequency than the base resonances). Vertical fins reduce the resonant gain (the $Q$) for the direction in which they run, so it is usually best for the fins to run along the longest heatsink dimension. Vertical pins increase the resonant gain of most/all of the resonant modes. See Figures 8F, 8G and 8H.
5.3 Bonding heatsinks to a PCB plane

Bonding heatsinks to a copper reference plane in the PCB (usually the 0V plane in the case of signal processing ICs), generally reduces emissions and increases the frequency of the lowest resonance [15], [16], [17], [18]. All such bonds should be very short and direct, and can usefully be combined with mounting hardware (e.g. short mounting pillars). Multiple plane bonds should be spread around the heatsink to reduce the bonding inductance and raise the heatsink’s resonant frequencies.
Low bonding inductance between heatsink and plane is very important - [16] found that radiated emissions increase with the inductance of the heatsink’s bonding network approximately to the power of 3.5. [16] also found that evenly distributed bonds are important - they can have 20dB lower emissions than if the same number of bonds are unevenly distributed but achieve the same overall inductance. Intel recommends [18] bond spacings of less than λ/4 at the 3rd harmonic of the processor core’s clock frequency (e.g. <25mm for a 1GHz clock) but I recommend less than λ/10 at the highest frequency of concern for heatsink emissions or immunity.

Figure 8J shows a computer simulation of the fields around an example heatsink when it is ‘floating’ (not bonded to anything), and Figure 8K simulates the same heatsink bonded to an infinite plane with four direct connections - one at each corner. The simulator used was FLO/EMC running on a modern PC, and although it calculated the three-dimensional field patterns for all of the frequencies from d.c. to 10GHz, these two figures just show the field patterns in one plane at just one frequency.
Figure 8L graphs the field strength versus frequency at a point above the heatsink, for the situations described in Figures 8J and 8K. The floating heatsink is clearly a very good emitter of fields from d.c. to 2GHz, plus it has a resonance at 5.32GHz; whereas with four bonds at its corners it has significantly lower emissions from d.c. to 1GHz and its lowest resonance is at 2.0GHz.

Figure 8L then goes on to simulate the same heatsink with eight and sixteen equally-spaced bonds. With eight it has significantly lower emissions than the floating heatsink from d.c. to 2GHz.
and its lowest resonance is increased to 3.75GHz. With 16 it has very much lower emissions from d.c. to 3GHz and its lowest resonance is further increased to 4.6GHz. Adding even more bonds would continue the trend: increasing the frequency of the lowest resonance; and reducing the level of the emissions below about 75% of that frequency.

Note that the simulation with sixteen bonds has a new resonance at 9.75GHz, peaking at about +12dB, which was not present in the others. It is not yet known what the physical cause of this is, but it shows the value of simulation in revealing unexpected results that could potentially cause problems, early in a project before any hardware has been made, when changes cost the least.

The above simulations employed 'direct' heatsink bonds assumed to have a resistance of 0Ω. Section 5.9 of [7] showed that, for PCB plane-chassis bonding, using resistive (lossy) bonds instead of 0Ω bonds reduced the amplitude of the resonant peaks at the cost of increased emissions below the resonant frequency. Figure 8M shows a simulation that explores whether the same trade-off might work for heatsink-plane bonds. It shows that with bond resistances of 25Ω and above the lowest resonance is almost completely damped, at the cost of increased emissions below the resonant frequency. Higher values of bond resistance result in higher emissions from d.c. up to the lowest resonant frequency, and lower emissions above that frequency. Using 50Ω ferrite beads instead of resistors for the bonds should restore the good emissions performance at the lower frequencies where the ferrites have a very low impedance.
These simulation results point to some interesting and useful applications, especially where it proves impractical to move the lowest heatsink resonance above the frequency range of concern. However, I know of no one who has yet tried to use resistive or ferrite heatsink-plane bonding in a real design so do not know if it is really as effective in real-life as the simulation implies.

Some processor sockets may now be available with built-in heatsink grounding posts for heatsinks, but in the main it is up to each designer to work with his electrical and mechanical engineering colleagues to come up with a low-cost solution that is easy to assemble on the PCB and does not consume too much board area. Figure 8N shows an example designed by Intel Corporation [19] - simply a metal stamping that solders to the PCB and makes spring-finger contact with the heatsink above the device (the hole in the middle is for the thermal transfer medium between the IC and heatsink).

It is relatively easy to design and make similar metal parts, and they will work well if designed with the right kind of springy metal, with plating to make a reliable electrical connection to whatever the heatsink is made of. Manufacturers of PCB shielding cans or spring-finger gaskets
should be able to recommend the best materials, and may also be the most appropriate manufacturers for them.

When designing methods of bonding PCB planes to heatsinks, be aware that the desired low impedance can be severely compromised by corrosion at any contacts between dissimilar metals, oxidation effects over time (especially with aluminium or steel), manufacturing residues or protective coatings on metal parts (especially anodising or passivation using insulating polymer coatings). Corrosion can be a big problem where condensation or other wetting by liquids can occur. Use appropriate techniques to ensure that all of the intended heatsink bonds maintain very low impedance contact despite the anticipated physical, chemical, biological and climatic exposures over the entire lifecycle.

In manufacturing always check that each batch of metal parts (heatsinks, fixings, etc.) have surfaces with very high conductivity, using smooth probes with low contact pressure. This is recommended because some manufacturers or platers of metal items do not understand surface conductivity specifications, and are liable to apply coatings of insulating clear polymer (which are invisible to the eye) on a whim. Also, some manufacturing buyers will purchase anodised
aluminium instead of alochromed aluminium, or polymer-passivated coated items despite what is written on the purchasing specification, because "it looks just the same: grey metal".

5.4 Combining shielding with heatsinking

Looking at Figure 8N, the next step seems obvious - design the part that connects the heatsink to the PCB so that it encloses the IC in a 'Faraday Cage' - shielding the IC and making even better bonding between heatsink and plane to give the best EMC performance at PCB-level. Shielding ICs at PCB level (as discussed in [12]) restricts airflow and can cause overheating, and combining shielding with heatsinking can solve this problem. An example of a suitable construction is shown in Figure 8P.

Figure 8P shows a metal structure surrounding the IC, with spring finger contacts top and bottom to make electrical contact with a 0V guard trace on the component side of the PCB (tinned and not covered by solder resist), and to make electrical contact with the base of the heatsink. Such metal structures are sometimes called 'picket fences' or 'picture frames'. The figure does not show any alignment or mounting pins on the picket fence, or how the heatsink is held in place.
There are many design possibilities for bonding the heatsink to the 0V plane all around the IC to make a shield: it could use a picket fence made of metal or plated plastic, soldered to the PCB at multiple locations instead of using spring fingers. If the IC has a low enough profile it could use a compressible conductive gasket or even a bead of conductive glue. It could be a metal structure that is welded or soldered directly to the heatsink, or formed as an intrinsic part of it.

To be an effective shield the picket fence (or whatever) must be continuous all around the IC, and must make frequent low-impedance electrical contacts to both the heat sink and a 0V ‘guard ring’ or plane on top of the PCB all around its perimeter. The 0V guard ring or topside plane must be via’d very frequently to the main 0V plane, all around its perimeter. The design guidance for the spacing of the contact points and of the vias are the same as for the PCB shields in section 2 of [12].

5.5 Other heatsink techniques that may help

Where practical, increase the flow of air (or other cooling medium) so as to be able to reduce the size of the heatsinks to increase their lowest resonant frequencies.

Use insulating thermal interface materials that have a lower dielectric constant and/or are thicker to reduce the amount of stray capacitance between the heatsink and the semiconductors’ silicon chips and bond wires [20].

Shielded thermal interfaces may be able to be used. These have two insulating thermally-conductive layers with a metal shielding layer sandwiched between them, and help to keep stray noise currents out of the heatsinks. The inner metal layer should be bonded directly to the appropriate plane, ideally at multiple places around its periphery to reduce emissions and increase its lowest resonant frequency, as discussed earlier for heatsinks.
When heat pipes are used, their length will generally give them lower resonant frequencies than equivalent heatsinks fitted directly to devices. Heat pipes should be bonded to the appropriate PCB plane as described earlier, along their length, to reduce their emissions at low frequency and place their resonant frequencies away from any clock harmonics or other strong signals in the PCB. Ideally, the heat pipe resonant frequency would be located higher than the highest frequency of concern, but this is often not possible.

The part of the heat pipe that collects the heat from the device is quite small, and so has much higher resonant frequencies - on its own - than the overall heat pipe (or an equivalent heatsink fitted directly to the device). So if it is difficult to bond the whole heat pipe assembly to the PCB plane or associated chassis (in turn well bonded to the PCB plane, see [7]) - it might be possible to bond the heat collector to a PCB plane as described earlier, then clip a ferrite around the heat pipe’s ‘pipe’ element to reduce the emissions from the larger part of the heat pipe’s assembly, as shown in Figure 8Q.

5.6 Heatsinks for power devices
The methods described in 6.2 to 6.5 above, have centred on heatsinks for ICs, but the methods described can also be applied to heatsinks for power devices.

Where there is no electrical isolation between a device and its heatsink (a low-cost method commonly used) the heatsink may need to be connected to the relevant power plane via a suitably-rated capacitor that provides the necessary galvanic isolation. The type and number of capacitors used, their location on the PCB, and their trace routing will have a significant effect on the heatsink bonding at higher frequencies, similar to the issues discussed for decoupling capacitors in [21]. With such 'live' heatsinks, electrical safety issues should always be taken into account in the design, (e.g. the total value of capacitance used may be limited to prevent electric shock, the capacitor may need to be safety-approved to Class Y1 or Y2) see Volume 4 of [5].

The heatsink tabs of power transistors can also be effective radiators of emissions even when an external heatsink has not been fitted. I once saw a low-cost inverter on a PCB not much more than 20mm square, with a single TO-220 power-switching device standing vertically above the PCB. The emissions from the TO-220’s metal tab caused the inverter to fail the generic emissions limits (conducted and radiated) over a wide range of frequencies, but of course it could not be connected to the reference because it was connected internally to the drain of the switching semiconductor. A capacitor of a few pF, from the tab to a suitable reference, solved the problem.

Power devices are often mounted along one edge of a PCB so that they can use the metal enclosure as a heatsink to save cost, as shown in Figure 8R. In this case the metal enclosure should be bonded to the main 0V plane in the PCB at multiple points, especially in the vicinity of the power devices. The purpose is to encourage the stray currents caused by the power devices to be returned to the PCB (and thence to all relevant power rails) with very low impedance at the
highest frequency of concern, so that (due to the skin effect) these currents remain mostly on the inside of the enclosure and do not cause external emissions. [7] deals with PCB-chassis bonding, so its design guidance is relevant here. The metal enclosure should ideally have no apertures or joints in the vicinity of the power devices and the nearby enclosure-PCB bonds, as the intense currents flowing in the enclosure in this area will make them 'leak' RF fields.

6 Package resonances

The frequencies that are now being used (e.g. radiocommunications, serial data, clocks and their harmonics at many GHz) plus the increasing requirements to test for emissions up to as much as 40GHz in some radiocommunication compliance, EMC compliance or military applications, means that semiconductor packages themselves can be large enough to resonate and become very effective 'accidental antennas' in their own right - even before a heatsink is attached (see earlier).

Eric Bogatin, in [22], says: "Know the resonant frequencies of all packages and change the package geometry if there is an overlap with a clock harmonic" and I don’t think it is possible to
improve on this advice. If it is not possible to avoid overlaps between the package resonances and the clock harmonics that are necessary for the functioning of the circuit, and if spread-spectrum clocking is not sufficient or not possible for some reason, then shielding is likely to be the only answer. [12] describes PCB shielding techniques - the lowest-cost way to provide shielding.

A 3-D field solver is required to accurately determine the resonant frequencies of packages in real applications, but it may be possible to roughly estimate the lowest resonant frequency using simple mathematics.

Chip-scale packaging (see earlier) provides the smallest possible package size. But where there are hundreds of contacts to be made to a device, affordable PCB technology might not be able to connect to them all because their contact pitch is so small. So HDI/microvia PCB technology [23] might be required simply to connect to the device, even if not to provide good EMC.

7 Eliminate the test pads for bed-of-nails or flying probe testing

Testing bare or assembled PCBs using ‘bed-of-nails’ or ‘flying probe’ techniques is a traditional manufacturing process that became common in the 1970s but is getting more difficult to employ as devices get smaller and the number of device pins rises. The test pads required for these test methods can seriously damage EMC, and may even damage SI causing functionality or reliability problems. And in many cases these test methods are no longer the most cost-effective.

It is very important for EMC that test pads are not added to every circuit node. Adding such pads can cause huge difficulties for the routing of high pin count devices such as BGAs (which are difficult enough to route anyway). But, more importantly, test pads on the end of traces act
as 'accidental antennas' just like any other conductor - but very few designers think to analyse
them to see if transmission line techniques are needed.

BGAs often end up surrounded by a forest of test pad accidental antennas, some of them using
very long traces when compared with the electrical lengths of the signals or noise present on
them. The stray capacitance associated with a test pad itself considerably increases the effective
electrical length of the trace that connects to it. The result is that test pads behave as
unterminated stub transmission lines (making them very efficient at damaging SI) and as
effective accidental antennas above 100MHz (compromising emissions and immunity). As a
rough example, a test pad with a trace length longer than 15mm will probably cause significant
SI and EMC problems below 1GHz.

Unless each test pad is analysed from a transmission line viewpoint for SI, the signals measured
by the test probes may be distorted and perfectly good PCBs may be sent for rework. Unless
each test pad is analysed and designed as a matched transmission line for reasons of good
EMC performance, such a PCB will probably require a great deal of costly shielding to comply
with EMC emissions requirements. But the cost of doing this and the PCB space lost to test pads
and their traces and terminators (where it is even possible to use them), makes it much more
likely that it will be more economical for products using modern ICs to scrap such 1970s
techniques and instead invest in good quality board manufacture.

However, there are well-proven PCB testing techniques that can locate faults without using test
pads. "Device-centric" boundary scan testing (JTAG, etc.) techniques [24a] now allow many/all
device faults to be located at the level of an individual component, using a PCB’s own address
and data busses and testing using only PCB’s functional connectors, even where some of the
devices on the board are not JTAG compliant. The 'Built-In Self Test' (BIST) facilities provided in
most modern VLSI devices and in the software of many systems can also be accessed with JTAG, extending the usefulness of the technique even further [24b] [24c].

Board rework is very costly and reduces the reliability of the PCB, leading to increased warranty costs. So even if JTAG is not available it can be more cost-effective to rely on built-in self test (BIST) and/or functional testing to check PCBs - and improve the quality of the circuit design, PCB layout, components and assembly so that the number of faulty PCBs becomes so low that it costs less to scrap the faulty boards than pay for bed-of-nails or flying probe testing.

I often come across companies whose purchasing departments insist on using the lowest-cost board manufacturers and assemblers, and lowest-cost component suppliers, thinking that they are saving their company money. But they do not consider that the overall costs of implementing the resulting bed-of-nails testing and reworking may be greater than what they saved by using such low-quality suppliers. In effect, they are 'saving money at any cost'. Marconi Instruments discovered in the 1980’s that despite suppliers’ claims to the contrary, there were known bad batches of components being sold as full-spec in the UK, and they were sold to the buyers who showed the least loyalty to their suppliers and drove the hardest bargains (surprise!). As in so many other areas of life, you get what you pay for. Although it clearly makes sense to reduce the cost of the bill of materials (BOM) - if in doing this the overall cost of manufacture (including the costs of warranty returns) is increased by more than the BOM cost savings, it is not cost-effective after all.

When the EMC problems of advanced PCBs are added, the cost balance shifts even further in the direction of eliminating test pads by using higher quality suppliers and manufacturing, and/or using JTAG design/testing techniques.
If test pads or connectors, or programming connectors must be used, it is important to add them to the PCB at its initial design, so that all of the functional and EMC proving is done with them in place (page 31-072 of [25]). In some companies the manufacturing departments add the test pads to the layouts after the PCB design is (supposedly) complete, but with modern semiconductor devices this can easily completely ruin the EMC, even if it doesn’t affect functionality.

Traces connecting to test or programming connectors have exactly the same EMC problems as traces to test pads, so should be treated exactly the same way. Any traces that were only needed during prototyping should either be removed before EMC testing begins, or treated with the same care for EMC as if they were functional traces. Such traces may need to be treated as stubs on transmission lines (see [6]).

Some companies design their prototype PCBs with huge numbers of additional traces that go off to an appendage whose sole purpose is to test most/all nodes on the prototypes. When judged ready for manufacture the ‘test appendage’ is simply cut off the PCB artwork, leaving large numbers of test traces reaching to the edge of the PCB. On a PCB that uses modern digital or RF devices, with their very fast signal edges and/or high frequencies, such a technique makes it impossible for the prototype PCBs to have SI or EMC that bears any resemblance to the manufactured PCB, and also makes it very difficult, if not impossible, to achieve good SI or EMC (for reasons that should be obvious to anyone who has been following this series of articles).

Even if the redundant test traces are completely removed from the layout, the layout that remains is generally less than ideal because its traces were originally laid out to fit in with the test traces. Usually at this stage in a project there is no time left to reroute the whole PCB and then retest its functionality and EMC. This whole technique is something that was possibly acceptable with the
slow devices and low frequencies of the 1970s or 80s, but is wholly inappropriate for modern electronic devices.

If the above technique must still be used, the traces and planes that are required for the functionality and EMC of the final design should be designed using the layers and stack-up they will have in the final product - taking all the guidance in this series into account. The test traces should then be added as additional PCB layers taking care to avoid crosstalk with the original traces. The 'test PCB' appendage should be cut off as early in the project as possible, and its associated test trace layers removed completely. Even if the 'test appendage' design is carefully done and transmission-line matching maintained (which it often is not) removing it will significantly alter the EMC performance, and could also alter the functional and SI performance. It is best not to use this technique at all with advanced PCBs (see Figure 1D in [26] for how to determine if a PCB requires treating as 'advanced').

Where a bus is provided for a cable (or a docking station), and when it is unterminated when the connector is not plugged in, or when the product is undocked - arrange for these clocks and data to be disabled when not required.

8 Unused I/O pins

Unused input pins should be pulled up or down, to prevent unintended oscillation, see page 31-28 of [25]. I have seen equipment behave like a Class C oscillator and radiate about 2W of RF power at 200MHz, simply because one section of an 'HC00' style inverter was unused and accidentally left with its input floating. Tying inputs directly to a rail might cause functional problems, or make fault testing difficult, so it is best to use a resistor of 10KΩ or so for pulling-up, and 200Ω or so for pulling down.
Some EMC engineers recommend programming any unused I/O ports to be outputs, with a 'strong' output driving capability, then programming them LOW and connecting them to the 0V plane to reduce ground bounce. Some could be programmed HIGH and connected to the power plane to reduce power supply bounce. Ground and power supply bounce is a problem for SI, and also a source of common-mode noise voltages and currents that increase emissions - so reducing them is a good thing.

But a problem can occur with this technique if, during booting-up or interference, the pin programming could be altered even momentarily, possibly causing high currents to be drawn from the power supply that could cause malfunction or damage.

9 Crystals and oscillators

Crystals and crystal oscillators should lie flat down on the PCB, close to their 0V plane and very far away from its edges (at least 15mm, unless they are placed inside a larger shielding can as discussed in [12]). Where the 0V plane layer in the PCB is not closest to the side on which the crystal is mounted, it helps to place an area of 0V plane on the component side underneath the crystal and extending at least 5mm around its outline on all sides. This small plane should be via'd to the main (solid) 0V plane at least every λ/10 at the highest frequency of concern, taking the dielectric constant of the PCB substrate into account (e.g. for up to 1GHz, vias in an FR4 PCB should be placed at least every 15mm over the whole area). It may help some devices if their metal can is soldered directly to the 0V plane by a very short wire or a U-shaped metal strap.

10 IC tricks
Although not PCB design techniques as such, it is worth mentioning that there are an increasing number of advanced EMC techniques becoming available in FPGAs and ASICs. These include:

a) Output drivers with user-programmable slew rates.
b) Output drivers with user-programmable drive ‘strength’.
c) Drivers that automatically adjust their output impedance to reduce the overshoot and ringing on their signals.
d) Drivers with built-in voltage-doubling and output impedances that allow ‘classical’ (both-ends) matching of transmission lines with no loss of signal amplitude.
e) Differential receivers with increased sensitivity that allow ‘classical’ (both-ends) matching of transmission lines with no problems caused by the 50% loss of signal amplitude.
f) ‘Dithered’ output switching that prevents outputs from changing state at exactly the same time (helping reduce ground bounce and rail collapse and CM noise in the PCB’s power structure).
g) On-chip, in-package, or in-multi-chip-module decoupling capacitors.

IC designers are constantly developing more techniques for improving the EMC of their devices, so when beginning a new ASIC of FPGA design always ask what is available. The lowest-cost place to control EMC is generally in the semiconductor devices themselves, even if they cost more as a result. Controlling EMC at PCB level is generally the next most cost-effective [26].

11 Location of terminations at the ends of transmission-lines

With the complexity of modern PCB layouts, it is sometimes difficult to locate transmission-line terminators immediately adjacent to the input or output pins of their receivers or drivers. [27] describes how to calculate if the resulting stub trace length is too great for SI, taking into account
the inductance of the bond wires and lead frame inside the devices themselves. For good EMC, the stub trace lengths should be at least one-third of the length that is required for good SI.

Some PCB manufacturers offer embedded resistive metal layers (instead of copper), which can be etched to create transmission-line matching resistors inside the PCB stack-up itself. It is much easier to place such terminators exactly on the pins of their devices.

Some devices now operate so quickly that the length of their internal interconnections is sufficient - on its own - to prevent good enough line-matching for EMC reasons, even when the termination resistors are placed as close as possible to their pins. There is always some overshoot and ringing caused by the ‘stubs’ internal to the devices. This can be another reason for using the smallest packages available, such as the chip scale packages discussed earlier.

12 Electromagnetic Band Gap (EBG)

Arrays of small copper squares, each connected to a large plane by a via as shown in Figures 8S and 8T, can reduce the propagation of some frequencies along a PCB plane (or in a cavity between two planes) by as much as 30dB. This technology is generally either called photonic band gap (PBG) or electromagnetic band gap (EBG), and the earliest reference that I have is [28] (which itself references earlier papers).
It requires a field solver or experiments to correctly assess the attenuation achieved by PBG/EBG structures, but I estimate that when using small square planes of side D as the elements of the PBG/EBG structure in a PCB employing an FR4 substrate, the useful attenuation occurs approximately over the frequency range 22/D to 42/D. D in millimetres gives frequencies in GHz, for example an array of 10mm squares creates useful attenuation over 2.2 - 4.2 GHz. Higher attenuation requires a larger area of PBG/EBG arrays.
PBG/EBG arrays can be used to reduce the noise or signals in one zone from flowing along a common plane to another zone, so might be able to be used all around the perimeter of a PCB zone, or around a ‘connector zone’, to help isolate one area from another as described in [12], or even as an alternative to the guard trace technique described in [11]. Do not use PBG/EBG to attenuate waves that are important for the operation of the circuit, e.g. preventing the 0V/Power planes from providing current at certain necessary frequencies. For more information on this new technology with potentially very significant possibilities, see [29] [30] [31] [32] and [33]. [34] explores the possibility of combining PBG/EBG technology with high dielectric constant thin films to improve the performance of embedded decoupling capacitance (section 3.14 of [21] discusses embedded decoupling).

The number of vias required to use PGB/EBG in a PCB implies that it would be easiest to use with blind or buried microvia PCB manufacturing techniques (see Part 7 of the series [23]). PBG/EBG technology either uses more PCB area, or an extra PCB layer, so will add to costs, but it does provide a method of controlling propagation and resonances at frequencies above 1GHz that could be more difficult and/or more costly by other means. I do not know of anyone using this technique in anything other than experimental PCBs so far, and would be pleased to hear of any experiences of using it in a PCB in a real product.

13 Some final PCB design issues

Unused traces should have any clocks, data or high-frequency signals on them disabled to reduce emissions, and if they connect to receivers they may need suppressing to improve immunity.
If a trace has to route to the other side of a microprocessor, RAM or other noisy device, it should circle around the device instead of cutting across its footprint (see page 31-72 of [25]).

14 Beware board manufacturers changing layouts or stack-ups

Board manufacturers routinely adjust layouts, to make them easier to manufacture with good yields. This usually means increasing the diameter of the clearance holes (antipads) around vias and through-holes, even if this cuts into nearby traces or creates large holes in planes when the antipads merge with each other. The tendency of some manufacturing buyers to only buy PCBs from the supplier that quoted the lowest price only encourages this practice. So it is important to always check the PCB suppliers’ final films after panelling [35], or check their preliminary unlaminated panels, to prevent the all-too-common situation depicted in Figure 8U or other unauthorised changes from causing problems.

I have seen PCBs modified without authorisation by low-cost high-volume PCB manufacturers to such a degree that they became unsafe. Of course, this was only discovered after a batch of 100,000 finished products using those unsafe PCBs had been delivered to the UK. The original designer’s identification and version numbers were left unchanged on the PCB, but the rest of the layout bore little resemblance to his design! I have also seen PCBs where the merged antipads effectively split the main 0V plane, intended to be continuous over the whole PCB, into two large planes connected only by a whisker of copper no more than 0.25mm (10 thousands of an inch) wide. The EMC performance of the products built with those batches of PCBs bore no resemblance at all to the ones that had been tested for EMC compliance, which had been made with the correct antipad diameters.
Oversized clearance holes or other unauthorised routing adjustments are more likely to occur on ‘production’ batches than on prototype PCBs. So if functional or EMC problems not present on the prototypes arise during serial manufacture - always suspect the PCBs. With PCBs of more than two layers, X-ray inspection might be required to see what is really going on inside a finished PCB.

PCB manufacturers sometimes add copper pads or areas to assist with copper balancing (see sections 3.3 and 4 of [23]) or for solder ‘thieving’ when using wave-soldering (page G-23 of [36]). These can upset the impedance of controlled-impedance traces, or unbalance differential lines (see [6] and section 4 of [23]). When a PCB is revised, the manufacturer might add the copper pads or areas in a different way, causing different problems. Where such additional pads or areas are required, they should be applied by the PCB designer and their impact on EMC taken into account.

Every aspect of a finished PCB must be under the complete control of its designers - no PCB manufacturer must be allowed to change anything at all without their carefully considered approval in writing. But even if this is written in the purchasing contract for the PCBs it is best to
assume it will not be followed, and insist on checking the final films or preliminary panels in every case.

15 Future-proofing the EMC design

Designs often suffer decreased EMC performance when they are no longer under the control of their original designers. This is especially a problem for ‘value analysis’ or ‘cost reduction’ projects - they should use people who are at least as knowledgeable and experienced as the original designers - but in practice usually use people with lesser skills who just delete anything they don’t see the reason for. This exact problem has cost at least one company their reputation for reliability, which took them decades to achieve.

In many companies, it does not help if the original designer writes technical reports about the EMC features of a design - because the people working on the next version or the cost-reduction either cannot understand them, or do not feel that they have the time to read them, or do not even bother to ask if such documents exist. We need to make sure that all of our good EMC work is 'future-proofed' so it is not wasted (at great cost to the company) when someone else becomes responsible for the design.

15.1 Marking EMC design features or critical parts on the design drawings

EMC features associated with the PCB design include such issues as multiple 0V return traces, additional 0V planes, routing constraints, PCB stack-up to achieve buried capacitance, etc. Components that are critical for EMC (but may not be for functionality) include multiple decoupling capacitors, transmission-line terminations, etc.
To help future-proof the EMC of a design it is very important to annotate all of the design features or components - that are needed for the EMC performance to be achieved - on the schematics, PCB design documents, assembly drawings, work instructions, and maybe on the parts lists (bills of material) too. In some cases all that will be needed is an adjacent 'EMC' symbol (maybe just an E), along with a footnote on each drawing page that this symbol means it is important for EMC. In other cases some instructions will be needed, for example: "These trace pairs must be routed symmetrically as striplines between two solid 0V planes along their entire length, on a single PCB layer."

At least this should warn the people who may be tempted to change those aspects of the design that they are messing with the EMC performance, so had better know what they are doing, or else expect to spend a lot of time testing and redesigning while they waste their employer’s money in large amounts learning the hard way about how to do EMC design properly. If you feel that a stronger warning is required (e.g. over a subtle design aspect that took a long time to get right - add it!

15.2 A quality-controlled procedure for EMC design

If an organisation has an effective QC system (e.g. ISO 9000), adding an EMC Design Procedure should help ensure that designers and others (e.g. 'cost-reducers') who take over other people’s projects or products do not destroy the good EMC performance they achieved. Such a design procedure will generally include requirements for identifying EMC design features and EMC-critical components as described above.

16 EMC-competent QA, change control, cost-reduction

See section 8 of [7] for a discussion of this important issue.
The electronic circuit designer, who should take full responsibility for ensuring the layout is good for EMC, should always review PCB layouts. The only exception to this rule is when the person doing the PCB layout is competent in understanding EMC in PCBs and applying that knowledge effectively. As discussed in [26] - good modern PCB design for SI and EMC requires a great deal of knowledge and technical expertise and the ability to understand and use computer applications such as field solvers. The level of expertise required can be equal to, or greater than, what is required to design the electronic circuits or write the software.

17 Compromises

It is easy to write an article like this and simply list all of the relevant good EMC design techniques - but in real-life there are a great many design compromises to be made, and this is where the circuit and PCB designers really earn their keep.

Designers are often put under cost or time pressure by managers who don’t understand the technical trade-offs, and so don’t understand that their actions could have the opposite effect to that which they intend and actually increase project costs and delays, as well as maybe increasing manufacturing and warranty costs. For more on this topic, please refer to [26], plus the final section of Part 2 [12].

18 References

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Some useful sources of further information

I would like to reference all of the articles, papers, application notes and textbooks that back-up the techniques described in this series, but the reference list would take longer to write than this series! However, I must mention the papers presented at the annual IEEE International EMC Symposium organised by the IEEE’s EMC Society (http://www.ewh.ieee.org/soc/emcs), especially the dozens of wonderful papers by Todd Hubing and his staff and students at the University of Missouri-Rolla EMC Lab (http://www.emclab.umr.edu), and papers by Bruce Archambeault of IBM and the EMC experts at Sun Microsystems.

Many other contributors to the IEEE EMC Symposia, and other conferences and symposia and private correspondence are far too numerous to be named here, but the following stand out: Tim Williams of Elmac Services, http://www.elmac.co.uk; Mark Montrose of Montrose Compliance Services, http://www.montrosecompliance.com; John Howard, http://www.emcguru.com; Tim Jarvis of RadioCAD, http://www.radiocad.com; Eric Bogatin of Giga-Test Labs, http://www.gigatest.com; and dozens of application notes from National Semiconductor; Rambus Corp.; California Micro Devices; Intel; IBM; Cypress Semiconductor; Xilinx; Sun; Motorola; AVX; X2Y Attenuators; Giga-Test Labs; Ansoft and Flomerics. I apologise to the very many excellent people and companies that I have had to leave out of this list.
Some other useful textbooks are:


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