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INTRODUCTION

High speed analog signal processing applications, such as video and communications, require op amps which have wide bandwidth, fast settling time, low distortion and noise, high output current, good DC performance, and operate at low supply voltages. These devices are widely used as gain blocks, cable drivers, ADC pre-amps, current-to-voltage converters, etc. Achieving higher bandwidths for less power is extremely critical in today's portable and battery-operated communications equipment. The rapid progress made over the last few years in high-speed linear circuits has hinged not only on the development of IC processes but also on innovative circuit topologies.

The evolution of high speed processes by using amplifier bandwidth as a function of supply current as a figure of merit is shown in Figure 1.1. (In the case of duals, triples, and quads, the current per amplifier is used). Analog Devices BiFET process, which produced the AD712 and OP249 (3MHz bandwidth, 3mA current), yields about 1MHz per mA. The CB (Complementary Bipolar) process (AD817, AD847, AD811, etc.) yields about 10MHz/mA of supply current. F_t's of the CB process PNP transistors are about 700MHz, and the NPN's about 900MHz.

The latest generation complementary bipolar process from Analog Devices is a high speed dielectrically isolated process called XFCB (eXtra Fast Complementary Bipolar). This process (2-4 GHz F_t matching PNP and NPN transistors), coupled with innovative circuit topologies allow op amps to achieve new levels of cost-effective performance at astonishing low quiescent currents. The approximate figure of merit for this process is typically 100MHz/mA, although the AD8011 op amp is capable of 300MHz bandwidth on 1mA of supply current due to its unique two-stage current-feedback architecture.
In order to select intelligently the correct op amp for a given application, an understanding of the various op amp topologies as well as the tradeoffs between them is required. The two most widely used topologies are voltage feedback (VFB) and current feedback (CFB). The following discussion treats each in detail and discusses the similarities and differences.

**Voltage Feedback (VFB) Op Amps**

A voltage feedback (VFB) op amp is distinguished from a current feedback (CFB) op amp by circuit topology. The VFB op amp is certainly the most popular in low frequency applications, but the CFB op amp has some advantages at high frequencies. We will discuss CFB in detail later, but first the more traditional VFB architecture.

Early IC voltage feedback op amps were made on "all NPN" processes. These processes were optimized for NPN transistors, and the "lateral" PNP transistors had relatively poor performance. Lateral PNPs were generally only used as current sources, level shifters, or for other non-critical functions. A simplified diagram of a typical VFB op amp manufactured on such a process is shown in Figure 1.2.
The input stage is a differential pair consisting of either a bipolar pair (Q1, Q2) or a FET pair. This \( g_m \) (transconductance) stage converts the small-signal differential input voltage, \( v \), into a current, \( i \), i.e., its transfer function is measured in units of conductance, 1/\( \Omega \), (or mhos). The small signal emitter resistance, \( r_e \), is approximately equal to the reciprocal of the small-signal \( g_m \). The formula for the small-signal \( g_m \) of a single bipolar transistor is given by the following equation:

\[
g_m = \frac{1}{r_e} = \frac{q}{kT} (I_C) = \frac{q}{kT} \left( \frac{I_T}{2} \right),
\]

or

\[
g_m \approx \left( \frac{1}{26mV} \right) \left( \frac{I_T}{2} \right).
\]

\( I_T \) is the differential pair tail current, \( I_C \) is the collector bias current (\( I_C = I_T/2 \)), \( q \) is the electron charge, \( k \) is Boltzmann's constant, and \( T \) is absolute temperature. At +25°C, \( V_T = kT/q = 26mV \) (often called the Thermal Voltage, \( V_T \)).

As we will see shortly, the amplifier unity gain-bandwidth product, \( f_u \), is equal to \( g_m / 2\pi C_p \), where the capacitance \( C_p \) is used to set the dominant pole frequency. For this reason, the tail current, \( I_T \), is made proportional to absolute temperature (PTAT). This current tracks the variation in \( r_e \) with temperature thereby making \( g_m \) independent of temperature. It is relatively easy to make \( C_p \) reasonably constant over temperature.

The output of one side of the \( g_m \) stage drives the emitter of a lateral PNP transistor (Q3). It is important to note that Q3 is not used to amplify the signal, only to level
shift, i.e., the signal current variation in the collector of Q2 appears at the collector of Q3. The output collector current of Q3 develops a voltage across high impedance node A. Cp sets the dominant pole of the frequency response. Emitter follower Q4 provides a low impedance output.

The effective load at the high impedance node A can be represented by a resistance, R_T, in parallel with the dominant pole capacitance, Cp. The small-signal output voltage, v_{out}, is equal to the small-signal current, i, multiplied by the impedance of the parallel combination of R_T and Cp.

Figure 1.3 shows a simple model for the single-stage amplifier and the corresponding Bode plot. The Bode plot is constructed on a log-log scale for convenience.

![Model and Bode Plot for a VFB Op Amp](image)

The low frequency breakpoint, f_o, is given by:

\[ f_o = \frac{1}{2\pi R_TC_p} \]

Note that the high frequency response is determined solely by g_m and Cp:

\[ v_{out} = v \cdot \frac{g_m}{j\omega C_p} \]

The unity gain-bandwidth frequency, f_u, occurs where \(|v_{out}| = |v|\). Solving the above equation for f_u, assuming \(|v_{out}| = |v|\):

\[ f_u = \frac{g_m}{2\pi C_p} \]

\[ f_CL = \frac{f_u}{1 + \frac{R_2}{R_1}} = \frac{f_u}{G} \]
\[ f_u = \frac{g_m}{2\pi Cp}. \]

We can use feedback theory to derive the closed-loop relationship between the circuit’s signal input voltage, \( v_{\text{in}} \), and its output voltage, \( v_{\text{out}} \):

\[
\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{j\omega C_p}{g_m} \left(1 + \frac{R_2}{R_1}\right)}.
\]

At the op amp 3dB closed-loop bandwidth frequency, \( f_{\text{cl}} \), the following is true:

\[
\frac{2\pi f_{\text{cl}} C_p}{g_m} \left(1 + \frac{R_2}{R_1}\right) = 1, \text{ and hence}
\]

\[
f_{\text{cl}} = \frac{g_m}{2\pi C_p} \left(\frac{1}{1 + \frac{R_2}{R_1}}\right), \text{ or}
\]

\[
f_{\text{cl}} = \frac{f_u}{1 + \frac{R_2}{R_1}}.
\]

This demonstrates a fundamental property of VFB op amps: The closed-loop bandwidth multiplied by the closed-loop gain is a constant, i.e., the VFB op amp exhibits a constant gain-bandwidth product over most of the usable frequency range.

Some VFB op amps (called de-compensated) are unstable at unity gain and are designed to be operated at some minimum amount of closed-loop gain. For these op amps, the gain-bandwidth product is still relatively constant over the region of allowable gain.

Now, consider the following typical example: \( I_T = 100\mu\text{A}, C_p = 2\text{pF} \). We find that:

\[
g_m = \frac{I_T / 2}{V_T} = \frac{50\mu\text{A}}{26\text{mV}} = \frac{1}{520\Omega}
\]

\[
f_u = \frac{g_m}{2\pi C_p} = \frac{1}{2\pi(520)(2 \cdot 10^{-12})} = 153\text{MHz}.
\]

Now, we must consider the large-signal response of the circuit. The slew-rate, \( \text{SR} \), is simply the total available charging current, \( I_T/2 \), divided by the dominant pole capacitance, \( C_p \). For the example under consideration,
\[ I = C \frac{dv}{dt}, \quad \frac{dv}{dt} = SR, \quad SR = \frac{I}{C} \]

\[ SR = \frac{I_T}{2} = \frac{50 \mu A}{2 p F} = 25 V / \mu s. \]

The full-power bandwidth (FPBW) of the op amp can now be calculated from the formula:

\[ \text{FPBW} = \frac{SR}{2 \pi A} = \frac{25 V / \mu s}{2 \pi \cdot 1 V} = 4 \text{MHz}, \]

where \( A \) is the peak amplitude of the output signal. If we assume a 2V peak-to-peak output sinewave (certainly a reasonable assumption for high speed applications), then we obtain a FPBW of only 4MHz, even though the small-signal unity gain-bandwidth product is 153MHz! For a 2V p-p output sinewave, distortion will begin to occur much lower than the actual FPBW frequency. We must increase the SR by a factor of about 40 in order for the FPBW to equal 153MHz. The only way to do this is to increase the tail current, \( I_T \), of the input differential pair by the same factor. This implies a bias current of 4mA in order to achieve a FPBW of 160MHz. We are assuming that \( C_p \) is a fixed value of 2pF and cannot be lowered by design.
VFB OP AMP BANDWIDTH AND SLEW RATE CALCULATION

- Assume that $I_T = 100\mu A$, $C_p = 2pF$
- $g_m = \frac{I_C}{V_T} = \frac{50\mu A}{26mV} = \frac{1}{520\Omega}$
- $f_u = \frac{g_m}{2\pi C_p} = 153MHz$
- Slew Rate $SR = \frac{I_T}{2C_p} = 25V/\mu s$

BUT FOR 2V PEAK-PEAK OUTPUT ($A = 1V$)

- $FPBW = \frac{SR}{2\pi A} = 4MHz$
- Must increase $I_T$ to 4mA to get $FPBW = 160MHz!!$
- Reduce $g_m$ by adding emitter degeneration resistors

In practice, the $FPBW$ of the op amp should be approximately 5 to 10 times the maximum output frequency in order to achieve acceptable distortion performance (typically 55-80dBc @ 5 to 20MHz, but actual system requirements vary widely).

Notice, however, that increasing the tail current causes a proportional increase in $g_m$ and hence $f_u$. In order to prevent possible instability due to the large increase in $f_u$, $g_m$ can be reduced by inserting resistors in series with the emitters of Q1 and Q2 (this technique, called emitter degeneration, also serves to linearize the $g_m$ transfer function and lower distortion).

A major inefficiency of conventional bipolar voltage feedback op amps is their inability to achieve high slew rates without proportional increases in quiescent current (assuming that $C_p$ is fixed, and has a reasonable minimum value of 2 or 3pF). This of course is not meant to say that high speed op amps designed using this architecture are deficient, it’s just that there are circuit design techniques available which allow equivalent performance at lower quiescent currents. This is extremely important in portable battery operated equipment where every milliwatt of power dissipation is critical.

**VFB Op Amps Designed on Complementary Bipolar Processes**

With the advent of complementary bipolar (CB) processes having high quality PNP transistors as well as NPNs, VFB op amp configurations such as the one shown in the simplified diagram (Figure 1.5) became popular.
Notice that the input differential pair (Q1, Q2) is loaded by a current mirror (Q3 and D1). We show D1 as a diode for simplicity, but it is actually a diode-connected PNP transistor (matched to Q3) with the base and collector connected to each other. This simplification will be used in many of the circuit diagrams to follow in this section. The common emitter transistor, Q4, provides a second voltage gain stage. Since the PNP transistors are fabricated on a complementary bipolar process, they are high quality and matched to the NPNs and suitable for voltage gain. The dominant pole of the amplifier is set by Cp, and the combination of the gain stage, Q4, and Cp is often referred to as a Miller Integrator. The unity-gain output buffer is usually a complementary emitter follower.

The model for this two-stage VFB op amp is shown in Figure 1.6. Notice that the unity gain-bandwidth frequency, $f_u$, is still determined by the $g_m$ of the input stage and the dominant pole capacitance, $C_p$. The second gain stage increases the DC open-loop gain, but the maximum slew rate is still limited by the input stage tail current: $SR = I_T/C_p$. 
The two-stage topology is widely used throughout the IC industry in VFB op amps, both precision and high speed.

Another popular VFB op amp architecture is the folded cascode as shown in Figure 1.7. An industry-standard video amplifier family (the AD847) is based on this architecture. This circuit takes advantage of the fast PNP’s available on a CB process. The differential signal currents in the collectors of Q1 and Q2 are fed to the emitters of a PNP cascode transistor pair (hence the term folded cascode). The collectors of Q3 and Q4 are loaded with the current mirror, D1 and Q5, and Q4 provides voltage gain. This single-stage architecture uses the junction capacitance at the high-impedance node for compensation (and some variations of the design bring this node to an external pin so that additional external capacitance can be added).
With no emitter degeneration resistors in Q1 and Q2, and no additional external compensating capacitance, this circuit is only stable for high closed-loop gains. However, unity-gain compensated versions of this family are available which have the appropriate amount of emitter degeneration.

The availability of JFETs on a CB process allows not only low input bias current but also improvements in the tradeoff which must be made between $g_m$ and $I_T$ found in bipolar input stages. Figure 1.8 shows a simplified diagram of the AD845 16MHz op amp. JFETs have a much lower $g_m$ per mA of tail current than a bipolar transistor. This allows the input tail current (hence the slew rate) to be increased without having to increase $C_p$ to maintain stability. The unusual thing about this seemingly poor performance of the JFET is that it is exactly what is needed on the input stage. For a typical JFET, the value of $g_m$ is approximately $I_S/1V$ ($I_S$ is the source current), rather than $I_c/26mV$ for a bipolar transistor, i.e., about 40 times lower. This allows much higher tail currents (and higher slew rates) for a given $g_m$ when JFETs are used as the input stage.
A New VFB Op Amp Architecture for "Current-on-Demand" Performance, Lower Power, and Improved Slew Rate

Until now, op amp designers had to make the above tradeoffs between the input $g_m$ stage quiescent current and the slew-rate and distortion performance. Analog Devices has patented a new circuit core which supplies current-on-demand to charge and discharge the dominant pole capacitor, $C_p$, while allowing the quiescent current to be small. The additional current is proportional to the fast slewing input signal and adds to the quiescent current. A simplified diagram of the basic core cell is shown in Figure 1.9.
The quad-core (gm stage) consists of transistors Q1, Q2, Q3, and Q4 with their emitters connected together as shown. Consider a positive step voltage on the inverting input. This voltage produces a proportional current in Q1 which is mirrored into Cp1 by Q5. The current through Q1 also flows through Q4 and Cp2. At the dynamic range limit, Q2 and Q3 are correspondingly turned off. Notice that the charging and discharging current for Cp1 and Cp2 is not limited by the quad core bias current. In practice, however, small current-limiting resistors are required forming an "H" resistor network as shown. Q7 and Q8 form the second gain stage (driven differentially from the collectors of Q5 and Q6), and the output is buffered by a unity-gain complementary emitter follower.

The quad core configuration is patented (Roy Gosser, U.S. Patent 5,150,074 and others pending), as well as the circuits which establish the quiescent bias currents (not shown in the diagram). A number of new VFB op amps using this proprietary configuration have been released and have unsurpassed high frequency low distortion performance, bandwidth, and slew rate at the indicated quiescent current levels (see Figure 1.10). The AD9631, AD8036, and AD8047 are optimized for a gain of +1, while the AD9632, AD8037, and AD8048 for a gain of +2. The same quad-core architecture is used as the second stage of the AD8041 rail-to-rail output, zero-volt input single-supply op amp. The input stage is a differential PNP pair which allows the input common-mode signal to go about 200mV below the negative supply rail. The AD8042 and AD8044 are dual and quad versions of the AD8041.
### CURRENT FEEDBACK (CFB) OP AMPS

We will now examine the current feedback (CFB) op amp topology which has recently become popular in high speed op amps. The circuit concepts were introduced many years ago, however modern high speed complementary bipolar processes are required to take full advantage of the architecture.

It has long been known that in bipolar transistor circuits, currents can be switched faster than voltages, other things being equal. This forms the basis of non-saturating emitter-coupled logic (ECL) and devices such as current-output DACs. Maintaining low impedances at the current switching nodes helps to minimize the effects of stray capacitance, one of the largest detriments to high speed operation. The current mirror is a good example of how currents can be switched with a minimum amount of delay.

The current feedback op amp topology is simply an application of these fundamental principles of current steering. A simplified CFB op amp is shown in Figure 1.11. The non-inverting input is high impedance and is buffered directly to the inverting input through the complementary emitter follower buffers Q1 and Q2. Note that the inverting input impedance is very low (typically 10 to 100Ω), because of the low emitter resistance. In the ideal case, it would be zero. This is a fundamental difference between a CFB and a VFB op amp, and also a feature which gives the CFB op amp some unique advantages.
The collectors of Q1 and Q2 drive current mirrors which mirror the inverting input current to the high impedance node, modeled by \( R_T \) and \( C_p \). The high impedance node is buffered by a complementary unity gain emitter follower. Feedback from the output to the inverting input acts to force the inverting input current to zero, hence the term *Current Feedback*. (In the ideal case, for zero inverting input impedance, no small signal voltage can exist at this node, only small signal current).

Consider a positive step voltage applied to the non-inverting input of the CFB op amp. Q1 immediately sources a proportional current into the external feedback resistors creating an *error current* which is mirrored to the high impedance node by Q3. The voltage developed at the high impedance node is equal to this current multiplied by the equivalent impedance. This is where the term *transimpedance op amp* originated, since the transfer function is an impedance, rather than a unitless voltage ratio as in a traditional VFB op amp.

Note that the error current is not limited by the input stage bias current, i.e., *there is no slew-rate limitation in an ideal CFB op amp*. The current mirrors supply *current-on-demand* from the power supplies. The negative feedback loop then forces the output voltage to a value which reduces the inverting input error current to zero.

The model for a CFB op amp is shown in Figure 1.12 along with the corresponding Bode plot. The Bode plot is plotted on a log-log scale, and the open-loop gain is expressed as a transimpedance, \( T(s) \), with units of ohms.
The finite output impedance of the input buffer is modeled by $R_o$. The input error current is $i$. By applying the principles of negative feedback, we can derive the expression for the op amp transfer function:

$$
\frac{v_{out}}{v_{in}} = \frac{1 + \frac{R_2}{R_1}}{1 + j\omega C P R_2 \left(1 + \frac{R_o}{R_2} + \frac{R_o}{R_1}\right)}.
$$

At the op amp 3db closed-loop bandwidth frequency, $f_{cl}$, the following is true:

$$
2\pi f_{cl} C P R_2 \left(1 + \frac{R_o}{R_2} + \frac{R_o}{R_1}\right) = 1.
$$

Solving for $f_{cl}$:

$$
f_{cl} = \frac{1}{2\pi C P R_2 \left(1 + \frac{R_o}{R_2} + \frac{R_o}{R_1}\right)}.
$$

For the condition $R_o << R_2$ and $R_1$, the equation simply reduces to:

$$
f_{cl} = \frac{1}{2\pi C P R_2}.
$$
Examination of this equation quickly reveals that the closed-loop bandwidth of a CFB op amp is determined by the internal dominant pole capacitor, \( C_p \), and the external feedback resistor \( R_2 \), and is independent of the gain-setting resistor, \( R_1 \). This ability to maintain constant bandwidth independent of gain makes CFB op amps ideally suited for wideband programmable gain amplifiers.

Because the closed-loop bandwidth is inversely proportional to the external feedback resistor, \( R_2 \), a CFB op amp is usually optimized for a specific \( R_2 \). Increasing \( R_2 \) from its optimum value lowers the bandwidth, and decreasing it may lead to oscillation and instability because of high frequency parasitic poles.

The frequency response of the AD8011 CFB op amp is shown in Figure 1.13 for various closed-loop values of gain (+1, +2, and +10). Note that even at a gain of +10, the closed loop bandwidth is still greater than 100MHz. The peaking which occurs at a gain of +1 is typical of wideband CFB op amps when used in the non-inverting mode and is due primarily to stray capacitance at the inverting input. The peaking can be reduced by sacrificing bandwidth and using a slightly larger feedback resistor. The AD8011 CFB op amp represents state-of-the-art performance, and key specifications are shown in Figure 1.14.

### AD8011 FREQUENCY RESPONSE

\[ G = +1, +2, +10 \]

![Frequency Response Graph](image)

### AD8011 CFB OP AMP KEY SPECIFICATIONS

- 1mA Power Supply Current (+5V or ±5V)
- 300MHz Bandwidth (\( G = +1 \))
- 2000 V/µs Slew Rate
- 29ns Settling Time to 0.1%
- Video Specifications (\( G = +2 \))
  - Differential Gain Error 0.02%
Traditional current feedback op amps have been limited to a single gain stage, using current-mirrors as previously described. The AD8011 (and also others in this family: AD8001, AD8002, AD8004, AD8005, AD8009, AD8013, AD8072, AD8073), unlike traditional CFB op amps uses a two-stage gain configuration as shown in Figure 1.15. Until now, fully complementary two-gain stage CFB op amps have been impractical because of their high power dissipation. The AD8011 employs a second gain stage consisting of a pair of complementary amplifiers (Q3 and Q4). Note that they are not connected as current mirrors but as grounded-emitters. The detailed design of current sources (I1 and I2), and their respective bias circuits (Roy Gosser, patent-applied-for) are the key to the success of the two-stage CFB circuit; they keep the amplifier’s quiescent power low, yet are capable of supplying current-on-demand for wide current excursions required during fast slewing.

A further advantage of the two-stage amplifier is the higher overall bandwidth (for the same power), which means lower signal distortion and the ability to drive heavier external loads.
Thus far, we have learned several key features of CFB op amps. The most important is that for a given complementary bipolar IC process, CFB generally always yields higher FPBW (hence lower distortion) than VFB for the same amount of quiescent supply current. This is because there is practically no slew-rate limiting in CFB. Because of this, the full power bandwidth and the small signal bandwidth are approximately the same.

The second important feature is that the *inverting input impedance of a CFB op amp is very low*. This can be advantageous when using the op amp in the inverting mode as an I/V converter, because there is much less sensitivity to inverting input capacitance than with VFB.

The third feature is that the *closed-loop bandwidth of a CFB op amp is determined by the value of the internal Cp capacitor and the external feedback resistor R2 and is relatively independent of the gain-setting resistor R1*. We will now examine some typical applications issues and make further comparisons between CFBs and VFBs.

### CURRENT FEEDBACK OP AMP FAMILY

<table>
<thead>
<tr>
<th>PART</th>
<th>I$_{Q}$/AMP</th>
<th>BANDWIDTH</th>
<th>SLEW RATE</th>
<th>DISTORTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8001 (1)</td>
<td>5.5mA</td>
<td>880MHz</td>
<td>1200V/µs</td>
<td>–65dBc@5MHz</td>
</tr>
<tr>
<td>AD8002 (2)</td>
<td>5.0mA</td>
<td>600MHz</td>
<td>1200V/µs</td>
<td>–65dBc@5MHz</td>
</tr>
<tr>
<td>AD8004 (4)</td>
<td>3.5mA</td>
<td>250MHz</td>
<td>3000V/µs</td>
<td>–78dBc@5MHz</td>
</tr>
<tr>
<td>AD8005 (1)</td>
<td>0.4mA</td>
<td>180MHz</td>
<td>500V/µs</td>
<td>–53dBc@5MHz</td>
</tr>
<tr>
<td>AD8009 (1)</td>
<td>11mA</td>
<td>1000MHz</td>
<td>7000V/µs</td>
<td>–80dBc@5MHz</td>
</tr>
<tr>
<td>AD8011 (1)</td>
<td>1mA</td>
<td>300MHz</td>
<td>2000V/µs</td>
<td>–70dBc@5MHz</td>
</tr>
<tr>
<td>AD8012 (2)</td>
<td>1mA</td>
<td>300MHz</td>
<td>1200V/µs</td>
<td>–66dBc@5MHz</td>
</tr>
<tr>
<td>AD8013 (3)</td>
<td>4mA</td>
<td>140MHz</td>
<td>1000V/µs</td>
<td>ΔG=0.02%, Δφ=0.06°</td>
</tr>
<tr>
<td>AD8072 (2)</td>
<td>5mA</td>
<td>100MHz</td>
<td>500V/µs</td>
<td>ΔG=0.05%, Δφ=0.1°</td>
</tr>
<tr>
<td>AD8073 (3)</td>
<td>5mA</td>
<td>100MHz</td>
<td>500V/µs</td>
<td>ΔG=0.05%, Δφ=0.1°</td>
</tr>
</tbody>
</table>

*Number in ( ) Indicates Single, Dual, Triple, or Quad*

---

**SUMMARY: CURRENT FEEDBACK OP AMPS**

- CFB yields higher FPBW and lower distortion than VFB for the same process and power dissipation
Inverting input impedance of a CFB op amp is low, non-inverting input impedance is high

Closed-loop bandwidth of a CFB op amp is determined by the internal dominant-pole capacitance and the external feedback resistor, independent of the gain-setting resistor

**EFFECTS OF FEEDBACK CAPACITANCE IN OP AMPS**

At this point, the term *noise gain* needs some clarification. Noise gain is the amount by which a small amplitude noise voltage source in series with an input terminal of an op amp is amplified when measured at the output. The input voltage noise of an op amp is modeled in this way. It should be noted that the DC noise gain can also be used to reflect the input offset voltage (and other op amp input error sources) to the output.

*Noise gain* must be distinguished from *signal gain*. Figure 1.18 shows an op amp in the inverting and non-inverting mode. In the non-inverting mode, notice that noise gain is equal to signal gain. However, in the inverting mode, the noise gain doesn't change, but the signal gain is now \(-\frac{R_2}{R_1}\). Resistors are shown as feedback elements, however, the networks may also be reactive.

**NOISE GAIN AND SIGNAL GAIN COMPARISON**

**NON-INVERTING**

\[
\text{SIGNAL GAIN} = 1 + \frac{R_2}{R_1}
\]

\[
\text{NOISE GAIN} = 1 + \frac{R_2}{R_1}
\]

**INVERTING**

\[
\text{SIGNAL GAIN} = -\frac{R_2}{R_1}
\]

\[
\text{NOISE GAIN} = 1 + \frac{R_2}{R_1}
\]

For VFB op amp:

\[
\text{CLOSED-LOOP BW} = \frac{\text{UNITY GAIN BANDWIDTH FREQUENCY}}{\text{NOISE GAIN}}
\]

\[
f_{CL} = \frac{f_u}{G}
\]
Two other configurations are shown in Figure 1.19 where the noise gain has been increased independent of signal gain by the addition of R3 across the input terminals of the op amp. This technique can be used to stabilize de-compensated op amps which are unstable for low values of noise gain. However, the sensitivity to input noise and offset voltage is correspondingly increased.

**INCREASING THE NOISE GAIN WITHOUT AFFECTING SIGNAL GAIN**

![Diagram of op amp configurations showing noise and signal gain calculations.]

Noise gain is often plotted as a function of frequency on a Bode plot to determine the op amp stability. If the feedback is purely resistive, the noise gain is constant with frequency. However, reactive elements in the feedback loop will cause it to change with frequency. Using a log-log scale for the Bode plot allows the noise gain to be easily drawn by simply calculating the breakpoints determined by the frequencies of the various poles and zeros. The point of intersection of the noise gain with the open-loop gain not only determines the op amp *closed-loop bandwidth*, but also can be used to analyze stability.

An excellent explanation of how to make simplifying approximations using Bode plots to analyze gain and phase performance of a feedback networks is given in Reference 4.

Just as signal gain and noise gain can be different, so can the *signal bandwidth* and the *closed-loop bandwidth*. The op amp closed-loop bandwidth, \( f_{cl} \), is always determined by the intersection of the noise gain with the open-loop frequency response. The signal bandwidth is equal to the closed-loop bandwidth only if the feedback network is purely resistive.
It is quite common to use a capacitor in the feedback loop of a VFB op amp to shape the frequency response as in a simple single-pole lowpass filter (see Figure 1.20a). The resulting noise gain is plotted on a Bode plot to analyze stability and phase margin. Stability of the system is determined by the net slope of the noise gain and the open loop gain where they intersect. For unconditional stability, the noise gain plot must intersect the open loop response with a net slope of less than 12dB/octave. In this case, the net slope where they intersect is 6dB/octave, indicating a stable condition. Notice for the case drawn in Figure 1.20a, the second pole in the frequency response occurs at a considerably higher frequency than $f_u$.

**NOISE GAIN STABILITY ANALYSIS FOR VFB AND CFB OP AMPS WITH FEEDBACK CAPACITOR**

In the case of the CFB op amp (Figure 1.20b), the same analysis is used, except that the open-loop transimpedance gain, $T(s)$, is used to construct the Bode plot. The definition of noise gain (for the purposes of stability analysis) for a CFB op amp, however, must be redefined in terms of a current noise source attached to the inverting input (see Figure 1.21). This current is reflected to the output by an impedance which we define to be the "current noise gain" of a CFB op amp:

"CURRENT NOISE GAIN"

$$
\equiv R_o + Z \left(1 + \frac{R_o}{Z_i}\right)
$$
CURRENT "NOISE GAIN" DEFINITION FOR CFB OP AMP FOR USE IN STABILITY ANALYSIS

Now, return to Figure 1.20b, and observe the CFB current noise gain plot. At low frequencies, the CFB current noise gain is simply $R_2$ (making the assumption that $R_o$ is much less than $Z_1$ or $Z_2$. The first pole is determined by $R_2$ and $C_2$. As the frequency continues to increase, $C_2$ becomes a short circuit, and all the inverting input current flows through $R_o$ (refer back to Figure 1.21).

The CFB op amp is normally optimized for best performance for a fixed feedback resistor, $R_2$. Additional poles in the transimpedance gain, $T(s)$, occur at frequencies above the closed loop bandwidth, $f_{cl}$, (set by $R_2$). Note that the intersection of the CFB current noise gain with the open-loop $T(s)$ occurs where the slope of the $T(s)$ function is 12dB/octave. This indicates instability and possible oscillation.

It is for this reason that **CFB op amps are not suitable in configurations which require capacitance in the feedback loop**, such as simple active integrators or lowpass filters. They can, however, be used in certain active filters such as the Sallen-Key configuration shown in Figure 1.22 which do not require capacitance in the feedback network.
EITHER CFB OR VFB OP AMPS CAN BE USED IN THE SALLEN-KÉY FILTER CONFIGURATION

VFB op amps, on the other hand, make very flexible active filters. A multiple feedback 20MHz lowpass filter using the AD8048 is shown in Figure 1.23.
In general, the amplifier should have a bandwidth which is at least ten times the bandwidth of the filter if problems due to phase shift of the amplifier are to be avoided. (The AD8048 has a bandwidth of over 200MHz in this configuration). The filter is designed as follows:

Choose:

\( F_0 = \text{Cutoff Frequency} = 20\text{MHz} \)
\( \alpha = \text{Damping Ratio} = 1/Q = 2 \)
\( H = \text{Absolute Value of Circuit Gain} \)
\( \quad = | -R_4/R_1 | = 1 \)
\( k = 2\pi F_0 C_1 \)

\[ C_2 = \frac{4C_1(H + 1)}{\alpha^2} = 100\text{pF} \text{, for } C_1 = 50\text{pF} \]

\[ R_1 = \frac{\alpha}{2Hk} = 159.2\Omega \text{, use } 154\Omega \]

\[ R_3 = \frac{\alpha}{2k(H + 1)} = 79.6\Omega \text{, use } 78.7\Omega \]

\[ R_4 = H \cdot R_1 = 159.2\Omega \text{, use } 154\Omega \]

**High Speed Current-to-Voltage Converters, and the Effects of Inverting Input Capacitance**

Fast op amps are useful as current-to-voltage converters in such applications as high speed photodiode preamplifiers and current-output DAC buffers. A typical application using a VFB op amp as an I/V converter is shown in Figure 1.24.
The net input capacitance, $C_1$, forms a pole at a frequency $f_p$ in the noise gain transfer function as shown in the Bode plot, and is given by:

$$f_p = \frac{1}{2\pi R_2 C_1}.$$  

If left uncompensated, the phase shift at the frequency of intersection, $f_x$, will cause instability and oscillation. Introducing a zero at $f_x$ by adding feedback capacitor $C_2$ stabilizes the circuit and yields a phase margin of about 45 degrees. The location of the zero is given by:

$$f_x = \frac{1}{2\pi R_2 C_2}.$$  

Although the addition of $C_2$ actually decreases the pole frequency slightly, this effect is negligible if $C_2 \ll C_1$. The frequency $f_x$ is the geometric mean of $f_p$ and the unity-gain bandwidth frequency of the op amp, $f_u$.

$$f_x = \sqrt{f_p \cdot f_u}.$$  

These equations can be solved for $C_2$:

$$C_2 = \sqrt[3]{\frac{C_1}{2\pi R^2 \cdot f_u}}.$$
This value of $C_2$ will yield a phase margin of about 45 degrees. Increasing the capacitor by a factor of 2 increases the phase margin to about 65 degrees (see References 4 and 5).

In practice, the optimum value of $C_2$ may be optimized experimentally by varying it slightly to optimize the output pulse response.

A similar analysis can be applied to a CFB op amp as shown in Figure 1.25. In this case, however, the low inverting input impedance, $R_o$, greatly reduces the sensitivity to input capacitance. In fact, an ideal CFB with zero input impedance would be totally insensitive to any amount of input capacitance!

The pole caused by $C_1$ occurs at a frequency $f_p$:

$$f_p = \frac{1}{2\pi (R_o || R_2) C_1} \approx \frac{1}{2\pi R_o C_1}.$$  

This pole frequency will be generally be much higher than the case for a VFB op amp, and the pole can be ignored completely if it occurs at a frequency greater than the closed-loop bandwidth of the op amp.

We next introduce a compensating zero at the frequency $f_x$ by inserting the capacitor $C_2$:

$$f_x = \frac{1}{2\pi R_2 C_2}.$$
As in the case for VFB, \( f_x \) is the geometric mean of \( f_p \) and \( f_{cl} \):

\[
f_x = \sqrt{f_p \cdot f_u}.
\]

Solving the equations for \( C_2 \) and rearranging it yields:

\[
C_2 = \frac{R_o \cdot \sqrt{\frac{C_1}{2\pi R_2 \cdot f_{cl}}}}{R_2}.
\]

There is a significant advantage in using a CFB op amp in this configuration as can be seen by comparing the similar equation for \( C_2 \) required for a VFB op amp. If the unity-gain bandwidth product of the VFB is equal to the closed-loop bandwidth of the CFB (at the optimum \( R_2 \)), then the size of the CFB compensation capacitor, \( C_2 \), is reduced by a factor of \( \sqrt{R_2/R_o} \).

A comparison in an actual application is shown in Figure 1.26. The full scale output current of the DAC is 4mA, the net capacitance at the inverting input of the op amp is 20pF, and the feedback resistor is 500\( \Omega \). In the case of the VFB op amp, the pole due to \( C_1 \) occurs at 16MHz. A compensating capacitor of 5.6pF is required for 45 degrees of phase margin, and the signal bandwidth is 57MHz.

For the CFB op amp, however, because of the low inverting input impedance (\( R_o = 50\Omega \)), the pole occurs at 160MHz, the required compensation capacitor is about 1.8pF, and the corresponding signal bandwidth is 176MHz. In actual practice, the
pole frequency is so close to the closed-loop bandwidth of the op amp that it could probably be left uncompensated.

It should be noted that a CFB op amp’s relative insensitivity to inverting input capacitance is when it is used in the inverting mode. In the non-inverting mode, even a few picofarads of stray capacitance on the inverting input can cause significant gain-peaking and potential instability.

Another advantage of the low inverting input impedance of the CFB op amp is when it is used as an I/V converter to buffer the output of a high speed current output DAC. When a step function current (or DAC switching glitch) is applied to the inverting input of a VFB op amp, it can produce a large voltage transient until the signal can propagate through the op amp to its output and negative feedback is regained. Back-to-back Schottky diodes are often used to limit this voltage swing as shown in Figure 1.27. These diodes must be low capacitance, small geometry devices because their capacitance adds to the total input capacitance.

A CFB op amp, on the other hand, presents a low impedance (Ro) to fast switching currents even before the feedback loop is closed, thereby limiting the voltage excursion without the requirement of the external diodes. This greatly improves the settling time of the I/V converter.

**LOW INVERTING INPUT IMPEDANCE OF CFB OP AMP HELPS REDUCE AMPLITUDE OF FAST DAC TRANSIENTS**

![Diagram](image)

**NOT REQUIRED FOR CFB OP AMP BECAUSE OF LOW INVERTING INPUT IMPEDANCE**
Op amp noise has two components: low frequency noise whose spectral density is inversely proportional to the square root of the frequency and white noise at medium and high frequencies. The low-frequency noise is known as 1/f noise (the noise power obeys a 1/f law - the noise voltage or noise current is proportional to 1/√f). The frequency at which the 1/f noise spectral density equals the white noise is known as the "1/f Corner Frequency" and is a figure of merit for the op amp, with the low values indicating better performance. Values of 1/f corner frequency vary from a few Hz for the most modern low noise low frequency amplifiers to several hundreds, or even thousands of Hz for high-speed op amps.

In most applications of high speed op amps, it is the total output rms noise that is generally of interest. Because of the high bandwidths, the chief contributor to the output rms noise is the white noise, and that of the 1/f noise is negligible.

In order to better understand the effects of noise in high speed op amps, we use the classical noise model shown in Figure 1.28. This diagram identifies all possible white noise sources, including the external noise in the source and the feedback resistors. The equation allows you to calculate the total output rms noise over the closed-loop bandwidth of the amplifier. This formula works quite well when the frequency response of the op amp is relatively flat. If there is more than a few dB of high frequency peaking, however, the actual noise will be greater than the predicted because the contribution over the last octave before the 3dB cutoff frequency will dominate. In most applications, the op amp feedback network is designed so that the bandwidth is relatively flat, and the formula provides a good estimate. Note that BW in the equation is the equivalent noise bandwidth which, for a single-pole system, is obtained by multiplying the closed-loop bandwidth by 1.57.

**OP AMP NOISE MODEL FOR A FIRST-ORDER CIRCUIT WITH RESISTIVE FEEDBACK**

![Diagram](image)

\[
V_{ON} = \sqrt{BW} \sqrt{\left( n_{-} R_2^2 + n_{+} R_p^2 \right) \left( \frac{R_2}{R_1} + \frac{R_2^2}{R_1^2} \right) + \left( n_{-}^2 + n_{+}^2 \right) \left( \frac{R_2}{R_1} \right) \left( \frac{R_2^2}{R_1^2} \right) + 4kT R_2 + 4kT R_2 R_p + 4kT R_1 + \frac{R_2}{R_1}}
\]

BW = 1.57f<sub>cl</sub>

f<sub>cl</sub> = CLOSED LOOP BANDWIDTH
Figure 1.29 shows a table which indicates how the individual noise contributors are referred to the output. After calculating the individual noise spectral densities in this table, they can be squared, added, and then the square root of the sum of the squares yields the RSS value of the output noise spectral density since all the sources are uncorrelated. This value is multiplied by the square root of the noise bandwidth (noise bandwidth = closed-loop bandwidth multiplied by a correction factor of 1.57) to obtain the final value for the output rms noise.

**REFERRING ALL NOISE SOURCES TO THE OUTPUT**

<table>
<thead>
<tr>
<th>Noise Source Expressed As a Voltage</th>
<th>Multiply By This Factor To Refer To the Op Amp Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Johnson Noise in Rp: ( \frac{\sqrt{4kTR_p}}{} )</td>
<td>Noise Gain = ( 1 + \frac{R_2}{R_1} )</td>
</tr>
<tr>
<td>Non-Inverting Input Current Noise Flowing in Rp: ( I_{n+}R_p )</td>
<td>Noise Gain = ( 1 + \frac{R_2}{R_1} )</td>
</tr>
<tr>
<td>Input Voltage Noise: ( V_n )</td>
<td>Noise Gain = ( 1 + \frac{R_2}{R_1} )</td>
</tr>
<tr>
<td>Johnson Noise in R1: ( \frac{\sqrt{4kTR_1}}{} )</td>
<td>(-R_2/R_1) (Gain from input of R1 to Output)</td>
</tr>
<tr>
<td>Johnson Noise in R2: ( \frac{\sqrt{4kTR_2}}{} )</td>
<td>1</td>
</tr>
<tr>
<td>Inverting Input Current Noise Flowing in R2: ( I_{n-R2} )</td>
<td>1</td>
</tr>
</tbody>
</table>

Typical high speed op amps with bandwidths greater than 150MHz or so, and bipolar input stages have input voltage noises ranging from about 2 to 20nV/√Hz. To put voltage noise in perspective, let’s look at the Johnson noise spectral density of a resistor:

\[ v_n = \sqrt{4kTR \cdot BW}, \]

where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature, \( R \) is the resistor value, and \( BW \) is the equivalent noise bandwidth of interest. (The equivalent noise bandwidth of a single-pole system is 1.57 times the 3dB frequency). Using the formula, a 100Ω resistor has a noise density of 1.3nV/√Hz, and a 1000Ω resistor about 4nV/√Hz (values are at room temperature: 27°C, or 300K).

The base-emitter in a bipolar transistor has an equivalent noise voltage source which is due to the "shot noise" of the collector current flowing in the transistor’s
(noiseless) incremental emitter resistance, \( r_e \). The current noise is proportional to the square root of the collector current, \( I_c \). The emitter resistance, on the other hand, is inversely proportional to the collector current, so the shot-noise voltage is inversely proportional to the square root of the collector current. (Reference 5, Section 9).

Voltage noise in FET-input op amps tends to be larger than for bipolar ones, but current noise is extremely low (generally only a few tens of fA/√Hz) because of the low input bias currents. However, FET-inputs are not generally required for op amp applications requiring bandwidths greater than 100MHz.

Op amps also have input current noise on each input. For high-speed FET-input op amps, the gate currents are so low that input current noise is almost always negligible (measured in fA/√Hz).

For a VFB op amp, the inverting and non-inverting input current noise are typically equal, and almost always uncorrelated. Typical values for wideband VFB op amps range from 0.5pA/√Hz to 5pA/√Hz. The input current noise of a bipolar input stage is increased when input bias-current cancellation generators are added, because their current noise is not correlated, and therefore adds (in an RSS manner) to the intrinsic current noise of the bipolar stage.

The input voltage noise in CFB op amps tends to be lower than for VFB op amps having the same approximate bandwidth. This is because the input stage in a CFB op amp is usually operated at a higher current, thereby reducing the emitter resistance and hence the voltage noise. Typical values for CFB op amps range from about 1 to 5nV/√Hz.

The input current noise of CFB op amps tends to be larger than for VFB op amps because of the generally higher bias current levels. The inverting and non-inverting current noise of a CFB is usually different because of the unique input architecture, and are specified separately. In most cases, the inverting input current noise is the larger of the two. Typical input current noise for CFB op amps ranges from 5 to 40pA/√Hz.

The general principle of noise calculation is that uncorrelated noise sources add in a root-sum-squares manner, which means that if a noise source has a contribution to the output noise of a system which is less than 20% of the amplitude of the noise from other noise source in the system, then its contribution to the total system noise will be less than 2% of the total, and that noise source can almost invariably be ignored - in many cases, noise sources smaller than 33% of the largest can be ignored. This can simplify the calculations using the formula, assuming the correct decisions are made regarding the sources to be included and those to be neglected.

The sources which dominate the output noise are highly dependent on the closed-loop gain of the op amp. Notice that for high values of closed loop gain, the op amp voltage noise will tend be the chief contributor to the output noise. At low gains, the effects of the input current noise must also be considered, and may dominate, especially in the case of a CFB op amp.

Feedforward/feedback resistors in high speed op amp circuits may range from less than 100Ω to more than 1kΩ, so it is difficult to generalize about their contribution
to the total output noise without knowing the specific values and the closed loop gain. The best way to make the calculations is to write a simple computer program which performs the calculations automatically and include all noise sources. In most high speed applications, the source impedance noise can be neglected for source impedances of 100Ω or less.

Figure 1.30 shows an example calculation of total output noise for the AD8011 (300MHz, 1mA) CFB op amp. All six possible sources are included in the calculation. The appropriate multiplying factors which reflect the sources to the output are also shown on the diagram. For G=2, the close-loop bandwidth of the AD8011 is 180MHz. The correction factor of 1.57 in the final calculation converts this single-pole bandwidth into the circuits equivalent noise bandwidth.

In communications applications, it is common to specify the noise figure (NF) of an amplifier. Figure 1.31 shows the definition. NF is the ratio of the total integrated output noise from all sources to the total output noise which would result if the op amp were "noiseless" (this noise would be that of the source resistance multiplied by the gain of the op amp using the closed-loop bandwidth of the op amp to make the calculation). Noise figure is expressed in dB. The value of the source resistance must be specified, and in most RF systems, it is 50Ω. Noise figure is useful in communications receiver design, since it can be used to measure the decrease in signal-to-noise ratio. For instance, an amplifier with a noise figure of 10dB following a stage with a signal-to-noise ratio of 50dB reduces the signal-to-noise ratio to 40dB.
The ratio is commonly expressed in dB and is useful in signal chain analysis. In the previous example, the total output voltage noise was 8.7nV/√Hz. Integrated over the closed loop bandwidth of the op amp (180MHz), this yielded an output noise of 146µV rms. The noise of the 50Ω source resistance is 0.9nV/√Hz. If the op amp were noiseless (with noiseless feedback resistors), this noise would appear at the output multiplied by the noise gain (G=2) of the op amp, or 1.8nV/√Hz. The total output rms noise just due to the source resistor integrated over the same bandwidth is 30.3µV rms. The noise figure is calculated as:

\[
NF \text{ dB} = 20 \log_{10} \left( \frac{146}{30.3} \right) = 13.7 \text{dB}.
\]

The same result can be obtained by working with spectral densities, since the bandwidths used for the integration are the same and cancel each other in the equation.

\[
NF = 20 \log_{10} \left( \frac{8.7}{1.8} \right) = 13.7 \text{dB}.
\]

**HIGH SPEED OP AMP NOISE SUMMARY**

- **Voltage Feedback Op Amps:**
  - Voltage Noise: 2 to 20nV/√Hz
  - Current Noise: 0.5 to 5pA/√Hz

- **Current Feedback Op Amps:**
Voltage Noise: 1 to 5nV/√Hz
Current Noise: 5 to 40pA/√Hz

- Noise Contribution from Source Negligible if < 100Ω
- Voltage Noise Usually Dominates at High Gains
- Reflect Noise Sources to Output and Combine (RSS)
- Errors Will Result if there is Significant High Frequency Peaking

DC CHARACTERISTICS OF HIGH SPEED OP AMPS

High speed op amps are optimized for bandwidth and settling time, not for precision DC characteristics as found in lower frequency op amps such as the industry standard OP27. In spite of this, however, high speed op amps do have reasonably good DC performance. The model shown in Figure 1.33 shows how to reflect the input offset voltage and the offset currents to the output.

MODEL FOR CALCULATING TOTAL OP AMP OUTPUT VOLTAGE OFFSET

\[
V_O = \pm V_{OS} \left[ 1 + \frac{R_2}{R_1} + I_{b+}R_3 \left( 1 + \frac{R_2}{R_1} \right) - I_{b-}R_2 \right]
\]

IF \( I_{b+} = I_{b-} \) AND \( R_3 = R_1|R_2 \)
\[
V_O = \pm V_{OS} \left[ 1 + \frac{R_2}{R_1} \right]
\]
Input offset voltages of high speed bipolar input op amps are rarely trimmed, since offset voltage matching of the input stage is excellent, typically ranging from 1 to 3mV, with offset temperature coefficients of 5 to 15µV/°C.

Input bias currents on VFB op amps (with no input bias current compensation circuits) are approximately equal for (+) and (–) inputs, and can range from 1 to 5µA. The output offset voltage due to the input bias currents can be nulled by making the effective source resistance, R3, equal to the parallel combination of R1 and R2.

This scheme will not work, however, with bias-current compensated VFB op amps which have additional current generators on their inputs. In this case, the net input bias currents are not necessarily equal or of the same polarity. Op amps designed for rail-to-rail input operation (parallel PNP and NPN differential stages as described later in this section) have bias currents which are also a function of the common-mode input voltage. External bias current cancellation schemes are ineffective with these op amps also. It should be noted, however, that it is often desirable to match the source impedance seen by the (+) and (–) inputs of VFB op amps to minimize distortion.

CFB op amps generally have unequal and uncorrelated input bias currents because the (+) and (–) inputs have completely different architectures. For this reason, external bias current cancellation schemes are also ineffective. CFB input bias currents range from 5 to 15µA, being generally higher at the inverting input.

**OUTPUT OFFSET VOLTAGE SUMMARY**

- **High Speed Bipolar Op Amp Input Offset Voltage:**
  - Ranges from 1 to 3mV for VFB and CFB
  - Offset TC Ranges from 5 to 15µV/°C

- **High Speed Bipolar Op Amp Input Bias Current:**
  - For VFB Ranges from 1 to 5µA
  - For CFB Ranges from 5 to 15µA

- **Bias Current Cancellation Doesn't Work for:**
  - Bias Current Compensated Op Amps
  - Current Feedback Op Amps

---

**PSRR CHARACTERISTICS OF HIGH SPEED OP amps**

As with most op amps, the power supply rejection ratio (PSRR) of high speed op amps falls off rapidly at higher frequencies. Figure 1.35 shows the PSRR for the AD8011 CFB 300MHz CFB op amp. Notice that at DC, the PSRR is nearly 60dB, however, at 10MHz, it falls to only 20dB, indicating the need for excellent external LF and HF decoupling. These numbers are fairly typical of most high speed VFB or CFB op amps, although the DC PSRR may range from 55 to 80dB depending on the op amp.
The power pins of op amps must be decoupled directly to a large-area ground plane with capacitors which have minimal lead length. It is generally recommended that a low-inductance ceramic surface mount capacitor (0.01µF to 0.1µF) be used for the high frequency noise. The lower frequency noise can be decoupled with low-inductance tantalum electrolytic capacitors (1 to 10µF).
REFERENCES


SECTION 2
HIGH SPEED OP AMP APPLICATIONS
Walt Kester, Walt Jung

OPTIMIZING THE FEEDBACK NETWORK FOR MAXIMUM BANDWIDTH FLATNESS IN WIDEBAND CFB OP AMPS

Achieving the highest 0.1dB bandwidth flatness is important in many video applications. Because of the critical relationship between the feedback resistor and the bandwidth of a CFB op amp, optimum bandwidth flatness is highly dependent on the feedback resistor value, the resistor parasitics, as well as the op amp package and PCB parasitics. Figure 2.1 shows the fine scale (0.1dB/division) flatness plotted versus the feedback resistance for the AD8001 in a non-inverting gain of 2. These plots were made using the AD8001 evaluation board with surface mount resistors.

AD8001 CFB OP AMP BANDWIDTH FLATNESS OPTIMIZED BY PROPER SELECTION OF FEEDBACK RESISTOR

It is recommended that once the optimum resistor values have been determined, 1% tolerance values should be used. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors are the optimum choice, and it is not recommended that leaded components be used with high speed op amps at these frequencies because of their parasitics.

Slightly different resistor values may be required to achieve optimum performance in the DIP versus the SOIC packages (see Figure 2.2). The SOIC package exhibits slightly lower parasitic capacitance and inductance than the DIP. The data shows the optimum feedback (RF) and feedforward (RG) resistors for highest 0.1dB bandwidth for the AD8001 in the DIP and the SOIC packages. As you might
suspect, the SOIC package can be optimized for slightly higher 0.1dB bandwidth because of its lower parasitics.

### OPTIMUM VALUES OF RF AND RG FOR AD8001 DIP AND SOIC PACKAGES (MAXIMUM 0.1dB BANDWIDTH)

#### AD8001AN (DIP) GAIN

<table>
<thead>
<tr>
<th>Component</th>
<th>–1</th>
<th>+1</th>
<th>+2</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF</td>
<td>649Ω</td>
<td>1050Ω</td>
<td>750Ω</td>
</tr>
<tr>
<td>RG</td>
<td>649Ω</td>
<td>-</td>
<td>750Ω</td>
</tr>
<tr>
<td>0.1dB Flatness</td>
<td>105MHz</td>
<td>70MHz</td>
<td>105MHz</td>
</tr>
</tbody>
</table>

#### AD8001AR (SOIC) GAIN

<table>
<thead>
<tr>
<th>Component</th>
<th>–1</th>
<th>+1</th>
<th>+2</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF</td>
<td>604Ω</td>
<td>953Ω</td>
<td>681Ω</td>
</tr>
<tr>
<td>RG</td>
<td>604Ω</td>
<td>-</td>
<td>681Ω</td>
</tr>
<tr>
<td>0.1dB Flatness</td>
<td>130MHz</td>
<td>100MHz</td>
<td>120MHz</td>
</tr>
</tbody>
</table>

As has been discussed, the CFB op amp is relatively insensitive to capacitance on the inverting input when it is used in the inverting mode (as in an I/V application). This is because the low inverting input impedance is in parallel with the external capacitance and tends to minimize its effect. In the non-inverting mode, however, even a few picofarads of stray inverting input capacitance may cause peaking and instability. Figure 2.3 shows the effects of adding summing junction capacitance to the inverting input of the AD8004 (SOIC package) for G = +2. Note that only 1pF of added inverting input capacitance (CJ) causes a significant increase in bandwidth and an increase in peaking. For G = –2, however, 5pF of additional inverting input capacitance causes only a small increase in bandwidth and no significant increase in peaking.

High speed VFB op amps are sensitive to stray inverting input capacitance when used in either the inverting or non-inverting mode.
DRIVING CAPACITIVE LOADS

From system and signal fidelity points of view, transmission line coupling between stages is best, and is described in some detail in the next section. However, complete transmission line system design may not always be possible or practical. In addition, various other parasitic issues need careful consideration in high performance designs. One such problem parasitic is amplifier load capacitance, which potentially comes into play for all wide bandwidth situations which do not use transmission line signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap loading) effects should always be considered. This is because PC board capacitance can build up quickly, especially for wide and long signal runs over ground planes insulated by a thin, higher K dielectric. For example, a 0.025” PC trace using a G-10 dielectric of 0.03” over a ground plane will run about 22pF/foot (Reference 1). Even relatively small load capacitance (i.e., <100 pF) can be troublesome, since while not causing outright oscillation, it can still stretch amplifier settling time to greater than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply detrimental, they are actually an anathema to high quality signals. However, before-the-fact designer knowledge still allows high circuit performance by employing various tricks of the trade to combat the capacitive loading. If it is not driven via a transmission line, remote signal circuitry should be checked for capacitive loading very carefully, and characterized as best possible. Drivers which face poorly defined load capacitance should be bullet-proofed accordingly with an appropriate design technique from the options list below.
Short of a true matched transmission line system, a number of ways exist to drive a load which is capacitive in nature while maintaining amplifier stability.

Custom capacitive load (cap load) compensation includes two possible options, namely a); overcompensation, and b); an intentionally forced-high loop noise gain allowing crossover in a stable region. Both of these steps can be effective in special situations, as they reduce the amplifier’s effective closed loop bandwidth, so as to restore stability in the presence of cap loading.

Overcompensation of the amplifier, when possible, reduces amplifier bandwidth so that the additional load capacitance no longer represents a danger to phase margin. As a practical matter however, amplifier compensation nodes to allow this are available on few high speed amplifiers. One such useful example is the AD829, compensated by a single capacitor at pin 5. In general, almost any amplifier using external compensation can always be over compensated to reduce bandwidth. This will restore stability against cap loads, by lowering the amplifier’s unity gain frequency.

Forcing a high noise gain, is shown in Figure 2.4, where the capacitively loaded amplifier with a noise gain of unity at the left is seen to be unstable, due to a $1/\beta$ - open loop rolloff intersection on the Bode diagram in an unstable $-12\text{dB/octave}$ region. For such a case, quite often stability can be restored by introducing a higher noise gain to the stage, so that the intersection then occurs in a stable $-6\text{dB/octave}$ region, as depicted at the diagram right Bode plot.

**CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY**

To enable a higher noise gain (which does not necessarily need to be the same as the stage’s signal gain), use is made of resistive or RC pads at the amplifier input, as in Figure 2.5. This trick is more broad in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally
allows use with any amplifier setup, even voltage followers. The technique adds an extra resistor $R_D$, which works against $R_F$ to force the noise gain of the stage to a level appreciably higher than the signal gain (which is unity in both cases here). Assuming that $C_L$ is a value which produces a parasitic pole near the amplifier's natural crossover, this loading combination would likely lead to oscillation due to the excessive phase lag. However with $R_D$ connected, the higher amplifier noise gain produces a new $1/\beta$ - open loop rolloff intersection, about a decade lower in frequency. This is set low enough that the extra phase lag from $C_L$ is no longer a problem, and amplifier stability is restored.

RAISING NOISE GAIN (DC OR AC) FOR FOLLOWER OR INVERTER STABILITY

A drawback to this trick is that the DC offset and input noise of the amplifier are raised by the value of the noise gain, when the optional $C_D$ is not present. But, when $C_D$ is used in series with $R_D$, the offset voltage of the amplifier is not raised, and the gained-up AC noise components are confined to a frequency region above $1/(2\pi \cdot R_D \cdot C_D)$. A further caution is that the technique can be somewhat tricky when separating these operating DC and AC regions, and should be applied carefully with regard to settling time (Reference 2). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

“Passive” cap load compensation, shown in Figure 2.6, is the most simple (and most popular) isolation technique available. It uses a simple “out-of-the-loop” series resistor $R_X$ to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.
As noted, this technique can be applied to virtually any amplifier, which is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor, RX. This resistor’s minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.

Drawbacks of this approach are the loss of bandwidth as RX works against CL, the loss of voltage swing, a possible lower slew rate limit due to I_MAX and CL, and a gain error due to the RX-RL division. The gain error can be optionally compensated with R_IN, which is ratioed to RF as RL is to RX. In this example, a ±100mA output from the op amp into CL can slew V_OUT at a rate of 100V/µs, far below the intrinsic AD811 slew rate of 2500V/µs. Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier is not otherwise protected, then an RX resistor of 50-100Ω should be used with virtually any amplifier facing capacitive loading. Although a non-inverting amplifier is shown, the technique is equally applicable to inverter stages.

With very high speed amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type problem. In such cases the amplifier must be stable driving the capacitance, but it must also preserve its best
bandwidth and settling time characteristics. To address this type of cap load case, \( R_S \) and \( C_L \) performance data for a specified settling time is most appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance, which in combination with \( C_L \) causes peaking or even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device \( F_L \), the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

In general, a small damping resistor (\( R_S \)) placed in series with \( C_L \) will help restore the desired response (see Figure 2.7). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simply stability or an acceptable amount of peaking has been used, but a more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of \( R_S - C_L \) curves exists, such as those of Figure 2.7. These data will aid in selecting \( R_S \) for a given application.

![AD8001 \( R_S \) REQUIRED FOR VARIOUS \( C_L \) VALUES](image)

The basic shape of this curve can be easily explained. When \( C_L \) is very small, no resistor is necessary. When \( C_L \) increases to some threshold value an \( R_S \) becomes necessary. Since the frequency at which the damping is required is related to the \( R_S \cdot C_L \) time constant, the \( R_S \) needed will initially increase rapidly from zero, and then will decrease as \( C_L \) is increased further. A relatively strict requirement, such as for 0.1%, settling will generally require a larger \( R_S \) for a given \( C_L \), giving a curve falling higher (in terms of \( R_S \)) than that for a less stringent requirement, such as...
20% overshoot. For the common gain configuration of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed loop gains lessen the problem dramatically, and will require less \( R_S \) for the same performance. The third (lower-most) curve illustrates this, demonstrating a closed loop gain of 10 \( R_S \) requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 2.5.

The recommended values for \( R_S \) will optimize response, but it is important to note that generally \( C_L \) will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large \( R_S \cdot C_L \) time constant will dominate the response. In any given application, the value for \( R_S \) should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

Active or “in-the-loop” cap load compensation can also be used as shown in Figure 2.8, and this scheme modifies the passive configuration to provide feedback correction for the DC & low frequency gain error associated with \( R_X \). In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers don’t allow the integrating connection of \( C_F \).

**ACTIVE "IN-LOOP" CAPACITIVE LOAD COMPENSATION CORRECTS FOR DC AND LF GAIN ERRORS**

![Circuit Diagram](image)

This circuit returns the DC feedback from the output side of isolation resistor \( R_X \), thus correcting for errors. AC feedback is returned via \( C_F \), which bypasses \( R_X/R_F \) at high frequencies. With an appropriate value of \( C_F \) (which varies with \( C_L \) for fixed resistances) this stage can be adjusted for a well damped transient response (Reference 2,3). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the DC errors can be very low. A drawback is the need to tune \( C_F \) to \( C_L \), as even if this is done well initially, any change to \( C_L \) will...
alter the response away from flat. The circuit as shown is useful for voltage feedback amplifiers only, because capacitor C_F provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of R_IN.

*Internal* cap load compensation involves the use of an amplifier which has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.

The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 2.9, a simplified diagram of an AD817 amplifier with internal cap load compensation, shows how it works. The cap load compensation is the C_F -resistor network shown around the unity gain output stage of the amplifier - note that the dotted connection of this network underscores the fact that it only makes its presence felt for certain load conditions.

**AD817 SIMPLIFIED SCHEMATIC ILLUSTRATES INTERNAL COMPENSATION FOR DRIVING CAPACITIVE LOADS**

Under normal (non-capacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the C_F network then sees a relatively small voltage drop, and has little or no effect on the AD817s high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the C_F network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner which is adaptive to the external
capacitance, $C_L$. As a point of reference, note that it requires 6.3mA peak current to support a 2Vp-p swing across a 100pF load at 10MHz.

Since this mechanism is resident in the amplifier output stage and it affects the overall compensation characteristics dynamically, it acts independent of the specific feedback hookup, as well as size of the external cap loading. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make it work (other than selecting an IC which employs it). Some amplifiers using internal cap load compensation are the AD847 and the AD817, and their dual equivalents, AD827 and AD826.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the $C_F$ network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits for lower-level outputs.

**RESPONSE OF INTERNAL CAP LOAD COMPENSATED AMPLIFIER VARIES WITH SIGNAL LEVEL**

(A) $V_{OUT} = 10\text{V p-p}$
Vertical Scale: 5V/div

(B) $V_{OUT} = 200\text{mV p-p}$
Vertical Scale: 100mV/div

Horizontal Scale: 500ns/div

AD817 INVERTER

$R_F = R_{IN} = 1\text{k}\Omega$

$R_L = 1\text{k}\Omega$, $C_L = 1\text{nF}$, $V_S = \pm15\text{V}$

The dynamic nature of this internal cap load compensation is illustrated in Figure 2.10, which shows an AD817 unity gain inverter being exercised at both high and low output levels, with common conditions of $V_S = \pm15\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 1\text{nF}$, and using 1kΩ input/feedback resistors. In both photos the input signal is on the top trace and the output signal is on the bottom trace, and the time scale is fixed. In the 10Vp-p output (A) photo at the left, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. This indicates that for this high level case, the bandwidth reduction due to $C_L$ is most effective. However, in the (B) photo at the right, the
200mVp-p output shows greater overshoot and ringing, for the lower level signal. The point is that the performance of the cap load compensated amplifier is signal dependent, but is always stable with any cap load.

Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion performance and load drive ability, and these factors influence amplifier performance in video applications. Though the network’s presence does not by any means make devices like the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase which are achievable with otherwise comparable amplifiers (for example, the AD818 which is an AD817 without the internal compensating network).

While the individual techniques for countering cap loading outlined above have various specific tradeoffs as noted, all of the techniques have a common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, then a matched transmission line system is the solution, and is discussed in more detail later in the chapter. As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem- just pick the right amplifier and forget about it. And indeed, that would seem the “panacea” solution for all cap load situations - if you use the “right” amplifier you never need to think about cap loading again. Could there be more to it?

Yes! The “gotcha” of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, without the Cp-resistor network. Like the old saying about no free lunches, if you care about attaining top-notch levels of high frequency AC performance, you should give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier could be a good choice. Such amplifiers are certainly easier to use, and relatively forgiving about loading issues. Some applications of this chapter illustrate the distortion point specifically, quoting performance in a driver circuit with/without the use of an internal cap load compensated amplifiers.

CABLE DRIVERS AND RECEIVERS

High quality video signals are best transmitted over terminated coaxial cable having a controlled characteristic impedance. The characteristic impedance is given by the equation $Z_0 = \sqrt{L/C}$ where $L$ is the distributed inductance per foot, and $C$ is the distributed capacitance per foot. Popular values are 50, 75, and 93 or 100Ω.

If a length of coaxial cable is terminated, it presents a resistive load to the driver. If left unterminated, however, it may present a predominately capacitive load to the driver depending on the output frequency. If the length of an unterminated cable is much less than the wavelength of the output frequency of the driver, then the load appears approximately as a lumped capacitance. For instance, at the audio frequency of 20kHz (wavelength ≈ 50,000 feet, or 9.5miles), a 5 foot length of unterminated 50Ω coaxial cable would appear as a lumped capacitance of
approximately 150pF (the distributed capacitance of coaxial cable is about 30pF/ft). At 100MHz (wavelength ≈ 10 feet), however, the unterminated coax must be treated as a transmission line in order to calculate the standing wave pattern and the voltage at the unterminated cable output.

Because of skin effect and wire resistance, coaxial cable exhibits a loss which is a function of frequency. This varies considerably between cable types. For instance the attenuation in at 100MHz of RG188A/U is 8dB/100ft, RG58/U is 5.5dB/100ft, and RG59/U 3.6dB/100ft (Reference 4).

Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (see Reference 5).

DRIVING CABLES

- All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not Controlled)
- The Characteristic Impedance is Equal to \( \sqrt{\frac{L}{C}} \), where L and C are the Distributed Inductance and Capacitance
- Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance
- Unterminated Transmission Lines Behave Approximately as Lumped Capacitance if the Wavelength of the Output Frequency is Much Greater than the Length of the Cable
  - Example: At 20kHz (Wavelength = 9.5 miles), 5 feet of Unterminated 50Ω Cable (30pF/ft) Appears Like 150pF Load
  - Example: At 100MHz (Wavelength = 10 feet), 5 feet of 50Ω Cable Must be Properly Terminated to Prevent Reflections and Standing Waves!!!!

It is useful to examine what happens for conditions of proper and improper cable source/load terminations. To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 2.12. The AD8001 drives 5 feet of 50Ω coaxial cable which is load-end terminated in the characteristic impedance of 50Ω. No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

The output of the cable was measured by connecting it directly to the 50Ω input of a 500MHz Tektronix 644A digitizing oscilloscope. The 50Ω resistor termination is
actually the input of the scope. The 50Ω load is not a perfect termination (the scope input capacitance is about 10pF), so some of the pulse is reflected out of phase back to the source. When the reflection reaches the op amp output, it sees the closed-loop output impedance of the op amp which, at 100MHz, is approximately 100Ω. Thus, it is reflected back to the load with no phase reversal, accounting for the negative-going "blip" which occurs approximately 16ns after the leading edge. This is equal to the round-trip delay of the cable (2•5ft•1.6 ns/ft=16ns). In the frequency domain (not shown), the cable mismatch will cause a loss of bandwidth flatness at the load.

**PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF LOAD-TERMINATED 50Ω COAXIAL CABLE**

Figure 2.13 shows a second case, the results of driving the same coaxial cable, but now used with both a 50Ω source-end as well as a 50Ω load-end termination. This case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier’s source termination resistor. The disadvantage is that there is a 2x gain reduction, because of the voltage division between the equal value source/load terminations. However, a major positive attribute of this configuration, with matched source and load terminations in conjunction with a low-loss cable, is that the best bandwidth flatness is ensured, especially at lower operating frequencies. In addition, the amplifier is operated under near optimum loading conditions, i.e., a resistive load.
Source-end (only) terminations can also be used as shown in Figure 2.14, where the op amp is source terminated by the 50Ω resistor which drives the cable. The scope is set for 1MΩ input impedance, representing an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100Ω load (the 50Ω source resistor in series with the 50Ω coax impedance. When the pulse reaches the load, a large portion is reflected in phase because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50Ω source resistance in series with the op amp closed loop output impedance (approximately 100Ω at the frequency represented by the 2ns risetime pulse edge). The reflected portion remains in phase, and appears at the scope input as the positive-going “blip” approximately 16ns after the leading edge.
From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100MHz. (Using the rule-of-thumb that bandwidth = 0.35/risetime). At video frequencies, either load-only, or source-only terminations may give acceptable results, but the data sheet should always be consulted to determine the op amp’s closed-loop output impedance at the maximum frequency of interest. A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy. It also places a burden on this amplifier to maintain a low output impedance at high frequencies.

Now, for a truly worst case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 150pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 2.15 shows the output of the AD8001 driving a lumped 160pF capacitance (including the scope input capacitance of 10pF). Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.
A High Performance Video Line Driver

The AD8047 and AD8048 VFB op amps have been optimized to offer outstanding performance as video line drivers. They utilized the “quad core” $g_m$ stage as previously described for high slew rate and low distortion. The AD8048 (optimized for $G = +2$) has a differential gain of 0.01% and a differential phase of 0.02°, making it suitable for HDTV applications. In the configuration shown in Figure 2.16, the 0.1dB bandwidth is 50MHz for ±5V supplies, slew rate is 1000V/µs, and 0.1% settling time is 13ns. Total quiescent current is 6mA (±5V), and quiescent power dissipation 60mW.
Differential Line Drivers/Receivers

Many applications require gain/phase matched complementary or differential signals. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of 2nd harmonic distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as in ADSL and HDSL.

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to design engineers. Differential techniques using high common-mode-rejection-ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies.

At audio frequencies, transformers, or products such as the SSM-2142 balanced line driver and SSM-2141/SSM-2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise. At high frequencies, small toroid transformers using bifilar windings are effective.

The problem of signal transmission at video frequencies is complex. Transformers are not effective, because the baseband video signal has low-frequency components down to a few tens of Hz. Video signals are generally single-ended, and therefore don’t adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive. Finally, designing high bandwidth, low distortion differential video drivers and receivers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make
use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Two solutions to the problem of differential transmission and reception are shown in Figure 2.17. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

**TWO APPROACHES FOR DIFFERENTIAL LINE DRIVING/RECEIVING**

![Diagram](image)

The second and most often used approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating in order to prevent a ground loop between the two systems. The common mode ground noise is rejected by the CMRR of the differential line receiver. The success of this approach depends upon the characteristics of the line receiver.

**Inverter-Follower Differential Driver**

The circuit of Figure 2.18 is useful as a high speed differential driver for driving high speed 10-12 bit ADCs, differential video lines, and other balanced loads at levels of 1-4Vrms. As shown it operates from ±5V supplies, but it can also be adapted to supplies in the range of ±5 to ±15V. When operated directly from ±5V as here, it minimizes potential for destructive ADC overdrive when higher supply voltage buffers drive a ±5V powered ADC, in addition to minimizing driver power.
In many of these differential drivers the performance criteria is high. In addition to low output distortion, the two signals should maintain gain/phase flatness. In this topology, two sections of an AD812 dual current feedback amplifier are used for the channel A & B buffers, U1A & U1B. This can provide inherently better open-loop bandwidth matching than the use of two singles (where bandwidth varies between devices from different manufacturing lots).

The two buffers here operate with precise gains of ±1, as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715Ω resistors- the value for using the AD812 on ±5V supplies.

In channel A, non-inverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network RFB1 and RG1(Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor RFB1, and no gain resistor at all. Here, with input resistor RG1 added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of RFB1-RG1, the signal gain is maintained at unity. Given the matched open loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction which greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for RG2-RFB2. Here a worst case 2% mis-match will result in less than 0.2dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.
If desired, phase matching is trimmed via $R_G_1$, so that the phase of channel A closely matches that of B. This can be done for new circuit conditions, by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as $R_G_1$ is adjusted for the best null conditions at the sum node. The A-B gain/phase matching is quite effective in this driver, with test results of the circuit as shown 0.04dB and 0.1° between the A and B output signals at 10MHz, when operated into dual 150Ω loads. The 3dB bandwidth of the driver is about 60MHz.

Net input impedance of the circuit is set to a standard line termination value such as 75Ω (or 50Ω), by choosing $R_{IN}$ so that the desired value results with $R_{IN}$ in parallel with $R_G_2$. In this example, an $R_{IN}$ value of 83.5Ω provides a standard input impedance of 75Ω when paralleled with 715Ω. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this is not totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813, with the third channel as a variable gain input buffer.

Cross-Coupled Differential Driver

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 2.19, by connecting AD8002 dual current feedback amplifier sections as cross-coupled inverters, their outputs are forced equal and opposite, assuring zero output common mode voltage.
The gain cell which results, U1A and U1B plus cross-coupling resistances \( R_X \), is fundamentally a differential input and output topology, but it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The gain of the stage from \( V_{IN} \) to \( V_{OUT} \) is:

\[
G = \frac{V_{OUT}}{V_{IN}} = \frac{2R_2}{R_1}
\]

where \( V_{OUT} \) is the differential output, equal to \( V_{OUTA} - V_{OUTB} \).

This relationship may not be obvious, so it can be derived as follows:

Using the conventional inverting op amp gain equation, the input voltage \( V_{IN} \) develops an output voltage \( V_{OUTB} \) given by:

\[
V_{OUTB} = -V_{IN} \frac{R_2}{R_1}.
\]

Also, \( V_{OUTA} = -V_{OUTB} \),

because \( V_{OUTA} \) is inverted by U1B.

However, \( V_{OUT} = V_{OUTA} - V_{OUTB} = -2V_{OUTB} \).

Therefore,

\[
V_{OUT} = -2\left(-V_{IN} \frac{R_2}{R_1}\right) = 2V_{IN} \frac{R_2}{R_1},
\]

and

\[
\frac{V_{OUT}}{V_{IN}} = \frac{2R_2}{R_1}.
\]

This circuit has some unique benefits. First, differential gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as in the case of a conventional current feedback amplifier. Thus, they are not highly critical as to value as long as the equivalent resistance seen by U1A is reasonably low (\( \leq 1k\Omega \) in this case). Third, the cell bandwidth can be optimized to the desired gain by a single optional resistor, \( R_3 \), as follows. If for instance, a net gain of 20 is desired (\( R_2/R_1=10 \)), the bandwidth would otherwise be reduced by roughly this amount, since without \( R_3 \), the cell operates with a constant gain-bandwidth product (working in the voltage feedback mode). With \( R_3 \) present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of \( R_3 \), which, given an appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.
In the circuit as shown, no R3 is necessary at the low working gain of 2 times differential, since the 511Ω RX resistors are already optimized for maximum bandwidth. Note that these four matched RX resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains as set by R2/R1, R3 can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

\[ R3 \approx \frac{R_{X}}{(R2 / R1) - 1} \]

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, C1, may be needed to optimize flatness of frequency response. In this example, a 0.9pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5-2pF. This capacitor is then value selected at board characterization for optimum frequency response.

For the dual trace, 1-500MHz swept frequency response plot of Figure 2.20, output levels were 0dBm into matched 50Ω loads, through back termination resistances R_TA and R_TB, at V_OUTA and V_OUTB. In this plot the vertical scale is 2dB/div, and it shows the 3dB bandwidth of the driver measuring about 250MHz, with peaking about 0.1dB. The four RX resistors along with R_TA and R_TB control low frequency amplitude matching, which was within 0.1dB in the lab tests, using 511Ω 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

FREQUENCY RESPONSE OF AD8002 CROSS-COUPLED DRIVER IS >250MHz (C1 = 0.9pF ± 0.1pF)

Due to the high gain-bandwidths involved with the AD8002, the construction of this circuit should follow RF rules, with the use of a ground plane, chip bypass capacitors
of zero lead length at the ±5V supply pins, and surface mount resistors for lowest inductance.

**4 Resistor Differential Line Receiver**

Figure 2.21 shows a low cost, medium performance line receiver using a high speed op amp rated for video use. It is actually a standard 4 resistor difference amplifier optimized for high speed, with a differential to single-ended gain of \( \frac{R_2}{R_1} \). Using low value, DC accurate/AC trimmed resistances for \( R_1-R_4 \) and a high speed, high CMR op amp provides the good performance.

**SIMPLE VIDEO LINE RECEIVER USING THE AD818 OP AMP**

Practically speaking however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst case CMR (in dB) of this circuit due to resistor mismatch is:

\[
CMR = 20 \log_{10} \left( 1 + \frac{R_2}{R_1} \cdot \frac{R_3}{R_4} \right).
\]

In this expression the term “\( Kr \)” is a single resistor tolerance in fractional form (1%=0.01, etc.), and it is assumed the amplifier has significantly higher CMR (≥100dB). Using discrete 1% metal films for \( R_1/R_2 \) and \( R_3/R_4 \) yields a worst case CMR of 34dB, 0.1% types 54dB, etc. Of course 4 random 1% resistors will on the average yield a CMR better than 34dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Ohmtek 1005, (Reference 6) which has a ratio match of 0.1%, which will provide a worst case low frequency CMR of 66 dB.
This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed ±5V supply rails in some cases without hazard. For operation with ±15V supplies, inputs should not exceed the supply rails.

At frequencies above 1MHz, the bridge balance is dominated by AC effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values. In a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5pF increments, for best high frequency CMR. Using designated PC pads, production values then would use the trimmed value. Good AC matching is essential to achieving good CMR at high frequencies. C1-C2 should be types similar physically, such as NPO (or other stable) ceramic chip style capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit. Alternately, a scheme for continuous gain control without interaction with CMR is to follow this receiver with a scaling amplifier/driver with adjustable gain. The similar AD828 dual amplifier allows this with the addition of only two resistors.

Video gain/phase performance of this stage is dependent upon the device used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of ±10 - ±15V, which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with low distortion video operation perform best. The circuit as shown can be used with supplies of ±5 to ±15V, but lowest NTSC video distortion occurs for supplies of ±10V or more, where differential gain/differential phase errors are less than 0.01%/0.05°. Operating at ±5V supplies, the distortion rises somewhat, but the lowest power drain of 70mW occurs.

One drawback to this circuit is that it does load a 75Ω video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

**Active Feedback Differential Line Receiver**

Fully integrating the line receiver function eliminates the resistor-related drawbacks of the 4 resistor line receiver, improving CMR performance, ease of use, and overall circuit flexibility. An IC designed for this function is the AD830 active feedback amplifier (Reference 7,8). Its use as a differential line receiver with gain is illustrated in Figure 2.22.
The AD830 operates as a feedback amplifier with two sets of fully differential inputs, available at pins 1-2 and 3-4, respectively. Internally, the outputs of the two stages are summed and drive a buffer output stage. Both input stages have high CMR, and can handle differential signals up to ±2V, and CM voltages can range up to –Vs+3V or +Vs–2.1V, with a ±1V differential input applied. While the AD830 does not normally need protection against CM voltages, if sustained transient voltage beyond the rails is encountered, an optional pair of equal value (≅200Ω) resistances can be used in series with pins 1-2.

In this device the overall feedback loop operates so that the differential voltages V1-2 and V3-4 are forced to be equal. Feedback is taken from the output back to one input differential pair, while the other pair is driven by a differential input signal. An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so CMR isn’t dependent on resistor bridges and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at DC.

The general expression for the U1 stage’s gain “G” is like a non-inverting op amp, or:

\[
G = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 + \frac{R2}{R1}
\]

For lowest DC offset, balancing resistor R3 is used (equal to R1 || R2).

In this example of a video “loop-through” connection, the input signal tapped from a coax line and applied to one input stage at pins 1-2, with the scaled output signal
tied to the second input stage between pins 3-4. With the R1-R2 feedback attenuation of 2/1, the net result is that the output of U1, is then equal to 2\cdot V_{IN}, i.e., a gain of 2.

Functionally, the input and local grounds are isolated by the CMR of the AD830, which is typically 75dB at frequencies below 1MHz, 60dB at 4.43MHz, and relatively supply independent.

With the addition of an output source termination resistor R_T, this circuit has an overall loaded gain of unity at the load termination, R_L. It is a ground isolating video repeater, driving the terminated 75\Omega output line, delivering a final output equal to the original input, V_{IN}.

NTSC video performance will be dependent upon supplies. Driving a terminated line as shown, the circuit has optimum video distortion levels for V_s = \pm15V, where differential gain is typically 0.06%, and differential phase 0.08°. Bandwidth can be optimized by the optional 5.1pF (or 12pF) capacitor, C_A, which allows a 0.1dB bandwidth of 10MHz with \pm15V operation. The differential gain and phase errors are about 2\times at \pm5V.

**HIGH SPEED CLAMPING AMPLIFIERS**

There are many situations where it is desirable to clamp the output of an op amp to prevent overdriving the circuitry which follows. Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high (V_H) and low (V_L) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to competing devices that use output-clamping. Recovery time from overdrive is less than 5ns.

The key to the AD8036 and AD8037’s fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. This new design reduces clamp errors by more than 10x over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.

Figure 2.23 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200V/\mu s, 240MHz high voltage gain, differential to single-ended amplifier) and A2 (a G=+1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.
The input clamp section is comprised of comparators \(C_H\) and \(C_L\), which drive switch S1 through a decoder. The unity-gain buffers in series with the \(+V_{IN}\), \(V_H\), and \(V_L\) inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision.

The two comparators have about the same bandwidth as A1 (240MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the input clamp circuit, consider the case where \(V_H\) is referenced to +1V, \(V_L\) is open, and the AD8036 is set for a gain of +1 by connecting its output back to its inverting input through the recommended 140\(\Omega\) feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects A1’s noninverting input.

If a 0V to +2V voltage ramp is applied to the AD8036’s \(+V_{IN}\) for the connection just described, \(V_{OUT}\) should track \(+V_{IN}\) perfectly up to +1V, then should limit at exactly +1V as \(+V_{IN}\) continues to +2V.

In practice, the AD8036 comes close to this ideal behavior. As the \(+V_{IN}\) input voltage ramps from zero to 1V, the output of the high limit comparator \(C_H\) starts in the off state, as does the output of \(C_L\). When \(+V_{IN}\) just exceeds \(V_H\) (practically, by about 18mV), \(C_H\) changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to \(V_H\), further increases in \(+V_{IN}\) have no effect on the AD8036’s output voltage. The AD8036 is now operating as a unity-gain buffer for the \(V_H\) input, as any variation in \(V_H\), for \(V_H > 1V\), will be faithfully produced at \(V_{OUT}\).

Operation of the AD8036 for negative input voltages and negative clamp levels on \(V_L\) is similar, with comparator \(C_L\) controlling S1. Since the comparators see the
voltage on the +VIN pin as their common reference level, the voltage V_H and V_L are defined as "High" or "Low" with respect to +VIN. For example, if VIN is set to zero volts, V_H is open, and V_L is +1V, comparator C_L will switch S1 to "C", so the AD8036 will buffer the voltage on V_L and ignore +VIN.

The performance of the AD8036/AD8037 closely matches the ideal just described. The comparator's threshold extends from 60mV inside the clamp window defined by the voltages on V_L and V_H to 60mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's + input makes a continuous transition from say, VIN to V_H as the input voltage traverses the comparator's input threshold from 0.9V to 1.0V for V_H = 1.0V.

The practical effect of the non-ideal operation is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 2.24 is a graph of V_OUT versus VIN for the AD8036 and a typical output clamp amplifier. Both amplifiers are set for G=+1 and V_H = +1V.

**COMPARISON BETWEEN INPUT AND OUTPUT CLAMPING**

![Graph showing comparison between input and output clamping](image)

The worst case error between V_OUT (ideally clamped) and V_OUT (actual) is typically 18mV times the amplifier closed-loop gain. This occurs when VIN equals V_H (or V_L). As VIN goes above and/or below this limit, V_OUT will stay within 5mV of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8V, and can have an output voltage as far as 200mV over the clamp limit. In addition, since the output clamp causes the amplifier to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.
It is important that a clamped amplifier such as the AD8036/AD8037 maintain low levels of distortion when the input signals approach the clamping voltages. Figure 2.25 shows the second and third harmonic distortion for the amplifiers as the output approaches the clamp voltages. The input signal is 20MHz, the output signal is 2V peak-to-peak, and the output load is 100Ω.

Recovery from step voltage which is two times over the clamping voltage is shown in Figure 2.26. The input step voltage starts at +2V and goes to 0V (left-hand traces on scope photo). The input clamp voltage (V_H) is set at +1V. The right-hand trace shows the output waveform. The key specifications for the AD8036/AD8037 clamped amplifiers are summarized in Figure 2.27.
AD8036/AD8037 OVERDRIVE (2x) RECOVERY

![Graph showing overdrive recovery](image)

**AD8036/AD8037 SUMMARY SPECIFICATIONS**

- Proprietary Input Clamping Circuit with Minimized Nonlinear Clamping Region
- Small Signal Bandwidth: 240MHz (AD8036), 270MHz (AD8037)
- Slew Rate: 1500V/µs
- 1.5ns Overdrive Recovery
- Low Distortion: -72dBc @ 20MHz (500Ω load)
- Low Noise: 4.5nv/√Hz, 2pA/√Hz
- 20mA Supply Current on ±5V

---

Figure 2.28 shows the AD9002 8-bit, 125MSPS flash converter driven by the AD8037 (240MHz bandwidth) clamping amplifier. The clamp voltages on the AD8037 are set to +0.55 and −0.55V, referenced to the ±0.5V input signal, with the external resistive dividers. The AD8037 also supplies a gain of two, and an offset of −1V (using the AD780 voltage reference), to match the 0 to −2V input range of the AD9002 flash converter. The output signal is clamped at +0.1V and −2.1V. This multi-function clamping circuit therefore performs several important functions as
well as preventing damage to the flash converter which occurs if its input exceeds +0.5V, thereby forward biasing the substrate diode. The 1N5712 Schottky diode adds further protection during power-up.

**AD9002 8-BIT, 125MSPS FLASH CONVERTER DRIVEN BY AD8037 CLAMP AMPLIFIER**

The feedback resistor, \( R_2 = 301\Omega \), is selected for optimum bandwidth per the data sheet recommendation. For a gain of two, the parallel combination of \( R_1 \) and \( R_3 \) must also equal \( R_2 \):

\[
\frac{R_1 \cdot R_3}{R_1 + R_3} = R_2 = 301\Omega \\
\text{(nearest 1% standard resistor value).}
\]

In addition, the Thevenin equivalent output voltage of the AD780 +2.5V reference and the \( R_3/ R_1 \) divider must be +1V to provide the –1V offset at the output of the AD8037.

\[
\frac{2.5 \cdot R_1}{R_1 + R_3} = 1\text{volt}
\]

Solving the equations yields \( R_1 = 499\Omega \), \( R_3 = 750\Omega \) (using the nearest 1% standard resistor values).

Other input and output voltages ranges can be accommodated by appropriate changes in the external resistors.

Further examples of applications of these fast clamping op amps are given in Reference 9.
**SINGLE-SUPPLY/RAIL-TO-RAIL CONSIDERATIONS**

The market is driving high speed amplifiers to operate at lower power on lower supply voltages. High speed bipolar processes, such as Analog Devices' CB and XFCB, are basically 12V processes, and circuits designed on these processes are generally limited to ±5V power supplies (or less). This is ideal for high speed video, IF, and RF signals, which rarely exceed 5V peak-to-peak.

The emphasis on low power, battery-operated portable communications and instrumentation equipment has brought about the need for ICs which operate on single +5V, and +3V, and lower supplies. The term *single-supply* has various implications, some of which are often further confused by marketing hype.

There are many obvious reasons for lower power dissipation, such as the ability to function without fans, reliability issues, etc. There are, therefore, many applications for single-supply devices other than in systems which have only one supply voltage. For example, the lower power dissipation of a single-supply ADC may be the reason for its selection, rather than the fact that it requires just one supply.

There are also systems which truly operate on a single power supply. In such cases, it can often be difficult to maintain DC coupling from a transducer all the way through to the ADC. In fact, AC coupling is often used in single-supply systems, with DC restoration preceding the ADC. This may be required to prevent the loss of dynamic range which would otherwise occur because of the need to provide adequate headroom to an AC coupled signal of arbitrary duty cycle. In the AC-coupled portions of such systems, a "false-ground" is often created, usually centered between the rails.

There are other disadvantages associated with lower power supply voltages. Signal swings are limited, therefore high-speed single-supply circuits tend to be more sensitive to corruption by wideband noise, etc. The single-supply op amp and ADC usually utilize the same power bus that supplies the digital circuits, making proper filtering and decoupling extremely critical.

In order to maximize the signal swing in single-supply circuits, it is desirable that a high speed op amp utilize as much of the supply range as possible on both the input and output. Ideally, a true *rail-to-rail* input op amp has an input common-mode range that includes both supply rails, and an output range which does likewise. This makes for some interesting tradeoffs and compromises in the circuit design of the op amp.

In many cases, an op amp may be fully specified for both dual ±5V and single-supply operation but neither its input nor its output can actually swing closer than about 1V to either supply rail. Such devices must be used in applications where the input and output common-mode restrictions are not violated. This generally involves offsetting the inputs using a false ground reference scheme.

To summarize, there are many tradeoffs involved in single-supply high-speed designs. In many cases, using devices specified for operation on +5V, but without true rail inclusive input/output operation can give good performance. Amplifiers are
also becoming available that are true single supply rail-to-rail devices. Understanding single-supply rail-to-rail input and output limitations is easy if you understand a few basics about the circuitry inside the op amp. We shall consider input and output stages separately.

### HIGH SPEED SINGLE SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - Lower Power
  - Battery Operated Portable Equipment
  - Simplifies Power Supply Requirements (one voltage)

- **Design Tradeoffs:**
  - Limited Signal Swings Increase Sensitivity to Noise
  - Usually Share Noisy Digital Power Supply
  - DC Coupling Throughout is Difficult
  - Rail-to-Rail Input and Output Increases Signal Swing, but not Required in All Applications
  - Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs

There is some demand for high-speed op amps whose input common-mode voltage includes both supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common-mode range close to the supplies or one that includes one of the supplies is necessary, but input rail-to-rail operation is not.

In many single-supply applications, it is required that the input go to only one of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 2.30 (circuit used in the AD8041, AD8042, AD8044). The input common-mode range of such an op amp extends from about 200mV below the negative supply to within about 1V of the positive supply. If the stage is designed with N-channel JFETs (AD820/AD822/AD823/AD824), the input common-mode range would also include the negative rail.
The input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input common-mode range would include the positive rail and to within about 1V of the negative rail; however, this requirement typically occurs in applications such as high-side current sensing, a low-frequency measurement application. The OP282/OP482 input stage uses the P-channel JFET input pair whose input common-mode range includes the positive rail.

True rail-to-rail input stages require two long-tailed pairs (see Figure 2.31), one of NPN bipolar transistors (or N-channel JFETs), the other of PNP transistors (or N-channel JFETs). These two pairs exhibit different offsets and bias currents, so when the applied input common-mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources (I1 and I2) remain active throughout the entire input common-mode range, amplifier input offset voltage is the average offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply.
Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the common-mode input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over part of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair somewhere along the input common-mode voltage range. Devices like the AD8031/AD8032 (specified for ±5V, +5V, +3V, and +2.5V) have a common-mode crossover threshold at approximately 1V below the positive supply. The PNP differential input stage is active from about 200mV below the negative supply to within about 1V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common-mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Applications which require true rail-rail inputs should therefore be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.
Figure 2.32 shows two typical high-speed op amp output stages. The emitter-follower stage is widely used, but its output voltage range is limited to within about 1V of either supply voltage. This is sufficient for many applications, but the common-emitter stage (used in the AD8041/8042/8044/8031/8032 and others) allows the output to swing to within the transistor saturation voltage, $V_{CE(SAT)}$, of the rails. For small amounts of load current (less than 100µA), the saturation voltage may be as low as 5 to 20mV, but for higher load currents, the saturation voltage can increase to several hundred millivolts (for example, 500mV at 50mA). This is illustrated in Figure 2.33 for the AD8042 (zero-volts in, rail-to-rail output). The solid curves show the output saturation voltage of the PNP transistor (output sourcing current), and the dotted curves the NPN transistor (sinking current). The saturation voltage increases with increasing temperature as would be expected.

**HIGH SPEED SINGLE SUPPLY OP AMP OUTPUT STAGES**

![Emitter Follower and Common Emitter Schematic Diagrams](image-url)
An output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions, and in much lower frequency amplifiers. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically 100Ω).

**SINGLE SUPPLY OP AMP APPLICATIONS**

The following section illustrates a few applications of op amps in single-supply circuits. All of the op amps are fully specified for both ±5V and +5V (and +3V where the design supports it). Both rail-to-rail and non-rail-to-rail applications are shown.

**A Single-Supply 10-bit 20MSPS ADC Direct-Coupled Driver Using the AD8011**

The circuit in Figure 2.34 shows the AD8011 op amp driving the AD876 10-bit, 20MSPS ADC in a direct-coupled application. The input and output common-mode voltage of the AD8011 must lie between approximately +1 and +4V when operating on a single +5V supply. The input range of the AD876 is 2V peak-to-peak centered around a common-mode value of +2.6V, well within the output voltage range of the AD8011. The upper and lower range setting voltages are +1.6V and +3.6V and are supplied externally to the AD876. They are easily derived from a resistor divider driven by a reference such as the REF198 (+4.096V). The two taps on the resistor divider should be buffered using precision single-supply op amps such as the AD822 (dual).
The source is represented as a 2V video signal referenced to ground. (The equivalent of a current generator of 0 to 27mA in parallel with the 75Ω source resistor. The termination resistor, RT, is selected such that the parallel combination of RT and R1 is 75Ω. The peak-to-peak swing at the termination resistor is 1V, so the AD8011 must supply a gain of two.

The non-inverting input of the AD8011 is biased to a common-mode voltage of +1.6V (well within its allowable common-mode range). R3 is calculated as follows:

When the source voltage is zero-volts, there is a current of 3.0mA flowing through R1 (499Ω) and into 40.6Ω to ground (the equivalent parallel combination of the 75Ω source and the 88.7Ω termination resistor is 40.6Ω). The output of the AD8011 should be +3.6V under these conditions. This means that 2mA must flow through R2. Therefore R3 (connected to the +3.6V source) must supply 1.0mA into the summing junction (+1.6V), and therefore its value must be 2000Ω.

The input of the AD876 has a series MOSFET switch that turns on and off at the sampling frequency. This MOSFET is connected to a hold capacitor internal to the device. The on impedance of the MOSFET is about 50Ω, while the hold capacitor is about 5pF.

In a worst case condition, the input voltage to the AD876 will change by a full-scale value (2V) in one sampling cycle. When the input MOSFET turns on, the output of the op amp will be connected to the charged hold capacitor through the series resistance of the MOSFET. Without any other series resistance, the instantaneous current that flows would be 40mA. This causes settling problems for the op amp.
The series 100Ω resistor limits the instantaneous current to about 13mA. This resistor cannot be made too large, or the high frequency performance will be affected. In practice, the optimum value is often determined experimentally.

The sampling MOSFET of the AD876 is closed for half of each cycle (25ns when sampling at 20MSPS). Approximately 7 time constants are required for settling to 10 bits. The series 100Ω resistor along with the 50Ω on resistance and the 5pF hold capacitor form a time constant of about 750ps. These values leave a comfortable margin for settling. Overall, the AD8011 provides adequate buffering for the AD876 ADC without introducing distortion greater than that of the ADC itself.

**A 10-Bit, 40MSPS ADC Low-Distortion Single-Supply ADC Driver Using the AD8041 Op Amp**

A DC coupled application which requires the rail-to-rail output capability of the AD8041 is shown in Figure 2.35 as a driver for the AD9050 10-bit, 40MSPS single-supply ADC. The input range of the AD9050 is 1V p-p centered around +3.3V. The maximum input signal is therefore +3.8V. The non-inverting input of the AD8041 is driven with a common-mode voltage of +1.65V which is derived from the unused differential input of the AD9050. This allows the op amp to act as a level shifter for the ground-referenced bipolar input 1V p-p signal, with unity gain as determined by the 1kΩ resistors, R1 and R2.

Op amps with complementary emitter follower outputs such as the AD8011 (operating on +5V) generally will exhibit high frequency distortion for sinewaves with full-scale amplitudes of 1V p-p centered at +3.3V. Because of its common emitter output stage, however, the AD8041 is capable of driving the AD9050, while maintaining a distortion floor of greater than 66dB with a 4.9MHz fullscale input (see Figure 2.36).
Single-Supply RGB Buffer

Op amps such as the AD8041/AD8042/ and AD8044 can provide buffering of RGB signals that include ground while operating from a single +3V or +5V supply. The signals that drive an RGB monitor are usually supplied by current output DACs that operate from a single +5V supply. Examples of such are triple video DACs like the ADV7120/21/22 from Analog Devices.

During the horizontal blanking interval, the current output of the DACs goes to zero, and the RGB signals are pulled to ground by the termination resistors. If more than one RGB monitor is desired, it cannot simply be connected in parallel because it will provide an additional termination. Therefore, buffering must be provided before connecting a second monitor.

Since the RGB signals include ground as part of their dynamic output range, it has previously been required to use a dual supply op amp to provide this buffering. In some systems, this is the only component that requires a negative supply, so it can be quite inconvenient to incorporate this multiple monitor feature.

Figure 2.37 shows a diagram of one channel of a single supply gain-of-two buffer for driving a second RGB monitor. No current is required when the amplifier output is at ground. The termination resistor at the monitor helps pull the output down at low voltage levels.
Figure 2.38 shows the output of such a buffer operating from a single +3V supply and driven by the Blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700mV peak. The output of the AD8041 is +1.4V with the termination resistors providing a divide-by-two. The Red and Green signals can be buffered in the same manner with a duplication of this circuit. Another possibility is to use the quad AD8044 single-supply op amp.

**INPUT/OUTPUT OF SINGLE SUPPLY RGB BUFFER OPERATING ON +3V**
Single-Supply Sync Stripper

Some RGB monitors use only three cables total and carry the synchronizing signals and the Green (G) signal on the same cable. The sync signals are pulses that go in the negative direction from the blanking level of the G signal.

In some applications, such as prior to digitizing component video signals with ADCs, it is desirable to remove or strip the sync portion from the G signal. Figure 2.39 is a circuit using the AD8041 running on a single +5V supply that performs this function.

![SINGLE SUPPLY VIDEO SYNC STRIPPER](image)

The upper waveform in Figure 2.40 shows the Green plus sync signal that is output from an ADV7120, a single supply triple video DAC. Because the DAC is single supply, the lowest level of the sync tip is at ground or slightly above. The AD8041 is set from a gain of two to compensate for the divide-by-two of the output terminations. The reference voltage for R1 should be twice the DC blanking level of the G signal. If the blanking level is at ground and the sync tip is negative, as in some dual supply systems, then R1 can be tied to ground. In either case, the output will have the sync removed and have the blanking level at ground.
A Single-Supply Video Line Driver with Zero-Volt Output,
Eamon Nash

When operated with a single supply, the AD8031 80MHz rail-to-rail voltage feedback op amp has optimum distortion performance when the signal has a common mode level of \( V_s/2 \), and when there is about 500mV of headroom to each rail. If low distortion is required for signals which swing close to ground, an emitter follower can be used at the op amp output.

Figure 2.41 shows the AD8031 configured as a single supply gain-of-two line driver. With the output driving a back terminated 50Ω line, the overall gain is unity from Vin to Vout. In addition to minimizing reflections, the 50Ω back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the AD8031 stays about 700mV above ground. Using this circuit excellent distortion is obtained even when the output signal swings to within 50mV of ground. The circuit was tested at 500kHz and 2MHz using a single +5V supply. For the 500kHz signal, THD was 68dBc with a peak-to-peak swing at Vout of 1.85V (50mV to +1.9V). This corresponds to a signal at the emitter follower output of 3.7V p-p (100mV to 3.8V). Data was taken with an output signal of 2MHz, and a THD of 55dBc was measured with a Vout of 1.55V p-p (50mV to 1.6V).
This circuit can also be used to drive the analog input of a single supply high speed ADC whose input voltage range is ground-referenced. In this case, the emitter of the external transistor is connected directly to the ADC input. A peak positive voltage swing of approximately 3.8V is possible before significant distortion begins to occur.

**Headroom Considerations in AC-Coupled Single-Supply Circuits**

The AC coupling of arbitrary waveforms can actually introduce problems which don't exist at all in DC coupled or DC restored systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are AC coupled.

In Figure 2.42 (A), an example of a 50% duty cycle square wave of about 2Vp-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5V supply amplifier. Assume that the amplifier has a complementary emitter follower output and can only swing to the limited DC levels as marked, about 1V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.
Since standard video waveforms do vary in duty cycle as the scene changes, the point is made that low distortion operation on AC coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3Vp-p output swing available before clipping, and it must cleanly reproduce an arbitrary waveform, then the maximum allowable amplitude is less than 1/2 of this 3Vp-p swing, that is <1.5Vp-p. An example of violating this criteria is the 2Vp-p waveform of Figure 2.42, which is clipping for both the high and low duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an even more conservative criteria for lowest distortion operation such as composite NTSC video amplifiers.

Figure 2.43 shows a single supply gain-of-two composite video line driver using the AD8041. Since the sync tips of a composite video signal extend below ground, the input must be AC coupled and shifted positively to prevent clipping during negative excursions. The input is terminated in 75Ω and AC coupled via the 47µF to a voltage divider that provides the DC bias point to the input. Setting the optimal common-mode bias voltage requires some understanding of the nature of composite video signals and the video performance of the AD8041.
As discussed above, signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after AC coupling. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle, and vice versa.

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame, but occasionally has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for only about 75% of the time.

As a result of the duty cycle variations between the two extremes presented above, a 1V p-p composite video signal that is multiplied by a gain-of-two requires about 3.2V p-p of dynamic voltage swing at the output for the op amp to pass a composite video signal of arbitrary duty cycle without distortion.

The AD8041 not only has ample signal swing capability to handle the dynamic range required, but also has excellent differential gain and phase when buffering these signals in an AC coupled configuration.

To test this, the differential gain and phase were measured for the AD8041 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect is that the sync tips become compressed before the differential gain
and phase are adversely affected. Thus, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6V. Thus, the highest video level should be kept at least 0.6V below the positive supply rail.

Taking the above into account, it was found that the optimal point to bias the non-inverting input was at +2.2V DC. Operating at this point, the worst case differential gain was 0.06% and the differential phase 0.06°.

The AC coupling capacitors used in the circuit at first glance appear quite large. A composite video signal has a lower frequency band edge of 30Hz. The resistances at the various AC coupling points - especially at the output - are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors are required. For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slight observable change in the picture quality.

**Single-Supply AC Coupled Single-Ended-to-Differential Driver**

The circuit shown in Figure 2.44 provides a flexible solution to differential line driving in a single-supply application and utilizes the dual AD8042. The basic operation of the cross-coupled configuration has been described earlier in this section. The input, \( V_{IN} \), is a single-ended signal that is capacitively coupled into the feedforward resistor, \( R_1 \). The non-inverting inputs of each half of the AD8042 are biased at +2.5V. The gain from single-ended input to differential output is equal to \( 2R_2/R_1 \). The gain can be varied by changing one resistor (either \( R_1 \) or \( R_2 \)).

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![Single-Supply AC Coupled Differential Driver Circuit](image-url)
HIGH SPEED VIDEO MULTIPLEXING WITH OP AMPS UTILIZING DISABLE FUNCTION

A common video circuit function is the multiplexer, a stage which selects one of "N" video inputs and transmits a buffered version of the selected signal to the output. A number of video op amps (AD810, AD813, AD8013) have a disable mode which, when activated by applying the appropriate level to a pin on the package, disables the op amp output stage and drops the power to a lower value.

In the case of the AD8013 (triple current-feedback op amp), asserting any one of the disable pins about 1.6V from the negative supply will put the corresponding amplifier into a disabled, powered-down state. In this condition, the amplifier’s quiescent current drops to about 0.3mA, its output becomes a high impedance, and there is a high level of isolation from the input to the output. In the case of the gain-of-two line driver, for example, the impedance at the output node will be about equal to the sum of the feedback and feedforward resistors (1.6kΩ) in parallel with about 12pF capacitance. Input-to-output isolation is about 66dB at 5MHz.

Leaving the disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pin is about 40kΩ in parallel with 5pF. When driven to 0V, with the negative supply at –5V, about 100µA flows into the disable pin.

When the disable pins are driven by CMOS logic, on a single +5V supply, the disable and enable times are about 50ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the disable pins.

The AD8013’s input stages include protection from the large differential voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3V. The high input-to-output isolation will be maintained for voltages below this limit.

Wiring the amplifier outputs together as shown in Figure 2.45 will form a 3:1 multiplexer with about 50ns switching time between channels. The 0.1dB bandwidth of the circuit is 35MHz, and the OFF channel isolation is 60dB at 10MHz. The simple logic level-shifting circuit shown on the diagram does not significantly affect switching time.

The resistors were chosen as follows. The feedback resistor R2 of 845Ω was chosen first for optimum bandwidth of the AD8013 current feedback op amp. When any given channel is ON, it must drive both the termination resistor RL, and the net dummy resistance, RX/2, where RX is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity plus an effective source resistance of 75Ω, the other resistor values must be as shown.
Configuring two amplifiers as unity gain followers and using the third to set the gain results in a high performance 2:1 multiplexer as shown in Figure 2.46. The circuit takes advantage of the very low crosstalk between the amplifiers and achieves the OFF channel isolation shown in Figure 2.47. The differential gain and phase performance of the circuit is 0.03% and 0.07°, respectively.

2:1 VIDEO MULTIPLEXER
Closely related to the multiplexers described above is a programmable gain video amplifier, or PGA, as shown in Figure 2.48. In the case of the AD813, the individual op amps are disabled by pulling the disable pin about 2.5V below the positive supply. This puts the corresponding amplifier in its powered down state. In this condition, the amplifier’s quiescent supply current drops to about 0.5mA, its output becomes a high impedance, and there is a high level of isolation between the input and the output. Leaving the disable pin disconnected (floating) will leave the amplifier operational, in the enabled state. The input impedance of the disable pins is about 35kΩ in parallel with 5pF. When grounded, about 50µA flows out of a disable pin when operating on ±5V supplies. The switching threshold is such that the disable pins can be driven directly from +5V CMOS logic with no level shifting (as was required in the previous example).
With a two-line digital control input, this circuit can be set up to provide 3 different gain settings. This makes it a useful circuit in various systems which can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, etc. The gains can be binary related as here, or they can be arbitrary. An extremely useful feature of the AD813 CFB current feedback amplifier is the fact that the bandwidth does not reduce as gain is increased. Instead, it stays relatively constant as gain is raised. Thus more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product VFB amplifier type.

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can vary by adjustment of the R2/R3 or R4/R5 ratios. For the gain range and values shown, the PGA will be able to maintain a 3dB bandwidth of about 50MHz or more for loading as shown (a high impedance load of 1kΩ or more is assumed). Fine tuning the bandwidth for a given gain setting can be accomplished by lowering the resistor values at the higher gains, as shown in the circuit, where for G=1, R1=750Ω, for G=2, R2=649Ω, and for G=4, R4=301Ω.

**VIDEO MULTIPLEXERS AND CROSSPOINT SWITCHES**

Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 100ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch "on" resistance with signal level (called $R_{on}$ modulation) introduces unwanted distortion and degradation.
in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies.

Functional block diagrams of the AD8170/8174/8180/8182 bipolar video multiplexer are shown in Figure 2.49. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10ns to 0.1%. The AD8170/8174 muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80dB for the entire family. Key specifications are shown in Figure 2.50.

**AD8170/8174/8180/8182 BIPOLAR VIDEO MULTIPLEXERS**

**AD817X AND AD818X MULTIPLEXER KEY SPECIFICATIONS**

- **10ns Switching Time**
- **Wide Bandwidth (-3dB BW):**
  - 200MHz (AD817X)
  - 600MHz (AD818X)
- **Gain Flatness (0.1dB):**
  - 80MHz (AD817X)
  - 150MHz (AD818X)
- **0.02% / 0.02° Differential Gain and Phase (AD817X, RL = 150Ω)**
- 0.02% / 0.03° Differential Gain and Phase (AD818X, $R_L = 1k\Omega$)
- Off-Channel Isolation and Crosstalk > –80dB @ 10MHz
- Low Power (±5V Supplies):
  - AD8170 - 65mW
  - AD8174 - 85mW
  - AD8180 - 35mW
  - AD8182 - 70mW

Figure 2.51 shows an application circuit for three AD8170 2:1 muxes where the RGB monitor can be switched between two computers. The AD8174 4:1 mux is used in Figure 2.52 to allow a single high speed ADC to digitize the RGB outputs of a scanner. Figure 2.53 shows two AD8174 4:1 muxes expanded into an 8:1 mux.

**DUAL SOURCE RGB MULTIPLEXER USING THREE 2:1 MUXES**
The AD8116 extends the concepts above to yield a 16×16 buffered video crosspoint switch matrix (Figure 2.54). The 3dB bandwidth is greater than 200MHz, and the 0.1dB gain flatness extends to greater than 40MHz. Channel switching time is less than 30ns to 0.1%. Crosstalk is 70dB and isolation is 90dB (both measured at 10MHz). Differential gain and phase is 0.01% and 0.01° for a 150Ω load. Total power dissipation is 900mW on ±5V supplies.
The AD8116 includes output buffers which can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control which can accommodate "daisy chaining" of several devices. The AD8116 is packaged in a 128-pin TQFP package. Key specifications for the device are summarized in Figure 2.55.
**AD8116 CROSSPOINT SWITCH KEY SPECIFICATIONS**

- 16×16 Buffered Inputs and Outputs
- Output Buffer Disable Feature Allows Expansion
- 3dB Bandwidth 200MHz, 0.1dB Bandwidth 40MHz
- 30ns Switching to 0.1%
- Differential Gain 0.01%, Differential Phase 0.01°
- Power Dissipation: 900mW (±5V Supplies)
- 128-pin TQFP, 0.36 Square Inches Area

**HIGH POWER LINE DRIVERS AND ADSL**

ADSL (Asymmetric Digital Subscriber Line) uses the current subscriber line connection to the central office to transmit data as high as 8Mbps, almost 300 times the speed of the fastest traditional modem. ADSL uses the entire bandwidth (approximately 1MHz) of the connection in addition for the modulation scheme called Discrete Multi Tone (DMT).

Although high-speed fiber links already exist, it is still too difficult and expensive to bring them directly to every residence. ADSL uses the existing infrastructure for “the last mile” connecting the home and the local central office (which already has a high-speed fiber link to the national network).

Many applications are uneven (asymmetric) in their bandwidth needs - sending more information in one direction than the other. Typically, a user will request a video channel, ask for information from a central database, or view complex graphical images on a web page. All of these applications require considerable bandwidth. In contrast, the user may only send commands or files back up to the server. Realizing this, ADSL was designed to deliver a bigger downstream capacity to the home, while having a smaller two-way capacity.

Key to the ADSL system is the requirement for a low-distortion differential drive amplifier which delivers approximately 40V p-p into a 60Ω differential load impedance. The AD815 dual high current driver can deliver 40V p-p differential into a 50Ω load (corresponding to 400mA peak current!) using the application circuit shown in Figure 2.56. Low harmonic distortion is also required for ADSL applications, since it affects system bit error rates. The typical distortion of the device is shown in Figure 2.57 for 50Ω and 200Ω differential loads.
There are three AD815 models, two are available in a 15-pin power package, and the third as a 24-pin thermally enhanced SOIC. The 15-pin power package (AD815AY-through hole and AD815AVR-surface mount) has a low thermal resistance ($\theta_{JA} = 41^\circ$C/W) which can be reduced considerably (to $\theta_{JA} = 16^\circ$C/W) by connecting the package to an area of copper which acts as a heat sink. The AD815 incorporates a thermal shutdown circuit to protect the die from thermal overload.
The AD815 also has applications as a general purpose high current coil, transformer, or twisted pair cable driver, a CRT convergence adjustment control, or a video signal distribution amplifier. Each amplifier in the AD815 is capable of driving 6 back-terminated 75Ω video loads with a differential gain and phase of 0.05% and 0.45° respectively.

**HIGH SPEED PHOTODIODE PREAMPS**

Photodiodes generate a small current which is proportional to the level of illumination. They have many applications ranging from precision light meters to high-speed fiber optic receivers.

The equivalent circuit for a photodiode is shown in Figure 2.58. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent (I_sc) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color temperature of 2850K. At 100fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit current is usually in the picoamps to hundreds of microamps range for small area (less than 1mm²) diodes.

![PHOTODIODE EQUIVALENT CIRCUIT](image)

The short circuit current is very linear over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage drop across the photodiode varies logarithmically with light level, but, because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance is usually in the order of several hundred kΩ to more than 1GΩ at room temperature, and decreases by a factor of two for every 10°C rise in
temperature. Diode capacitance is a function of junction area and the diode bias voltage. A value of 10 to 50pF at zero bias is typical for small area diodes.

Photodiodes may either be operated with zero bias (photovoltaic mode) or reverse bias (photoconductive mode) as shown in Figure 2.59. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode. Under reverse bias conditions, a small amount of current called dark current will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode, the diode noise is basically the thermal noise generated by the shunt resistance. In the photoconductive mode, shot noise due to conduction is an additional source of noise. Photodiodes are usually optimized during the design process for use in either the photovoltaic mode or the photoconductive mode, but not both.

**PHOTODIODE MODES OF OPERATION**

![Photodiode Modes of Operation Diagram]

- **PHOTOVOLTAIC**
  - Zero Bias
  - No Dark Current
  - Precision Applications
  - Low Noise (Johnson)

- **PHOTOCONDUCTIVE**
  - Reverse Bias
  - Dark Current Exists
  - High Speed Applications
  - Higher Noise (Johnson + Shot)

Optimizing photodiode preamplifiers is probably one of the most challenging of design problems, especially if high bandwidth and direct coupling is required. Figure 2.60 shows a basic photodiode preamp designed with an op amp connected as a current-to-voltage converter.
The sensitivity of the circuit is determined by the amount of photodiode current multiplied by the feedback resistor \( R_2 \). The key parameters of the diode (see Figure 2.61) are its sensitivity (output current as a function of illumination level), dark current (the amount of current which flows due to the reverse bias voltage when the diode is not illuminated), risetime, shunt capacitance, and shunt resistance.

The key parameters of the op amp are its input voltage and current noise, bias current, unity gain-bandwidth product, \( f_u \), and input capacitance, \( C_{in} \).

The HP 5082-4204 PIN Photodiode will be used as an example for our discussion. Its characteristics are given in Figure 2.61. It is typical of many commercially available PIN photodiodes. As in most high-speed photodiode applications, the diode is operated in the reverse-biased or photoconductive mode. This greatly lowers the diode junction capacitance, but causes a small amount of dark current to flow even when the diode is not illuminated (we will show a circuit which compensates for the dark current error later in the section).

**HP 5082-4204 PHOTodiode**

- Sensitivity: 350\( \mu \)A @ 1mW, 900nm
- Maximum Linear Output Current: 100\( \mu \)A
- Area: 0.002cm\(^2\) (0.2mm\(^2\))
- Capacitance: 4pF @ 10V reverse bias
This photodiode is linear with illumination up to approximately 50 to 100µA of output current. The dynamic range is limited by the total circuit noise and the diode dark current (assuming no dark current compensation).

Using the simple circuit shown in Figure 2.60, assume that we wish to have a full scale output of 10V for a diode current of 100µA. This determines the value of the feedback resistor R2 to be 10V/100µA = 100kΩ.

**Analysis of Frequency Response and Stability**

The photodiode preamp model is the classical second-order system shown in Figure 2.62, where the I/V converter has a total input capacitance C1 (the sum of the diode capacitance and the op amp input capacitance). The shunt resistance of the photodiode is neglected since it is much greater than R2, the feedback resistor.

**COMPENSATING FOR INPUT CAPACITANCE IN A CURRENT-TO-VOLTAGE CONVERTER USING VFB OP AMP**

The net input capacitance, C1, forms a pole at a frequency fp in the noise gain transfer function as shown in the Bode plot.
\[
fp = \frac{1}{2\pi R2C1}.
\]

Note that we are neglecting the effects of the compensation capacitor \(C2\) and are assuming that it is small relative to \(C1\) and will not significantly affect the pole frequency \(fp\) when it is added to the circuit. In most cases, this approximation yields results which are close enough, considering the other variables in the circuit.

If left uncompensated, the phase shift at the frequency of intersection, \(fx\), will cause instability and oscillation. Introducing a zero at \(fx\) by adding the feedback capacitor \(C2\) stabilizes the circuit and yields a phase margin of about 45 degrees.

\[
fx = \frac{1}{2\pi R2C2}
\]

Since \(fx\) is the geometric mean of \(fp\) and the unity-gain bandwidth frequency of the op amp, \(fu\),

\[
fx = \sqrt{fp \cdot fu}.
\]

These equations can be solved for \(C2\):

\[
C2 = \sqrt[2]{\frac{C1}{2\pi R2 \cdot fu}}.
\]

This value of \(C2\) will yield a phase margin of about 45 degrees. Increasing the capacitor by a factor of 2 increases the phase margin to about 65 degrees (see References 4 and 5).

In practice, the optimum value of \(C2\) should be optimized experimentally by varying it slightly to optimize the output pulse response.

**Selection of the Op Amp**

The photodiode preamp should be a wideband FET-input one in order to minimize the effects of input bias current and allow low values of photocurrents to be detected. In addition, if the equation for the 3dB bandwidth, \(fx\), is rearranged in terms of \(fu\), \(R2\), and \(C1\), then

\[
fx = \sqrt{\frac{fu}{2\pi R2C1}},
\]

where \(C1 = CD + Cin\)

By inspection of this equation, it is clear that in order to maximize \(fx\), the FET-input op amp should have both a high unity gain-bandwidth product, \(fu\), and a low input capacitance, \(Cin\). In fact, the ratio of \(fu\) to \(Cin\) is a good figure-of-merit when evaluating different op amps for this application. Figure 2.63 compares a number of FET-input op amps suitable for photodiode preamps.
FET-INPUT OP AMP COMPARISON TABLE
FOR WIDE BANDWIDTH PHOTODIODE PREAMPS

<table>
<thead>
<tr>
<th>Product</th>
<th>Unity GBW Product, $f_u$ (MHz)</th>
<th>Input Capacitance $C_{in}$ (pF)</th>
<th>$f_u/C_{in}$ (MHz/pF)</th>
<th>Input Bias Current $I_b$ (pA)</th>
<th>Voltage Noise @10kHz (nV/$\sqrt{Hz}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD823</td>
<td>16</td>
<td>1.8</td>
<td>8.9</td>
<td>3</td>
<td>16</td>
</tr>
<tr>
<td>AD843</td>
<td>34</td>
<td>6</td>
<td>5.7</td>
<td>600</td>
<td>19</td>
</tr>
<tr>
<td>AD744</td>
<td>13</td>
<td>5.5</td>
<td>2.4</td>
<td>100</td>
<td>16</td>
</tr>
<tr>
<td>AD845</td>
<td>16</td>
<td>8</td>
<td>2</td>
<td>500</td>
<td>18</td>
</tr>
<tr>
<td>AD745*</td>
<td>20</td>
<td>20</td>
<td>1</td>
<td>250</td>
<td>2.9</td>
</tr>
<tr>
<td>AD645</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>8</td>
</tr>
<tr>
<td>AD820</td>
<td>1.9</td>
<td>2.8</td>
<td>0.7</td>
<td>2</td>
<td>13</td>
</tr>
<tr>
<td>AD743</td>
<td>4.5</td>
<td>20</td>
<td>0.2</td>
<td>250</td>
<td>2.9</td>
</tr>
</tbody>
</table>

* Stable for Noise Gains $\geq 5$, Usually the Case, Since High Frequency Noise Gain $= 1 + C_1/C_2$, and $C_1$ Usually $\geq 4C_2$.

By inspection, the AD823 op amp has the highest ratio of unity gain-bandwidth product to input capacitance, in addition to relatively low input bias current. For these reasons, it was chosen for the wideband photodiode preamp design.

Using the diode capacitance, $C_D=4\mu F$, and the AD823 input capacitance, $C_{in}=1.8\mu F$, the value of $C_1 = C_D+C_{in} = 5.8\mu F$. Solving the above equations using $C_1=5.8\mu F$, $R_2=100k\Omega$, and $f_u=16MHz$, we find that:

$$f_p = 274kHz$$
$$C_2 = 0.76\mu F$$
$$f_x = 2.1MHz.$$  

In the final design (Figure 2.64), note that the 100k$\Omega$ resistor is replaced with three 33.2k$\Omega$ film resistors to minimize stray capacitance. The feedback capacitor, $C_2$, is a variable 1.5$\mu F$ ceramic and is adjusted in the final circuit for best bandwidth/pulse response. The overall circuit bandwidth is approximately 2MHz.

The full scale output voltage of the preamp for 100$\mu A$ diode current is 10V, and the error (RTO) due to the photodiode dark current of 600pA is 60mV. The dark current...
Photodiode Preamp Noise Analysis

As in most noise analyses, only the key contributors need be identified. Because the noise sources combine in an RSS manner, any single noise source that is at least three or four times as large as any of the others will dominate.

In the case of the wideband photodiode preamp, the dominant sources of output noise are the input voltage noise of the op amp, $V_{n_i}$, and the resistor noise due to $R_2$, $V_{nR_2}$. The input current noise of the FET-input op amp is negligible. The shot noise of the photodiode (caused by the reverse bias) is negligible because of the filtering effect of the shunt capacitance $C_1$. The resistor noise is easily calculated by knowing that a 1kΩ resistor generates about $4nV/\sqrt{Hz}$, therefore, a 100kΩ resistor generates $40nV/\sqrt{Hz}$. The bandwidth for integration is the signal bandwidth, 2.1MHz, yielding a total output rms noise of:

$$V_{nR_2(OUT)} = 40\sqrt{1.57 \cdot 21 \cdot 10^6} = 73\mu\text{Vrms}.$$ 

The factor of 1.57 converts the approximate single-pole bandwidth of 2.1MHz into the equivalent noise bandwidth.

The output noise due to the input voltage noise is obtained by multiplying the noise gain by the voltage noise and integrating the entire function over frequency. This would be tedious if done rigorously, but a few reasonable approximations can be made which greatly simplify the math. Obviously, the low frequency 1/f noise can be
neglected in the case of the wideband circuit. The primary source of output noise is
due to the high-frequency noise-gain peaking which occurs between \( f_p \) and \( f_u \). If we
simply assume that the output noise is constant over the entire range of frequencies
and use the maximum value for AC noise gain \([1 + (C1/C2)]\), then

\[
V_{\text{ni(OUT)}} = V_{\text{ni}} \left(1 + \frac{C1}{C2}\right) \sqrt{1.57f_x} = 250\mu\text{Vrms}.
\]

The total rms noise referred to the output is then the RSS value of the two
components:

\[
V_n(\text{TOTAL}) = \sqrt{(73)^2 + (250)^2} = 260\mu\text{Vrms}.
\]

The total output dynamic range can be calculated by dividing the full scale output
signal (10V) by the total output rms noise, 260\(\mu\text{Vrms}\), and converting to dB, yielding
approximately 92dB.

**EQUIVALENT CIRCUIT FOR OUTPUT NOISE ANALYSIS**

\[V_{\text{ni}} = 16nV/\sqrt{\text{Hz}}\]

\[V_{\text{nR2(out)}} = \sqrt{4kT R2 \cdot 1.57f_x} = 73\mu\text{V rms} \]

\[V_{n(\text{TOTAL})} = \sqrt{250^2 + 73^2} = 260\mu\text{V rms} \]

\[\text{DYNAMIC RANGE} = 20 \log \left(\frac{10V}{260\mu\text{V}}\right) = 92\text{dB}\]

\[\text{ANALOG DEVICES} \quad 2.65\]
REFERENCES


DYNAMIC RANGE COMPRESSION

In many cases, a wide dynamic range is an essential aspect of a signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music and in communications systems. However, it is often necessary to compress the signal to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation, and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is "undone" by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using "compandors", and many schemes have been devised to achieve this function.

There is a class of linear dynamic range compression systems where the gain of the amplifiers in the signal processing chain is independent of the instantaneous amplitude of the signal, but is controlled by a closed loop system in such a way as to render the output (that is the peak, or rms value) essentially constant. The harmonic distortion is relatively low. These systems use what are often called variable-gain amplifiers. While correct, this lacks precision, because nonlinear amplifiers (such as log amps) also exhibit variable gain, but in direct response to the signal magnitude. The term voltage controlled amplifier (VCA) is preferred in this context; it clearly describes the way in which the gain control is implemented, while allowing latitude in regard to the actual circuit means used to achieve the function. The gain may be controlled by a current within the circuit, but usually a voltage. Analog multipliers may be used as VCAs, but there are other topologies which will be discussed later in this section.

Logarithmic amps find applications where signals having wide dynamic ranges (perhaps greater than 100dB) must be processed by elements, such as ADCs, which may have limited dynamic ranges. Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This permits the amplifier to accept signals with a wide input dynamic range and compress them substantially.

Log amps provide nonlinear dynamic range compression and are used in applications where low harmonic distortion is not a requirement. All types of log amps produce a low dynamic range output without the need to first acquire some measure of the signal amplitude for use in controlling gain.
We will first examine linear compression techniques using voltage-controlled amplifiers within automatic-gain-control (AGC) loops. Nonlinear signal compression using log amps is then discussed.

Both AGC loops using VCAs and log amps make excellent building blocks for highly integrated RF/IF subsystems for signal processing in communications systems as will be demonstrated.

**RF / IF SUBSYSTEM BUILDING BLOCKS**

- Signal Dynamic Range Compression Techniques
  - Linear: Automatic Gain Control Loop (AGC) using Voltage Controlled Amplifier (VCA) and Detector
  - Non-Linear: Demodulating / Limiting Logarithmic Amplifiers

- Modulation / Demodulation: In-Phase and Quadrature (I/Q) and Polar (Amplitude and Phase)
  - Dynamic Range Compression Required
  - IF Subsystems: AGC, Log / Limiting, RSSI, Mixers

**AUTOMATIC GAIN CONTROL (AGC) AND VOLTAGE-CONTROLLED AMPLIFIERS (VCAs)**

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1MHz carrier modulated at 1kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0dBm or –120dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since transient noise peaks can now activate the AGC detection circuits. Nonlinear filtering and the concept of “delayed AGC” can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 3.2 shows a basic system.
It is interesting to note that an AGC loop actually has two outputs. The obvious output is the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA, which is in reality, a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal, sometimes referred to as a received signal strength indicator (RSSI).

**Voltage Controlled Amplifiers (VCAs)**

An analog multiplier can be used as a variable-gain amplifier as shown in Figure 3.3. The control voltage is applied to one input, and the signal to the other. In this configuration, the gain is directly proportional to the control voltage.
Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, and they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, and AD603 achieve these demanding and conflicting objectives with a unique and elegant solution - the X-AMP™ (for *exponential amplifier*). The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator equipped with special means to alter its attenuation under the control of a voltage (see Figure 3.4). The amplifier is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30 to 40dB) and minimize distortion. Since this amplifier's gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts. Therefore, it is always operating within its small signal response range.
The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02dB. This provides the basis for the precise linear-in-dB behavior. The overall attenuation is 42.14dB. As will be shown, the amplifier’s input can be connected to any one of these taps, or even interpolated between them, with only a small deviation error of about ±0.2dB. The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14dB less. For example, in the AD600, the fixed gain is 41.07dB (a voltage gain of 113); using this choice, the full gain range is –1.07dB to +41.07dB. The gain is related to the control voltage by the relationship $G_{dB} = 32V_G + 20$ where $V_G$ is in volts. For the AD602, the fixed gain is 31.07dB (a voltage gain of 35.8), and the gain is given by $G_{dB} = 32V_G + 10$.

The gain at $V_G = 0$ is laser trimmed to an absolute accuracy of ±0.2dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 3.5 shows the gain versus the differential control voltage for both the AD600 and the AD602.
In order to understand the operation of the X-AMP, consider the simplified diagram shown in Figure 3.6. Notice that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance ($g_m$) stages; the other input of all these $g_m$ stages is connected to the amplifier’s gain-determining feedback network, $R_{F1}/R_{F2}$. When the emitter bias current, $I_E$, is directed to one of the 8 transistor pairs (by means not shown here), it becomes the input stage for the complete amplifier.

**CONTINUOUS INTERPOLATION BETWEEN TAPS IN THE X-AMP IS PERFORMED WITH CURRENT-CONTROLLED $g_m$ STAGES**
When $I_E$ is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If $I_E$ were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one $g_m$ stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When $I_E$ is equally divided between two $g_m$ stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first expect, but rather by $2\log 1.5$, or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of ±0.25dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of $I_E$ always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple (see Reference 12). As $I_E$ moves further to the right, the overall gain progressively drops.

The total input-referred noise of the X-AMP™ is 1.4nV/√Hz; only slightly more than the thermal noise of a 100Ω resistor which is 1.29nV/√Hz at 25°C. The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain. For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore 1.4nV/√Hz×113, or 158nV/√Hz. Referred to its maximum output of 2V rms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB. Key features of the AD600/AD602 are summarized in Figure 3.7

### KEY FEATURES OF THE AD600/AD602 X-AMPS

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Input-Referred Noise (1.4nV/√Hz)
- Constant Bandwidth (dc to 35MHz)
- Low Distortion: –60dBc THD at ±1V Output
- Stable Group Delay (±2ns Over Gain Range)
- Response Time: Less than 1μs for 40dB Gain Change
- Low Power (125mW per channel maximum)
- Differential Control Inputs
The AD603 X-AMP is a single version of the AD600/AD602 which provides 90MHz bandwidth. There are two pin-programmable gain ranges: –11dB to +31dB with 90MHz bandwidth, and +9dB to +51dB with 9MHz bandwidth. Key specifications for the AD603 are summarized in Figure 3.8.

**KEY FEATURES OF THE AD603 X-AMP**

- Precise "Linear in dB" Gain Control
- Pin Programmable Gain Ranges:
  - –11dB to +31dB with 90MHz Bandwidth
  - +9dB to +51dB with 9MHz Bandwidth
- Bandwidth Independent of Variable Gain
- Low Input-Reflected Noise (1.3nV/√Hz)
- ±0.5dB Typical Gain Accuracy
- Low Distortion: –60dBc, 1V rms Output @ 10MHz
- Low Power (125mW)
- 8-pin Plastic SOIC or Ceramic DIP

**AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM**

RMS/DC converters provide a means to measure the rms value of an arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3dB bandwidth of 900kHz for an input of 100mV rms, but only a 100kHz bandwidth for an input of 10mV rms. Its "raw" logarithmic output is unbuffered, uncalibrated, and not stable over temperature, requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an RMS/DC converter (i.e., AD636) merely as the detector element in an AGC loop, in which the difference between the rms output of the AD636 and a fixed DC reference is nulled in a loop integrator. The
dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS/DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has a precise exponential ("linear-dB") gain-control law, its control voltage is forced by the AGC loop to have the general form

\[ V_{\text{LOG}} = V_S \log_{10} \frac{V_{\text{IN}}(\text{RMS})}{V_Z} \]

where \( V_S \) is the logarithmic slope and \( V_Z \) is the logarithmic intercept, that is, the value of \( V_{\text{IN}} \) for which \( V_{\text{LOG}} \) is zero.

Figure 3.9 shows a practical wide-dynamic-range rms measurement system using the AD600. It can handle inputs from 100µV to 1V rms (4 decades) with a constant measurement bandwidth of 20Hz to 2MHz, limited primarily by the AD636 RMS/DC converter. Its logarithmic output is a buffered voltage, accurately-calibrated to 100mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be –4V for an input of 100µV rms input, zero for 10mV, and +4V for a 1V rms input. In terms of the above equation, \( V_S \) is 2V and \( V_Z \) is 10mV.

**A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM**

Note that the peak "log-output" of ±4V requires the use of ±6V supplies for the dual op-amp U3 (AD712), although lower supplies would suffice for the AD600 and AD636. If only ±5V supplies are available, it will either be necessary to use a reduced value for \( V_S \) (say, 1V, in which case the peak output would be only ±2V), or to restrict the dynamic range of the signal to about 60dB.
The two amplifiers of the AD600 are used in cascade. The modest bandwidth of the unity-gain buffer U3A acts as a low pass filter, thus eliminating the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12Hz. An input attenuator of 10dB (× 0.316) is now provided by R1 + R2 operating in conjunction with the AD600’s input resistance of 100Ω. The adjustment provides an exact calibration of V_Z in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215Ω if very close calibration is not needed, since the input resistance of the AD600 (and all the other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as ±4V to be accepted, that is, signals with an rms value of 1V combined with a crest-factor of up to 4.

The output of A2 is AC-coupled via another 12Hz high-pass filter formed by C2 and the 6.7kΩ input resistance of the AD636. The averaging time-constant for the RMS/DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316mV set by the positive supply voltage of +6V and resistors R6 and R7. (V_Z is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However, V_S is independent of the supply voltages, being determined by the band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3ms formed by the parallel sum of R6/R7 and C3.

If the gain of the AD600 is too high, V_OUT will be greater than the "set-point" of 316mV, causing the output of U3B – that is, V_LOG – to ramp up (note that the integrator is non-inverting). A fraction of V_LOG is connected to the inverting gain-control inputs of the AD600, causing the gain to be reduced, as required, until V_OUT is equal to 316mV (DC), at which time the AC voltage at the output of A2 is forced to exactly 316mV (rms). This fraction is set by R4 and R5 such that a 15.625mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at V_LOG. Since A2 is forced to operate well below its limiting level, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10mV rms is applied to the input, resulting in a voltage of 3.16mV rms at the input to A1 (due to the 10dB attenuator). If the system performs as claimed, V_LOG (and hence V_G) should be zero. This being the case, the gain of both A1 and A2 will be 20dB and the output of the AD600 will be 100 times (40dB) greater than its input, 316mV rms. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits, (which often have a high gain/temperature coefficient due to the internal "kT/q" scaling), the voltages and thus the output of this measurement system are very stable over temperature. This behavior arises directly from the exact exponential calibration of the ladder attenuator.

Typical results are shown for a sinewave input at 100kHz. Figure 3.10 shows that the output is held very close to the set-point of 316mV rms over an input range in excess of 80dB.
Figure 3.11 shows the "decibel" output voltage, \( V_{\text{LOG}} \), and Figure 3.12 shows that the deviation from the ideal output logarithmic output is within ±1 dB for the 80dB range from 80µV to 800mV.
By suitable choice of the input attenuator, R1+R2, this could be centered to cover any range from 25µV to 250mV to, say, 1mV to 10V, with appropriate correction to the value of $V_Z$. (Note that $V_S$ is not affected by the changes in the range). The gain ripple of $\pm0.2$dB seen in this curve is the result of the finite interpolation error of the X-AMP. It occurs with a periodicity of 12dB – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 3.13: the voltages at C1HI and C2HI are "split" by $\pm46.875$mV, or $\pm1.5$dB. Alternatively, either one of these pins can be individually offset by 3dB, and a 1.5dB gain adjustment made at the input attenuator (R1+R2).

The error curve shown in Figure 3.14 demonstrates that over the central portion of the range, the output voltage can be maintained very close to the ideal value. The penalty for this modification is higher errors at both ends of the range.
Figure 3.15 shows the ease with which the AD603 (90MHz X-AMP) can be used as a high speed AGC amplifier. The circuit uses few parts, has a linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio (see the data sheet for the AD600/AD602, or AD603 for a complete description of the methods for cascading X-AMPS), and external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.
The circuit operates from a single +10V supply. Resistors R1, R2 and R3, R4 bias the common pins of A1 and A2 at 5V. This pin is a low impedance point and must have a low impedance path to ground, provided by the 100µF tantalum capacitor and the 0.1µF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. The offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05V (42.14dB x 25mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact but is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42dB; thus the maximum gain of the circuit is twice that, or 84dB. The gain-control range can be shifted up by as much as 20dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100Ω of resistance at the input of A1 form a time-constant of 10µs. C2 blocks the small DC offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16kHz, eliminating low frequency noise.

A half-wave detector is used based on Q1 and R8. The current into capacitor CAV is the difference between the collector current of Q2 (biased to be 300µA at 27°C, 300K) and the collector current of Q1, which increases with the amplitude of the output signal. The automatic gain control voltage, VAGC, is the time-integral of this error current. In order for VAGC (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must,
on average, exactly balance the current in Q2. If the output of A2 is too small to do this, \( V_{\text{AGC}} \) will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where \( R_8 \) is zero and the output voltage \( V_{\text{OUT}} \) is a square wave at, say 455kHz, that is, well above the corner frequency of the control loop.

During the time \( V_{\text{OUT}} \) is negative with respect to the base voltage of Q1, Q1 conducts; when \( V_{\text{OUT}} \) is positive, it is cut off. Since the average collector current of Q1 is forced to be 300\( \mu \)A, and the square wave has a duty cycle of 1:1, Q1’s collector current when conducting must be 600\( \mu \)A. With \( R_8 \) omitted, the peak amplitude of \( V_{\text{OUT}} \) is forced to be just the \( V_{\text{BE}} \) of Q1 at 600\( \mu \)A, typically about 700mV, or 2\( V_{\text{BE}} \) peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7mV/°C. Although this may not be troublesome in some applications, the correct value of \( R_8 \) will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, \( V_{\text{OUT}} \) is now the sum of \( V_{\text{BE}} \) and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of \( V_{\text{BE}} \). This is actually nothing more than an application of the "bandgap voltage reference" principle. When \( R_8 \) is chosen such that the sum of the voltage across it and the \( V_{\text{BE}} \) of Q1 is close to the bandgap voltage of about 1.2V, \( V_{\text{OUT}} \) will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600\( \mu \)A during each half-cycle of the square wave, a resistor of 833\( \Omega \) would add a PTAT voltage of 500mV at 300K, increasing by 1.66mV/°C. In practice, the optimum value will depend on the type of transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N3906 pair and sine wave signals, the recommended value is 806\( \Omega \).

This resistor also serves to lower the peak current in Q1 when more typical signals (usually sinusoidal) are involved, and the 1.8kHz lowpass filter it forms with \( C_A \) helps to minimize distortion due to ripple in \( V_{\text{AGC}} \). Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current for an ideal rectifier would be 0.637 times as large, causing the output amplitude to be 1.2V/0.637=1.88V, or 1.33V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4Vrms, or 3.6V p-p.

The bandwidth of the circuit exceeds 40MHz. At 10.7MHz, the AGC threshold is 100\( \mu \)V (–67dBm) and its maximum gain is 83dB, 20log(1.4V/100\( \mu \)V). The circuit holds its output at 1.4V rms for inputs as low as –67dBm to +15dBm (82dB), where the input signal exceeds the AD603’s maximum input rating. For a +10dBm input at 10.7MHz, the second harmonic is 34dB down from the fundamental, and the third harmonic is 35dB down.
The term "Logarithmic Amplifier" (generally abbreviated to "log amp") is something of a misnomer, and "Logarithmic Converter" would be a better description. The conversion of a signal to its equivalent logarithmic value involves a nonlinear operation, the consequences of which can be confusing if not fully understood. It is important to realize that many of the familiar concepts of linear circuits are irrelevant to log amps. For example, the incremental gain of an ideal log amp approaches infinity as the input approaches zero, and a change of offset at the output of a log amp is equivalent to a change of amplitude at its input - not a change of input offset.

For the purposes of simplicity in our initial discussions, we shall assume that both the input and the output of a log amp are voltages, although there is no particular reason why logarithmic current, transimpedance, or transconductance amplifiers should not also be designed.

If we consider the equation $y = \log(x)$ we find that every time $x$ is multiplied by a constant $A$, $y$ increases by another constant $A_1$. Thus if $\log(K) = K_1$, then $\log(AK) = K_1 + A_1$, $\log(A^2K) = K_1 + 2A_1$, and $\log(K/A) = K_1 - A_1$. This gives a graph as shown in Figure 3.16, where $y$ is zero when $x$ is unity, $y$ approaches minus infinity as $x$ approaches zero, and which has no values for $x$ for which $y$ is negative.

![Graph of $y = \log(x)$](image)

On the whole, log amps do not behave in this way. Apart from the difficulties of arranging infinite negative output voltages, such a device would not, in fact, be very useful. A log amp must satisfy a transfer function of the form

$$V_{out} = V_y \log(V_{in}/V_x)$$

over some range of input values which may vary from 100:1 (40dB) to over 1,000,000:1 (120dB).
With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear $V_{in}/V_{out}$ law. This behavior is often lost in device noise. Noise often limits the dynamic range of a log amp. The constant, $V_y$, has the dimensions of voltage, because the output is a voltage. The input, $V_{in}$, is divided by a voltage, $V_{x}$, because the argument of a logarithm must be a simple dimensionless ratio.

A graph of the transfer characteristic of a log amp is shown in Figure 3.17. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When $V_{in} = V_{x}$, the logarithm is zero (log 1 = 0). $V_{x}$ is therefore known as the intercept voltage of the log amp because the graph crosses the horizontal axis at this value of $V_{in}$.

The slope of the line is proportional to $V_y$. When setting scales, logarithms to the base 10 are most often used because this simplifies the relationship to decibel values: when $V_{in} = 10V_{x}$, the logarithm has the value of 1, so the output voltage is $V_y$. When $V_{in} = 100V_{x}$, the output is $2V_y$, and so forth. $V_y$ can therefore be viewed either as the "slope voltage" or as the "volts per decade factor."

The logarithm function is indeterminate for negative values of $x$. Log amps can respond to negative inputs in three different ways: (1) They can give a fullscale negative output as shown in Figure 3.18. (2) They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 3.19. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a detecting log amp. (3) They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 3.20. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a logarithmic video (log video) amplifier or, sometimes, a true log amp (although this type of log amp is rarely used in video-display-related applications).
BASIC LOG AMP
(SATURATES WITH NEGATIVE INPUT)

DETECTING LOG AMP
(OUTPUT POLARITY INDEPENDENT OF INPUT POLARITY)
There are three basic architectures which may be used to produce log amps: the *basic diode log amp*, the *successive detection log amp*, and the "true log amp" which is based on cascaded semi-limiting amplifiers.

The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current as shown in Figure 3.21. In practice, the dynamic range of this configuration is limited to 40-60dB because of non-ideal diode characteristic, but if the diode is replaced with a diode-connected transistor as shown in Figure 3.22, the dynamic range can be extended to 120dB or more. This type of log amp has three disadvantages: (1) both the slope and intercept are temperature dependent; (2) it will only handle unipolar signals; and (3) its bandwidth is both limited and dependent on signal amplitude.

Where several such log amps are used on a single chip to produce an analog computer which performs both log and antilog operations, the temperature variation in the log operations is unimportant, since it is compensated by a similar variation in the antilogging. This makes possible the AD538, a monolithic analog computer which can multiply, divide, and raise to powers. Where actual logging is required, however, the AD538 and similar circuits require temperature compensation (Reference 7). The major disadvantage of this type of log amp for high frequency applications, though, is its limited frequency response - which cannot be overcome. However carefully the amplifier is designed, there will always be a residual feedback capacitance $C_C$ (often known as Miller capacitance), from output to input which limits the high frequency response.

What makes this Miller capacitance particularly troublesome is that the impedance of the emitter-base junction is inversely proportional to the current flowing in it - so that if the log amp has a dynamic range of 1,000,000:1, then its bandwidth will also vary by 1,000,000:1. In practice, the variation is less because other considerations
limit the large signal bandwidth, but it is very difficult to make a log amp of this type with a small-signal bandwidth greater than a few hundred kHz.

THE DIODE / OP-AMP LOG AMP

\[ V = \frac{kT}{q} \ln \left( \frac{I}{I_0} \right) \quad \text{if } I \gg I_0 \]

\[ E_O = \frac{kT}{q} \ln \left( \frac{I_{IN}}{I_0} \right) \approx 0.06 \log \frac{V_{IN}}{R_{IN} I_0} \quad \text{if } I_{IN} \gg I_0 \]

For high frequency applications, therefore, detecting and true log architectures are used. Although these differ in detail, the general principle behind their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behavior.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage (Figure 3.23). If each amplifier has a gain of A dB,
the small signal gain of the strip is $NA\,\text{dB}$. If the input signal is small enough for the last stage not to limit, the output of the summing amplifier will be dominated by the output of the last stage.

**BASIC MULTI-STAGE LOG AMP ARCHITECTURE**

As the input signal increases, the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to $(N-1)A\,\text{dB}$. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to $(N-2)A\,\text{dB}$, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.

The response curve is thus a set of straight lines as shown in Figure 3.24. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases, is an even better one, because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.
The choice of gain, \( A \), will also affect the log linearity. If the gain is too high, the log approximation will be poor. If it is too low, too many stages will be required to achieve the desired dynamic range. Generally, gains of 10 to 12dB (3x to 4x) are chosen.

This is, of course, an ideal and very general model - it demonstrates the principle, but its practical implementation at very high frequencies is difficult. Assume that there is a delay in each limiting amplifier of \( t \) nanoseconds (this delay may also change when the amplifier limits but let’s consider first order effects!). The signal which passes through all \( N \) stages will undergo delay of \( Nt \) nanoseconds, while the signal which only passes one stage will be delayed only \( t \) nanoseconds. This means that a small signal is delayed by \( Nt \) nanoseconds, while a large one is “smeared”, and arrives spread over \( Nt \) nanoseconds. A nanosecond equals a foot at the speed of light, so such an effect represents a spread in position of \( Nt \) feet in the resolution of a radar system-which may be unacceptable in some systems (for most log amp applications this is not a problem).

A solution is to insert delays in the signal paths to the summing amplifier, but this can become complex. Another solution is to alter the architecture slightly so that instead of limiting gain stages, we have stages with small signal gain of \( A \) and large signal (incremental) gain of unity (0dB). We can model such stages as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier as shown in Figure 3.25.
Figure 3.25 shows that such stages, cascaded, form a log amp without the necessity of summing from individual stages. Both the multi-stage architectures described above are video log amplifiers, or true log amplifiers, but the most common type of high frequency log amplifier is the successive detection log amp architecture shown in Figure 3.26.

**SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER WITH LOG AND LIMITER OUTPUTS**

The successive detection log amp consists of cascaded limiting stages as described above, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed as shown in Figure 3.26. If the
detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together.

Log amps using this architecture have two outputs: the log output and a limiting output. In many applications, the limiting output is not used, but in some (FM receivers with "S"-meters, for example), both are necessary. The limited output is especially useful in extracting the phase information from the input signal in polar demodulation techniques.

The log output of a successive detection log amplifier generally contains amplitude information, and the phase and frequency information is lost. This is not necessarily the case, however, if a half-wave detector is used, and attention is paid to equalizing the delays from the successive detectors - but the design of such log amps is demanding.

The specifications of log amps will include noise, dynamic range, frequency response (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the slope of the transfer characteristic (which is expressed as V/db or mA/dB depending on whether we are considering a voltage- or current-output device), the intercept point (the input level at which the output voltage or current is zero), and the log linearity. (See Figures 3.27 and 3.28)

**KEY PARAMETERS OF LOG AMPS**

- **NOISE**: The Noise Referred to the Input (RTI) of the Log Amp. It May Be Expressed as a Noise Figure or as a Noise Spectral Density (Voltage, Current, or Both) or as a Noise Voltage, a Noise Current, or Both

- **DYNAMIC RANGE**: Range of Signal Over Which the Amplifier Behaves in a Logarithmic Manner (Expressed in dB)

- **FREQUENCY RESPONSE**: Range of Frequencies Over Which the Log Amp Functions Correctly

- **SLOPE**: Gradient of Transfer Characteristic in V/db or mA/db

- **INTERCEPT POINT**: Value of Input Signal at Which Output is Zero

- **LOG LINEARITY**: Deviation of Transfer Characteristic (Plotted on log/lin Axes) from a Straight Line (Expressed in dB)
In the past, it has been necessary to construct high performance, high frequency successive detection log amps (called log strips) using a number of individual monolithic limiting amplifiers such as the Plessey SL-1521-series (see Reference 16). Recent advances in IC processes, however, have allowed the complete log strip function to be integrated into a single chip, thereby eliminating the need for costly hybrid log strips.

The AD641 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 250MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with proper layout, instability from feedback via supply rails is unlikely. A block diagram of the AD641 is shown in Figure 3.29. Unlike many previous integrated circuit log amps, the AD641 is laser trimmed to high absolute accuracy of both slope and intercept, and is fully temperature compensated. Key features of the AD641 are summarized in Figure 3.30. The transfer function for the AD641 as well as the log linearity is shown in Figure 3.31.
BLOCK DIAGRAM OF THE AD641 MONOLITHIC LOG AMP

AD641 KEY FEATURES

- 44dB Dynamic Range
- Bandwidth dc to 250MHz
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Laser-Trimmed Intercept of 1mV - Temperature Stable
- Less than 2dB Log Non-Linearity
- Limiter Output: ±1.6dB Gain Flatness, ±2° Phase Variation for -44dBm to 0dBm inputs @ 10.7MHz
- Balanced Circuitry for Stability
- Minimal External Component Requirement
Because of its high accuracy, the actual waveform driving the AD641 must be considered when calculating responses. When a waveform passes through a log function generator, the mean value of the resultant waveform changes. This does not affect the slope of the response, but the apparent intercept is modified according to Figure 3.32.

# THE EFFECT OF WAVEFORM ON INTERCEPT POINT

<table>
<thead>
<tr>
<th>INPUT WAVEFORM</th>
<th>PEAK OR RMS</th>
<th>INTERCEPT FACTOR</th>
<th>ERROR (RELATIVE TO A DC INPUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square Wave</td>
<td>Either</td>
<td>1</td>
<td>0.00dB</td>
</tr>
<tr>
<td>Sine Wave</td>
<td>Peak</td>
<td>2</td>
<td>-6.02dB</td>
</tr>
<tr>
<td>Sine Wave</td>
<td>RMS</td>
<td>1.414 (√2)</td>
<td>-3.01dB</td>
</tr>
<tr>
<td>Triwave</td>
<td>Peak</td>
<td>2.718 (e)</td>
<td>-8.68dB</td>
</tr>
<tr>
<td>Triwave</td>
<td>RMS</td>
<td>1.569 (e/√3)</td>
<td>-3.91dB</td>
</tr>
<tr>
<td>Gaussian Noise</td>
<td>RMS</td>
<td>1.887</td>
<td>-5.52dB</td>
</tr>
</tbody>
</table>

The AD641 is calibrated and laser trimmed to give its defined response to a DC level or a symmetrical 2kHz square wave. It is also specified to have an intercept of 2mV for a sinewave input (that is to say a 2kHz sinewave of amplitude 2mV peak [not
peak-to-peak] gives the same mean output signal as a DC or square wave signal of 1mV).

The waveform also affects the ripple or nonlinearity of the log response. This ripple is greatest for DC or square wave inputs because every value of the input voltage maps to a single location on the transfer function, and thus traces out the full nonlinearities of the log response. By contrast, a general time-varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. As is clear in Figure 3.33, this smoothing effect is greatest for a triwave.

**THE EFFECT OF WAVEFORM ON AD641 LOG LINEARITY**

![Graph showing the effect of different waveforms on log linearity](image)

Each of the five stages in the AD641 has a gain of 10dB and a full-wave detected output. The transfer function for the device was shown in Figure 3.21 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to RF applications, the AD641 is dc-coupled throughout. This allows it to be used in LF and VLF systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

The limiter output of the AD641 has better than 1.6dB gain flatness (-44dBm to 0dBm @ 10.7MHz) and less than 2° phase variation, allowing it to be used as a polar demodulator.

The AD606 is a complete monolithic 50MHz bandwidth log amp using 9 stages of successive detection, and is shown in Figure 3.34. Key specifications are summarized in Figure 3.35. Seven of the amplifier/detector stages handle inputs from -80dBm (32µV rms) up to about -14dBm (45mV rms). The noise floor is about -83dBm (18µV rms). Another two parallel stages receive the input attenuated by 22.3dB, and respond to inputs up to +10dBm (707mV rms). The gain of each stage is 11.15dB and is accurately stabilized over temperature by a precise biasing system.
The AD606 provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation lowpass filter and provides an output voltage of +0.1V DC to +4V DC. The logarithmic scaling is such that the output is +0.5V for a sinusoidal input of –75dBm, and +3.5V at an input of +5dBm. Over this range, the log linearity is typically within ±0.4dB.

AD606 LOG AMP KEY FEATURES

- Dynamic Range: –75dBm to +5dBm (80dB)
- Input Noise: < 1.5nV/√Hz
- Usable from 200Hz to Greater than 50MHz
- Slope: 37.5mV/dB Voltage Output
- On-Chip Lowpass Output Filter
- Limiter Output: ±1.6dB Gain Flatness, ±2° Phase Variation for -44dBm to 0dBm inputs @ 10.7MHz
- +5V Single-Supply, 65mW Power Consumption
The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90dB of conversion range. A second lowpass filter automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD606’s limiter output provides a hard-limited signal output as a differential current of ±1.2mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200Ω resistors to provide a voltage gain of more than 90dB from the input. This limiting amplifier has exceptionally low amplitude-to-phase conversion. The limiter output has ±1dB output flatness and ±3° phase stability over an 80dB range at 10.7MHz.
**RECEIVER OVERVIEW**

*Walt Kester, Bob Clarke*

We will now consider how the previously discussed building blocks can be used in designing a receiver. First, consider the analog superheterodyne receiver invented in 1917 by Major Edwin H. Armstrong (see Figure 3.36). This architecture represented a significant improvement over single-stage direct conversion (homodyne) receivers which had previously been constructed using tuned RF amplifiers, a single detector, and an audio gain stage. A significant advantage of the superheterodyne receiver is that it is much easier and more economical to have the gain and selectivity of a receiver at fixed intermediate frequencies (IF) than to have the gain and frequency-selective circuits “tune” over a band of frequencies.

**DUAL CONVERSION SUPERHET RECEIVER**

**(EXAMPLE FREQUENCIES)**

The receiver shown is a dual conversion receiver with two intermediate frequency (IF) stages. The frequencies chosen are typical in digital mobile radio (DMR), but the principles apply to other systems as well. The 900MHz RF signal is mixed down to the first IF frequency of 240MHz. Tuning is accomplished by the first local oscillator (LO1). The LO1 frequency is chosen such that the output of the first mixer is at the first IF frequency, 240MHz. Choosing a relatively high first IF frequency eases the requirement on the image frequency rejection filter as will be discussed in the next section on mixers. The first IF is then mixed down to the second IF frequency of 10.7MHz, where it is demodulated (either using analog or digital techniques).

Because of the wide dynamic range of the RF signal, such a receiver requires the use of automatic gain control, voltage controlled amplifiers, and in some cases (depending on the type of demodulation), logarithmic amplifiers.
Receiver design is a complicated art, and there are many tradeoffs that can be made between IF frequencies, single-conversion vs. double-conversion or triple conversion, filter cost and complexity at each stage in the receiver, demodulation schemes, etc. There are many excellent references on the subject, and the purpose of this section is only to acquaint the design engineer with some of the building block ICs which can make receiver design much easier.

Before we look at further details of a receiver, the subject of mixing requires further discussion.
MULTIPLIERS, MODULATORS, AND MIXERS
Barrie Gilbert, Bob Clarke

An idealized mixer is shown in Figure 3.37. An RF (or IF) mixer (not to be confused with video and audio mixers) is an active or passive device that converts a signal from one frequency to another. It can either modulate or demodulate a signal. It has three signal connections, which are called ports in the language of radio engineers. These three ports are the radio frequency (RF) input, the local oscillator (LO) input, and the intermediate frequency (IF) output.

THE MIXING PROCESS

![Diagram of an ideal mixer](image)

A mixer takes an RF input signal at a frequency $f_{RF}$, mixes it with a LO signal at a frequency $f_{LO}$, and produces an IF output signal that consists of the sum and difference frequencies, $f_{RF} \pm f_{LO}$. The user provides a bandpass filter that follows the mixer and selects the sum ($f_{RF} + f_{LO}$) or difference ($f_{RF} - f_{LO}$) frequency.

Some points to note about mixers and their terminology:

- When the sum frequency is used as the IF, the mixer called an upconverter; when the difference is used, the mixer is called a downconverter. The former is often used in a transmit channel, the latter in a receive channel.

- In a receiver, when the LO frequency is below the RF, it is called low-side injection and the mixer a low-side downconverter; when the LO is above the RF, it is called high-side injection, and the mixer a high-side downconverter.

- Each of the outputs is only half the amplitude (one-quarter the power) of the individual inputs; thus, there is a loss of 6dB in this ideal linear mixer. (In a
practical multiplier, the conversion loss may be greater than 6dB, depending on the scaling parameters of the device. Here, we assume a mathematical multiplier, having no dimensional attributes.

A mixer can be implemented in several ways, using active or passive techniques. A brief review of the various classes of nonlinear elements that can be used for frequency translation may be helpful in setting the context. We can identify three subclasses of circuits, sharing certain similarities. All are in the class of signal multipliers, producing at their output a signal which is, in one way or another, the product of its two inputs. They are multipliers, modulators, and mixers.

An analog multiplier generally has two signal input ports, which can be called X and Y, and generates an output W that is the linear product of the voltages applied to these two ports. To retain dimensional consistency, the analog linear multiplication function must invoke the use of a reference voltage, which we can call U, thus W=XY/U. In some cases, U is actually a third input that can be used to implement analog division.

There are three functional categories of multipliers: In single-quadrant multipliers, X and Y must be unipolar; in two-quadrant multipliers, one of the inputs may be bipolar; in four-quadrant multipliers, both X and Y may be bipolar. Analog Devices produces a wide range of "linear" multipliers, including the AD534, AD538, AD539, AD633, AD734, AD834 and AD835, providing the highest available accuracy (±0.02% for the AD734) to the highest speed (more than 500MHz for the AD834).

Modulators (sometimes called balanced-modulators, doubly-balanced modulators or even on occasions high level mixers) can be viewed as sign-changers. The two inputs, X and Y, generate an output W, which is simply one of these inputs (say, Y) multiplied by just the sign of the other (say, X), that is W = Ysign(X). Therefore, no reference voltage is required. A good modulator exhibits very high linearity in its signal path, with precisely equal gain for positive and negative values of Y, and precisely equal gain for positive and negative values of X. Ideally, the amplitude of the X input needed to fully switch the output sign is very small, that is, the X-input exhibits a comparator-like behavior. In some cases, where this input may be a logic signal, a simpler X-channel can be used. A highly-linear mixer such as the AD831 is well-suited as a modulator.

A mixer is a modulator optimized for frequency-translation. Its place in the signal path is usually close to the antenna, where both the wanted and (often large) unwanted signals coexist at its signal input, usually called the RF port. Thus, the mixer must exhibit excellent linearity in the sense that its output (at the IF port) is expected to increase by the same number of dB as a test signal applied to the RF port, up to as high as level as possible. This attribute is defined both by the 1dB gain-compression and the 3rd-order intercept (later explained). The conversion process is driven by an input applied to the LO port.

Noise and matching characteristics are crucial to achieving acceptable levels of performance in a receiver's mixer. It is desirable to keep the LO power to a minimum to minimize cross-talk between the three ports, but this often conflicts with other requirements. The gain from the RF port to its IF port at specified RF and LO frequencies is called the conversion gain and in classical diode-bridge mixers is less than –4dB. Active mixers provide higher conversion gain, and better port-port
isolation, but often at the expense of noise and linearity. It is not usually possibly (nor even desirable) to describe mixer behavior using equations relating the instantaneous values of inputs and outputs; instead, we generally seek to characterize mixers in terms of their non-ideal cross-product terms at the output. In this class, Analog Devices has the AD831, and mixers are found embedded in the AD607, AD608 and other signal-processing ICs.

Thus far, we have seen that multipliers are linear in their response to the instantaneous value of both of their input voltages; modulators are linear in their response to one input, the other merely flipping the sign of this signal at regular intervals, with virtually zero transition time, and beyond that having ideally no other effect on the signal; mixers are a sort of RF half-breed, ideally being very linear on the RF input, and ‘binary’ in their switching function in response to the LO input, but in reality being nonideal in both respects; they are optimized for very low noise and minimal intermodulation distortion.

Mixing Using an Ideal Analog Multiplier

Figure 3.38 shows a greatly simplified RF mixer by assuming the use of an analog multiplier.

Ideally, the multiplier has no noise, no limit to the maximum signal amplitude, and no intermodulation between the various RF signals (that is, no spurious nonlinearities). Figure 3.39 shows the result of mixing (= multiplying) an RF input of $\sin(\omega_{RF}t)$ with (= by) a LO input of $\sin(\omega_{LO}t)$, where $\omega_{RF} = 2\pi \times 11\text{MHz}$ and $\omega_{LO} = 2\pi \times 10\text{MHz}$.

Clearly, to better understand mixer behavior, we will need to consider not only the time-domain waveforms, as shown here, but also the spectrum of the IF output. Figure 3.40 shows the output spectrum corresponding to the above IF waveform.
"MIXING" USING AN ANALOG MULTIPLIER

ANALOG MULTIPLIER, e.g., AD834

INPUTS AND OUTPUTS FOR MULTIPLYING MIXER
FOR $f_{RF} = 11\text{MHz}$, $f_{LO} = 10\text{MHz}$

Horizontal: 200ns/div.
There is no mystery so far. The mathematics are simple. Neglecting scaling issues (real signals are voltages; thus a practical multiplier needs an embedded voltage reference, ignored here) the relationship is:

\[
\sin(\omega_{RF}t) \sin(\omega_{LO}t) = \frac{1}{2} \left\{ \cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t \right\} \quad \text{Eq. 1}
\]

The multiplier has thus transformed the RF input into two, equal-amplitude cosinusoidal components at its output (the IF port), one at the sum frequency, \(\omega_{RF} + \omega_{LO}\), and the other at the difference frequency, \(\omega_{RF} - \omega_{LO}\).

In practice, an analog multiplier would be a poor choice for a mixer because the two linear inputs bring with them a serious noise penalty.

**Image Response**

A receiver using even this mathematically perfect mixer suffers a basic problem, that of *image response*. Consider the use of a low-side downconverter. The wanted output is found at the frequency \(\omega_{IF} = \omega_{RF} - \omega_{LO}\). So we might suppose that the only component of the RF spectrum that finds its way through the mixer “sieve” to the narrow IF passband is the wanted component at \(\omega_{RF}\). But we could have just as easily written (1) as

\[
\sin(\omega_{RF}t) \sin(\omega_{LO}t) = \frac{1}{2} \left\{ \cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{LO} - \omega_{RF})t \right\} \quad \text{Eq. 1a}
\]

because the cosine function is symmetric about \(t = 0\). So there is another spectral component at the RF input that falls in the IF passband, namely the one for which \(\omega_{IF} = \omega_{LO} - \omega_{RF}\), in this case, the image frequency.
Consider the above example, where $f_{LO} = 10\text{MHz}$ and $f_{IF} = 1\text{MHz}$; the wanted response is at the IF frequency, $f_{IF} = 1\text{MHz}$ for $f_{RF} = 11\text{MHz}$. However, the mixer produces the same IF in response to the *image frequency*, $f_{IMAGE} = 9\text{MHz}$ (see Figure 3.41).

![Image Response Diagram]

The most practical solution to this dilemma is to carefully choose the IF frequency to minimize the likelihood of image sensitivity and also include an image-reject filter at the RF input, just ahead of the mixer. Another approach is to use a special type of mixer circuit that does not respond to the image frequency. This approach requires circuitry which is considerably more complex, and for this reason has generally been unpopular, but it is becoming more practical in a modern IC implementation. It has the further disadvantage of higher power consumption, since two mixer cells operating in quadrature are required.

**The Ideal Mixer**

Ideally, to meet the low-noise, high-linearity objectives of a mixer we need some circuit that implements a polarity-switching function in response to the LO input. Thus, the mixer can be reduced to Figure 3.42, which shows the RF signal being split into in-phase ($0^\circ$) and anti-phase ($180^\circ$) components; a changeover switch, driven by the local oscillator (LO) signal, alternately selects the in-phase and antiphase signals. Thus reduced to essentials, the ideal mixer can be modeled as a sign-switcher.
In a perfect embodiment, this mixer would have no noise (the switch would have zero resistance), no limit to the maximum signal amplitude, and would develop no intermodulation between the various RF signals. Although simple in concept, the waveform at the intermediate frequency (IF) output can be very complex for even a small number of signals in the input spectrum. Figure 3.43 shows the result of mixing just a single input at 11MHz with an LO of 10MHz.

The wanted IF at the difference frequency of 1MHz is still visible in this waveform, and the 21MHz sum is also apparent. But the spectrum of this waveform is clearly more complex than that obtained using the analog multiplier. How are we to analyze this?
We still have a product, but now it is that of a sinusoid (the RF input) at $\omega_{RF}$ and a variable that can only have the values +1 or –1, that is, a unit square wave at $\omega_{LO}$. The latter can be expressed as a Fourier series

$$S_{LO} = \frac{4}{\pi} \{ \sin(\omega_{LO}t) - \frac{1}{3} \sin(3\omega_{LO}t) + \frac{1}{5} \sin(5\omega_{LO}t) - \ldots \} \quad \text{Eq. 2}$$

Thus, the output of the switching mixer is its RF input, which we can simplify as $\sin(\omega_{RF}t)$, multiplied by the above expansion for the square wave, producing

$$S_{IF} = \frac{4}{\pi} \{ \sin(\omega_{RF}t) \sin(\omega_{LO}t) - \frac{1}{3} \sin(3\omega_{RF}t) \sin(3\omega_{LO}t) + \frac{1}{5} \sin(5\omega_{RF}t) \sin(5\omega_{LO}t) - \ldots \} \quad \text{Eq. 3}$$

Now expanding each of the products, we obtain

$$S_{IF} = \frac{2}{\pi} \{ \sin(\omega_{RF} + \omega_{LO})t + \sin(\omega_{RF} - \omega_{LO})t$$
$$- \frac{1}{3} \sin(\omega_{RF} + 3\omega_{LO})t - \frac{1}{3} \sin(\omega_{RF} - 3\omega_{LO})t$$
$$+ \frac{1}{5} \sin(\omega_{RF} + 5\omega_{LO})t + \frac{1}{5} \sin(\omega_{RF} - 5\omega_{LO})t - \ldots \} \quad \text{Eq. 4}$$

or simply

$$S_{IF} = \frac{2}{\pi} \{ \sin(\omega_{RF} + \omega_{LO})t + \sin(\omega_{RF} - \omega_{LO})t + \text{harmonics} \} \quad \text{Eq. 5}$$

The most important of these harmonic components are sketched in Figure 3.44 for the particular case used to generate the waveform shown in Figure 3.43, that is, $f_{RF} = 11\text{MHz}$ and $f_{LO} = 10\text{MHz}$. Because of the $2/\pi$ term, a mixer has a minimum $3.92$ dB insertion loss (and noise figure) in the absence of any gain.
Note that the ideal (switching) mixer has exactly the same problem of image response to $\omega_{LO} - \omega_{RF}$ as the linear multiplying mixer. The image response is somewhat subtle, as it does not immediately show up in the output spectrum: it is a latent response, awaiting the occurrence of the "wrong" frequency in the input spectrum.

**Diode-Ring Mixer**

For many years, the most common mixer topology for high-performance applications has been the diode-ring mixer, one form of which is shown in Figure 3.45. The diodes, which may be silicon junction, silicon Schottky-barrier or gallium-arsenide types, provide the essential switching action. We do not need to analyze this circuit in great detail, but note in passing that the LO drive needs to be quite high—often a substantial fraction of one watt—in order to ensure that the diode conduction is strong enough to achieve low noise and to allow large signals to be converted without excessive spurious nonlinearity.

Because of the highly nonlinear nature of the diodes, the impedances at the three ports are poorly controlled, making matching difficult. Furthermore, there is considerable coupling between the three ports; this, and the high power needed at the LO port, make it very likely that there will be some component of the (highly-distorted) LO signal coupled back toward the antenna. Finally, it will be apparent that a passive mixer such as this cannot provide conversion gain; in the idealized scenario, there will be a conversion loss of $2/\pi$ [as Eq. 4 shows], or 3.92dB. A practical mixer will have higher losses, due to the resistances of the diodes and the losses in the transformers.
Users of this type of mixer are accustomed to judging the signal handling capabilities by a “Level” rating. Thus, a Level-17 mixer needs +17dBm (50mW) of LO drive and can handle an RF input as high as +10dBm (±1V). A typical mixer in this class would be the Mini-Circuits LRMS-1H, covering 2-500MHz, having a nominal insertion loss of 6.25dB (8.5dB max), a worst-case LO-RF isolation of 20dB and a worst-case LO-IF isolation of 22dB (these figures for an LO frequency of 250-500MHz). The price of this component is approximately $10.00 in small quantities. Even the most expensive diode-ring mixers have similar drive power requirements, high losses and high coupling from the LO port.

**FET Mixers**

A modern alternative to the diode-ring mixer is one in which the diodes are replaced by FETs. The idea here is to reduce the distortion caused by the inherent nonlinearities of junction diodes, whose incremental resistance varies with the instantaneous signal current. To reduce this effect, the diodes are often driven to very high current levels. Indeed, some users of diode-ring mixers push them to extremes, operating at current levels close to those which will cause the diodes to fail by over-dissipation. Thus, in commenting about a certain minor variation to the diode-ring-mixer, we read:

“This helps the mixer to accept higher LO power without burning out the diodes!”

(From Wes Hayward, *Solid State Design for the Radio Amateur*, ARRL, 1986, Chapter 6, p.120)

To avoid “burning out the diodes”, some mixers use two or four J-FETs in an analogous way to that shown in Figure 3.45. The idea is that the channel resistance
of a large FET driven into its triode region of conduction can be as low as the
dynamic resistance of a diode, thus achieving similar conversion gain and noise
levels. But this low resistance arises without any current flow in the channel and it
is also more linear than that of the diodes when signal current does flow, thus
resulting in lower intermodulation, and hence a larger overall dynamic range. MOS-
FETs can also be used in a similar way.

This style of FET-based mixers is very attractive for many high-performance
applications. However, since the active devices are still used only as switches, they
do not provide power gain, and have typical insertion losses of 6 to 8dB.
Furthermore, the balance of these mixers is still critically dependent on such things
as transistor matching and transformer winding accuracy, large LO drives (volts)
are needed, and the overall matching requirements continue to be difficult to
achieve over the full frequency range. Finally, of course, they are not directly
amenable to monolithic integration.

Another popular circuit, widely used in many inexpensive receivers, is the dual-gate
MOS-FET mixer. In this type of mixer, the RF signal is applied to one gate of the
FET and the LO signal to the second gate. The multiplication process is not very
well-defined, but in general terms relies on the fact that both the first and second
gates influence the current in the channel. The structure can be modeled as two
FETs, where the drain of the lower FET (having the RF input applied to it) is
intimately connected to the source of the upper FET (having the LO input on its
gate). The lower FET operates in its triode region, and thus exhibits a $g_m$ that is a
function of its drain voltage, controlled by the LO. Though not readily modeled to
great accuracy, this mixer, like many others, can be pragmatically optimized to
achieve useful performance, though not without the support of many associated
passive components for biasing and matching.

**Classic Active Mixer**

The diode-ring mixer not only has certain performance limitations, but it is also not
amenable to fabrication using integrated circuit technologies, at least in the form
shown in Figure 3.45. In the mid sixties it was realized that the four diodes could be
replaced by four transistors to perform essentially the same switching function. This
formed the basis of the now-classical bipolar circuit shown in Figure 3.46, which is a
minimal configuration for the fully-balanced version. Millions of such mixers have
been made, including variants in CMOS and GaAs. We will limit our discussion to
the BJT form, an example of which is the Motorola MC1496, which, although quite
rudimentary in structure, has been a mainstay in semi-discrete receiver designs for
about 25 years.
The **active mixer** is attractive for the following reasons:

- It can be monolithically integrated with other signal processing circuitry.
- It can provide conversion gain, whereas a diode-ring mixer always has an insertion loss. (Note: Active mixers may have gain. The analog Devices' AD831 active mixer, for example, amplifies the result in Eq. 5 by $\pi/2$ to provide unity gain from RF to IF.)
- It requires much less power to drive the LO port.
- It provides excellent isolation between the signal ports.
- Is far less sensitive to load-matching, requiring neither diplexer nor broadband termination.

Using appropriate design techniques it can provide trade-offs between third-order intercept (3OI or IP3) and the 1dB gain-compression point ($P_{1dB}$), on the one hand, and total power consumption ($P_D$) on the other. (That is, including the LO power, which in a passive mixer is "hidden" in the drive circuitry.)

**Basic Operation of the Active Mixer**

Unlike the diode-ring mixer, which performs the polarity-reversing switching function in the voltage domain, the active mixer performs the switching function in the current domain. Thus the active mixer core (transistors Q3 through Q6 in Figure 3.46) must be driven by current-mode signals. The voltage-to-current converter formed by Q1 and Q2 receives the voltage-mode RF signal at their base terminals and transforms it into a differential pair of currents at the their collectors.
A second point of difference between the active mixer and diode ring mixer, therefore, is that the active mixer responds only to magnitude of the input voltage, not to the input power; that is, the active mixer is not matched to the source. (The concept of matching is that both the current and the voltage at some port are used by the circuitry which forms that port). By altering the bias current, $I_{bb}$, the transconductance of the input pair Q1-Q2 can be set over a wide range. Using this capability, an active mixer can provide variable gain.

A third point of difference is that the output (at the collectors of Q3–Q6) is in the form of a current, and can be converted back to a voltage at some other impedance level to that used at the input, hence, can provide further gain. By combining both output currents (typically, using a transformer) this voltage gain can be doubled. Finally, it will be apparent that the isolation between the various ports, in particular, from the LO port to the RF port, is inherently much lower than can be achieved in the diode ring mixer, due to the reversed-biased junctions that exist between the ports.

Briefly stated, though, the operation is as follows. In the absence of any voltage difference between the bases of Q1 and Q2, the collector currents of these two transistors are essentially equal. Thus, a voltage applied to the LO input results in no change of output current. Should a small DC offset voltage be present at the RF input (due typically to mismatch in the emitter areas of Q1 and Q2), this will only result in a small feedthrough of the LO signal to the IF output, which will be blocked by the first IF filter.

Conversely, if an RF signal is applied to the RF port, but no voltage difference is applied to the LO input, the output currents will again be balanced. A small offset voltage (due now to emitter mismatches in Q3–Q6) may cause some RF signal feedthrough to the IF output; as before, this will be rejected by the IF filters. It is only when a signal is applied to both the RF and LO ports that a signal appears at the output; hence, the term doubly-balanced mixer.

Active mixers can realize their gain in one other way: the matching networks used to transform a 50Ω source to the (usually) high input impedance of the mixer provides an impedance transformation and thus voltage gain due to the impedance step up. Thus, an active mixer that has loss when the input is terminated in a broadband 50Ω termination can have “gain” when an input matching network is used.

The AD831, 500MHz, Low Distortion Active Mixer

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in digital mobile radio base stations, direct-to-baseband conversion, quadrature modulation and demodulation, and doppler-frequency shift detection in ultrasound imaging applications. The mixer includes a local oscillator driver and a low-noise output amplifier. The AD831 provides a +24dBm third-order intercept point for −10dBm local oscillator power, thus improving system performance and reducing system cost, compared to passive mixers, by eliminating the need for a high power local oscillator driver and its associated shielding and isolation problems.
simplified block diagram of the AD831 is shown in Figure 3.47, and key specifications in Figure 3.48.

**AD831 500MHz LOW DISTORTION ACTIVE MIXER**

![Block Diagram of AD831 Active Mixer]

**AD831 ACTIVE MIXER KEY SPECIFICATIONS**

- Doubly-Balanced Mixer, 10dB Noise Figure
- Low Distortion (IF = 10.7MHz, RF to 200MHz):
  - +24dBm Third Order Intercept
  - +10dBm 1dB Compression Point
- Low LO Drive Required: –10dBm
- Bandwidth:
  - 500MHz RF and LO Input Bandwidths
  - 250MHz Differential Current IF Output
  - DC to > 200MHz Single-Ended Voltage IF Output
Noise Figure

Noise Figure (NF) is a figure of merit used to determine how a device degrades the signal-to-noise ratio of its input. Note: in RF systems, the impedance is 50Ω unless otherwise stated. Mathematically, noise figure is defined as:

\[
NF = 20 \log_{10} \frac{S_I / N_I}{S_O / N_O},
\]

where \( S_I / N_I \) is the input signal-to-noise ratio, and \( S_O / N_O \) is the output signal-to-noise ratio.

Typical noise figures for passive mixers with post amplifiers are 12 to 15dB. The NF of the AD831 is 10dB with a matched input, which is adequate for applications in which there is gain in front of the mixer.

Noise Figure is used in a "cascaded noise figure calculation", which gives the overall noise figure of a receiver. Basically, the noise figure of each stage is converted into a noise factor (\( F = \text{antilog} \ NF/10 \)) and plugged into a spreadsheet containing the Friis Equation:

\[
F_{\text{RECEIVER}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \sum_{K=4}^{N} \frac{F_K - 1}{\prod_{J=1}^{K-1} G_J},
\]

where \( F_N \) and \( G_N \) are the noise factor and gain, respectively, of the Nth stage in the receiver.

For a passive diode-ring mixer, the noise figure is the same as the insertion loss. For an active mixer, however, noise is added to the signal by the active devices in the signal path. The difference between the noise figure of a matched active mixer and an unmatched active mixer can be several dB due to the “voltage gain” of the impedance-matching network, which acts as a “noiseless” preamplifier (Figure 3.49). In the case of the AD831, the noise figure for the matched circuit is 10 dB (at 70MHz) and the unmatched circuit with its input terminated with a 50Ω resistor is 16dB.

The noise figure is 11.7dB at 220 MHz using the external matching network shown in Figure 3.49. The values shown are for 220 MHz and provide 10 dB of voltage gain.
Intermodulation Distortion

Even before the ‘mixing’ process in the core, the entire signal spectrum co-exists within the RF input stage. This part of the mixer is inevitably nonlinear, to a greater or lesser extent, and, with or without the LO input operative, generates a very large number of intermodulation products.

Thus, the key objectives in the design of a high-performance active mixer are to achieve a very linear RF input section, followed by a near-ideal polarity-switching stage, followed by a very linear IF output amplifier (if used) prior to the first filter.

1dB Compression Point and Third-Order Intercept Point

For a single-sinusoid input to a system, a point will be reached as the input amplitude is increased at which the apparent gain becomes 1dB lower than that observed at lower input amplitudes. This is called the 1dB gain compression level, which we’ll abbreviate \( P_{1dB} \), and is usually quoted in dBm, or ‘decibels above 1mW, that is, it is expressed as a power measurement. When using an active mixer with an input matching network, the gain of the input matching network must be taken into account when defining the system in terms of an active mixer’s 1dB compression point, since the impedance transformation of the network increases the input voltage to mixer.

Another metric used in characterizing mixers is the third-order intercept, known as \( P_{3OI} \) or IP3. If two tones of frequency \( f_1 \) and \( f_2 \) (representing two adjacent channels in a communications system, for example) are applied to a non-linear system, there will be a large number of intermodulation products generated. The third-order
distortion products which fall at $2f_2-f_1$ and $2f_1-f_2$ are particularly troublesome, because they are close to the original frequencies (see Figure 3.50). If the two tones represent true signals, then the third-order IMD products can interfere with signals in the adjacent channels.

THIRD-ORDER INTERMODULATION DISTORTION

Rather than measuring the third-order distortion products for a variety of signal amplitudes, the concept of third-order intercept can be used to extract the IMD information and is often used as a figure of merit for mixers and amplifiers in RF applications.

A plot (Figure 3.51) of the power levels at the output of the system for the fundamental of the output frequency and for its third harmonic, plotted versus the input power, will generally yield a pair of straight lines which eventually intersect (at the 3rd order intercept point, IP3).
The problem with this metric is that it has meaning only for certain simple cases. In particular, the 3rd harmonic is assumed to increase at three times the rate of the fundamental. The appeal of $P_{3OI}$ lies in the fact that it is easily measured, or at least, it is easy to obtain measurements. (The measurements are not hard to make, but it will be found that the apparent $P_{3OI}$ is signal-dependent). Apply a low level signal, at some known level $P_O$ (in dBm, see Figure 3.51), measure the output power at the fundamental, $P_1$ (in relative terms, dBc) and at the third harmonic, $P_3$ (also in dBc) and from simple geometry calculate

$$P_{3OI} = P_O + \frac{1}{2} (P_1 - P_3) \quad \text{Eq. 6}$$

The non-linearity in some classical circuits, such as the diode-ring mixer, approximates a cubic function, and the above relationship holds, but in practice, the $P_{3OI}$ can be quite misleading, for several reasons. First, other circuits may not, in general, exhibit this type of non-linearity. This type of behavior could easily lead to apparent third-order intercept values which were impressively high (theoretically infinite, if 'measured' using signals of less than the critical amplitude).

A spur chart is a compilation of the $nf_1 \pm mf_2$ products that result from the mixing process. The spur chart is useful because it allows an engineer developing a frequency plan for a radio to identify possible problems due to spurious signals created in the mixer. However, the spur chart is also tedious to create; for $n = m = 7$, a chart requires 112 measurements.

The compilation of results is the spur chart (also called a "mixer table"). Details of making the spur chart measurements and results are given in the AD831 data sheet (see Reference 17).
Mixer Summary

Mixers are a special kind of analog multiplier optimized for use in frequency translation, having one linear input (that associated with the RF signal) and a second (that associated with the LO input) which alternates the phase of the first input by 0/180°. In integrating complete receivers in monolithic form, certain basic circuit forms have proven useful. So far, we have considered a classic form, a six-transistor circuit exemplified by the AD831. Compared to a diode-ring mixer, this circuit has several advantages, including much better isolation between ports, the ability to provide conversion gain (which may also be variable), the need for much lower LO drive levels, and the elimination of special matching networks.

Often cited as a disadvantage of the active mixer is its poorer dynamic range: we have just begun to examine what defines this, beginning with a consideration of the linearity of the RF port, traditionally characterized by the 1dB gain-compression input power, $P_{1\text{dB}}$, and the third-order intercept, $P_{3\text{OI}}$. The second of these measures was shown to be meaningful only if the nonlinearity is essentially cubic in form, which may not always be true. In passing, we pointed out that while inputs and outputs are invariably characterized in terms of a power level of so-many-dBm, active mixers respond to instantaneous signal voltages at their inputs, which are usually not matched to their source, which can be confusing at times.

Now that we have examined each of the fundamental receiver building blocks, we are ready to look at receiver subsystems.
In order to design a communications receiver, a clear understanding of the modulation technique is essential. There are many types of modulation, ranging from simple amplitude modulation (AM), phase modulation (PM), and frequency modulation (FM) to multi-level quadrature-amplitude-modulation (QAM) where both amplitude and phase are modulated. Most modern modulation schemes make use of both signal amplitude and phase information. A complex signal can thus be represented in two ways as shown in the diagrams in Figure 3.52. The left-hand diagram represents the signal in rectangular coordinates as an inphase (I) and quadrature (Q) signal of the form:

\[ S(t) = I(t) + jQ(t). \]

The right hand diagram represents the same signal expressed in polar coordinates:

\[ S(t) = A(t)e^{j\phi(t)}. \]

The conversions between the two coordinate systems are:

\[ S(t) = A(t)e^{j\phi(t)} = I(t) + jQ(t), \]

where

\[ A(t) = \sqrt{I(t)^2 + Q(t)^2}, \]

\[ \phi(t) = \arctan \left( \frac{Q(t)}{I(t)} \right). \]
Note that the signals are identical, only their representation is different.

In the case of the I/Q (rectangular) representation, a linear IF strip is required. Variable gain is required because of the wide dynamic range, and amplitude and phase information must be preserved. This type of IF strip often incorporates an I/Q demodulator whose outputs drive baseband ADCs followed by a DSP. Linear IF amplifiers are used in these systems.

For the case of the polar representation, the signal amplitude is derived from the RSSI (log) output of a log/limiting amplifier and the phase information from the limited output. This type of IF strip operates at a high fixed gain, retains the phase information in the limited output, and often incorporates a phase demodulator.

In order to handle these two fundamental representations of modulation, ADI has developed two IF subsystems, the AD607 and the AD608. These are used in such applications as PHS, PCN, DECT, CT2, and GSM where the modulation mode is some form of phase-shift keying (PSK).

The choice of demodulation technique depends on the receiver architecture. The standard architecture in GSM and PHS uses a rectangular representation of the signal, that is $S(t) = I(t) + jQ(t)$ and requires a linear IF amplifier stage such as that in the AD607. In this architecture, a baseband converter consisting of two signal inputs; each with individual low-pass filters, digitizes the $I(t)$ and $Q(t)$ outputs of the IF IC’s quadrature demodulator. Further demodulation is performed digitally using a DSP. An equalizer in the DSP then determines the correct manual gain control (MGC) voltage (or digital signal) to change the IF gain to center the signal in the dynamic range of the baseband ADCs. The equalizer calculates the RSSI value as part of this process (see Figure 3.53).
A detailed block diagram of the AD607 Mixer/AGC/RSSI 3V receiver IF subsystem is shown in Figure 3.54. The RF input frequency can be as high as 500MHz, and the IF frequency from 400kHz to 12MHz. It consists of a mixer, linear IF amplifiers, I and Q demodulators, a phase-locked quadrature oscillator, AGC detector, and a biasing system with external power-down. Total power on +3V is 25mW.

**AD607 FUNCTIONAL BLOCK DIAGRAM**
The AD607’s low noise, high intercept mixer is a doubly-balanced Gilbert cell type. It has a nominal –15dBm input-referred 1dB compression point and a –8dBm input-referred third-order intercept. The mixer section also includes a local oscillator preamplifier, which lowers the required external LO drive to –16dBm.

The variable-gain mixer and the linear four-stage IF amplifier strip together provide a voltage controlled gain range of more than 90dB. The I and Q demodulators, each consisting of a multiplier followed by a 2-pole, 2MHz low-pass filter, are driven by a phase-locked loop providing inphase and quadrature clocks. An internal AGC detector is included, and the temperature stable gain control system provides an accurate RSSI capability.

The I and Q demodulators provide inphase and quadrature baseband outputs to interface with Analog Devices’ AD7013 (IS54/IS136, TETRA, MSAT) and AD7015 (GSM) baseband converters.

Key specifications for the AD607 are summarized in Figure 3.55.

**AD607 MIXER / AGC / RSSI 3V RECEIVER KEY FEATURES**

- **Mixer:**
  - –15dBm Input 1dB Compression Point
  - –8dBm Input Third Order Intercept Point
  - RF/LO Inputs to 500MHz
  - 12dB Noise Figure, Matched Input
  - –16dBm LO Drive

- **Linear IF Amplifier:**
  - 45MHz Bandwidth
  - Linear-in-dB Gain Control Over 90dB Gain Range
  - –15dBm Input 1dB Compression Point
  - +18dBm Output Third Order Intercept Point

- **In-Phase and Quadrature Demodulators:**
  - 1.5MHz Output Bandwidth
  - Compatible with Baseband Converters (AD7013, AD7015)

- 25mW Total Power @ Single +3V Supply

For cases where the signal is represented in polar form, the AD608 is the proper choice. The AD608 Mixer/Limiter/RSSI 3V Receiver IF Subsystem consists of a mixer followed by a logarithmic amplifier; the logarithmic amplifier has both limited output (phase information) and an RSSI output (amplitude information). This architecture is useful in polar demodulation applications as shown in Figure 3.56. A block diagram of the AD608 is shown in Figure 3.57, and key specifications in Figure 3.58.
RECEIVER BASED ON AD608 SUBSYSTEM USING POLAR DEMODULATION

AD608 FUNCTIONAL BLOCK DIAGRAM

AD608 MIXER / LIMITER / RSSI 3V RECEIVER KEY FEATURES

Mixer:
- -15dBm Input 1dB Compression Point
The log amp both measures the level of the signal (like the AD641 and AD606) and limits the signal. The RSSI or Received Signal Strength Indicator output is proportional to the log of the input signal. As a limiting amplifier, the AD608 removes any amplitude changes in the signal and keeps only the phase or frequency changes. These phase or frequency changes are proportional to the modulating signal and contain the intelligence in the signal. The AD608’s limiting amplifier is a 5-stage log amp with more than 80dB of dynamic range.

In a typical mobile phone application, the RF signal (typically 900MHz or 1800MHz) is mixed down to the first IF (typically 240MHz), is filtered, and enters the AD608, where it is mixed down to a second IF at 10.7MHz, where it is amplified, limited, and measured. The limited output is demodulated by an external frequency or phase demodulator. The RSSI output is digitized by an ADC and used for active power control in the phone system.

As a practical note, the cutoff frequency of the log amp’s internal low pass filter depends on what range of frequencies the log amp was designed for. In analog cellular systems, where the modulation mode is narrow-band FM, the IF is typically 450kHz. The low pass filters in the IF ICs designed for these standards have a fairly low cutoff frequency, and the filter’s voltage output response provides a "slow" RSSI. In GSM (Global System for Mobile Communications) and PHS (Personal Handy System) applications, the IF is typically 10.7MHz or higher, and the filter’s voltage output response provides a "fast" RSSI. The cutoff frequency of the low pass filter in the AD608 is 2MHz.
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SECTION 4
HIGH SPEED SAMPLING AND
HIGH SPEED ADCs, Walt Kester

INTRODUCTION

High speed ADCs are used in a wide variety of real-time DSP signal-processing applications, replacing systems that used analog techniques alone. The major reason for using digital signal processing are (1) the cost of DSP processors has gone down, (2) their speed and computational power has increased, and (3) they are reprogrammable, thereby allowing for system performance upgrades without hardware changes. DSP offers solutions that cannot be achieved in the analog domain, i.e. V.32 and V.34 modems.

However, in order for digital signal processing techniques to be effective in solving an analog signal processing problem, appropriate cost effective high speed ADCs must be available. The ADCs must be tested and specified in such a way that the design engineer can relate the ADC performance to specific system requirements, which can be more demanding than if they were used in purely analog signal processing systems. In most high speed signal processing applications, AC performance and wide dynamic range are much more important than traditional DC performance. This requires that the ADC manufacturer not only design the right ADCs but specify them as completely as possible to cover a wide variety of applications.

Another important aspect of integrating ADCs into a high speed system is a complete understanding of the sampling process and the distortion mechanisms which ultimately limit system performance. High speed sampling ADCs first were used in instrumentation and signal processing applications, where much emphasis was placed on time-domain performance. While this is still important, applications of ADCs in communications also require comprehensive frequency-domain specifications.

Modern IC processes also allow the integration of more analog functionality into the ADC, such as on-board references, sample-and-hold amplifiers, PGAs, etc. This makes them easier to use in a system by minimizing the amount of support circuitry required.

Another driving force in high speed ADC development is the trend toward lower power and lower supply voltages. Most high speed sampling ADCs today operate on either dual or single 5V supplies, and there is increasing interest in single-supply converters which will operate on 3V or less for battery powered applications. Lower supply voltages tend to increase a circuit’s sensitivity to power supply noise and ground noise, especially mixed-signal devices such as ADCs and DACs.

The trend toward lower cost and lower power has led to the development of a variety of high speed ADCs fabricated on standard 0.6 micron CMOS processes. Making a precision ADC on a digital process (no thin film resistors are available) is a real challenge to the IC circuit designer. ADCs which require the maximum in
performance still require a high speed complementary bipolar process (such as Analog Devices' XFCB) with thin film resistors.

The purpose of this section is to equip the engineer with the proper tools necessary to understand and select ADCs for high speed systems applications. Making intelligent tradeoffs in the system design requires a thorough understanding of the fundamental capabilities and limitations of state-of-the-art high speed sampling ADCs.

HIGH SPEED SAMPLING ADCs

- Wide Acceptance in Signal Processing and Communications
- Emphasis on Dynamic Performance
- Trend to Low Power, Low Voltage, Single-Supply
- More On-Chip Functionality: PGAs, SHA, Digital Filters, etc.
- Process Technology:
  - Low Cost CMOS: Up to 12-bits @ 10MSPS
  - High Speed Complementary Bipolar: Up to 12-bits @ 70MSPS
  - Statistical Matching Techniques Rather than Thin Film Laser Trimming

FUNDAMENTALS OF HIGH SPEED SAMPLING

The sampling process can be discussed from either the frequency or time domain or both. Frequency-domain analysis is applicable to communications, so that's what we will consider.

First consider the case of a single frequency sinewave of frequency \( f_a \) sampled at a frequency \( f_s \) by an ideal impulse sampler (see top diagram in Figure 4.2). Also assume that \( f_s > 2f_a \) as shown. The frequency-domain output of the sampler shows aliases or images of the original signal around every multiple of \( f_s \), i.e. at frequencies equal to
\[
| \pm Kf_s \pm f_a | , \ K = 1, 2, 3, 4, ..... \]
The Nyquist bandwidth is defined to be the frequency spectrum from DC to $f_s/2$. The frequency spectrum is divided into an infinite number of Nyquist zones, each having a width equal to $0.5f_s$ as shown. In practice, the ideal sampler is replaced by an ADC followed by an FFT processor. The FFT processor only provides an output from DC to $f_s/2$, i.e., the signals or aliases which appear in the first Nyquist zone.

Now consider the case of a signal which is outside the first Nyquist zone (Figure 4.2, bottom diagram) Notice that even though the signal is outside the first Nyquist zone, its image (or alias), $f_s-f_a$, falls inside. Returning to Figure 4.2, top diagram, it is clear that if an unwanted signal appears at any of the image frequencies of $f_a$, it will also occur at $f_a$, thereby producing a spurious frequency component in the first Nyquist zone. This is similar to the analog mixing process and implies that some filtering ahead of the sampler (or ADC) is required to remove frequency components which are outside the Nyquist bandwidth, but whose aliased components fall inside it. The filter performance will depend on how close the out-of-band signal is to $f_s/2$ and the amount of attenuation required.

**BASEBAND ANTIALLIASING FILTERS**

Baseband sampling implies that the signal to be sampled lies in the first Nyquist zone. It is important to note that with no input filtering at the input of the ideal sampler, any frequency component (either signal or noise) that falls outside the Nyquist bandwidth in any Nyquist zone will be aliased back into the first Nyquist zone. For this reason, an antialiasing filter is used in almost all sampling ADC applications to remove these unwanted signals.
Properly specifying the antialiasing filter is important. The first step is to know the characteristics of the signal being sampled. Assume that the highest frequency of interest is $f_a$. The antialiasing filter passes signals from DC to $f_a$ while attenuating signals above $f_a$.

Assume that the corner frequency of the filter is chosen to be equal to $f_a$. The effect of the finite transition from minimum to maximum attenuation on system dynamic range is illustrated in Figure 4.3.

![Effects of Antialiasing Filter on System Dynamic Range](image)

Assume that the input signal has fullscale components well above the maximum frequency of interest, $f_a$. The diagram shows how fullscale frequency components above $f_s - f_a$ are aliased back into the bandwidth DC to $f_a$. These aliased components are indistinguishable from actual signals and therefore limit the dynamic range to the value on the diagram which is shown as $DR$.

Some texts recommend specifying the antialiasing filter with respect to the Nyquist frequency, $f_s/2$, but this assumes that the signal bandwidth of interest extends from DC to $f_s/2$ which is rarely the case. In the example shown in Figure 4.3, the aliased components between $f_a$ and $f_s/2$ are not of interest and do not limit the dynamic range.

The antialiasing filter transition band is therefore determined by the corner frequency $f_a$, the stopband frequency $f_s - f_a$, and the stopband attenuation, $DR$. The required system dynamic range is chosen based on our requirement for signal fidelity.
Filters have to become more complex as the transition band becomes sharper, all other things being equal. For instance, a Butterworth filter gives 6dB attenuation per octave for each filter pole. Achieving 60dB attenuation in a transition region between 1MHz and 2MHz (1 octave) requires a minimum of 10 poles, not a trivial filter, and definitely a design challenge.

Therefore, other filter types are generally more suited to high speed applications where the requirement is for a sharp transition band and in-band flatness coupled with linear phase response. Elliptic filters meet these criteria and are a popular choice.

There are a number of companies which specialize in supplying custom analog filters. TTE is an example of such a company (Reference 1). As an example, the normalized response of the TTE, Inc., LE1182 11-pole elliptic antialiasing filter is shown in Figure 4.4. Notice that this filter is specified to achieve at least 80dB attenuation between $f_c$ and $1.2f_c$. The corresponding passband ripple, return loss, delay, and phase response are also shown in Figure 4.4. This custom filter is available in corner frequencies up to 100MHz and in a choice of PC board, BNC, or SMA with compatible packages.

**CHARACTERISTICS OF TTE, INC., LE1182-SERIES 11-POLE ELLIPTICAL FILTER**

From this discussion, we can see how the sharpness of the antialiasing transition band can be traded off against the ADC sampling frequency. Choosing a higher sampling rate (oversampling) reduces the requirement on transition band sharpness (hence, the filter complexity) at the expense of using a faster ADC and processing data at a faster rate. This is illustrated in Figure 4.5 which shows the effects of
increasing the sampling frequency while maintaining the same analog corner frequency, \( f_a \), and the same dynamic range, \( DR \), requirement.

**INCREASING SAMPLING FREQUENCY RELAXES REQUIREMENT ON ANTIALIASING FILTER**

![Diagram showing the effect of increasing sampling frequency on antialiasing filter requirements.](image)

LOWPASS FILTER SPECIFICATIONS:

The above design process is started by choosing an initial sampling rate of 2 to 4 times \( f_a \). Determine the filter specifications based on the required dynamic range and see if such a filter is realizable within the constraints of the system cost and performance. If not, consider a higher sampling rate which may require using a faster ADC.

The antialiasing filter requirements can be relaxed somewhat if it is certain that there will never be a fullscale signal at the stopband frequency \( f_s - f_a \). In many applications, it is improbable that fullscale signals will occur at this frequency. If the maximum signal at the frequency \( f_s - f_a \) will never exceed \( X \) dB below fullscale. Then, the filter stopband attenuation requirement is reduced by that same amount. The new requirement for stopband attenuation at \( f_s - f_a \) based on this knowledge of the signal is now only \( DR - X \) dB. When making this type of assumption, be careful to treat any noise signals which may occur above the maximum signal frequency \( f_a \) as unwanted signals which will also alias back into the signal bandwidth.

**UNDERSAMPLING (HARMONIC SAMPLING, BANDPASS SAMPLING, IF SAMPLING, DIRECT IF TO DIGITAL CONVERSION)**

Thus far we have considered the case of baseband sampling, i.e., all the signals of interest lie within the first Nyquist zone. Figure 4.6A shows such a case, where the band of sampled signals is limited to the first Nyquist zone, and images of the original band of frequencies appear in each of the other Nyquist zones.
Consider the case shown in Figure 4.6B, where the sampled signal band lies entirely within the second Nyquist zone. The process of sampling a signal outside the first Nyquist zone is often referred to as **undersampling** or **harmonic sampling**. Note that the first Nyquist zone image contains all the information in the original signal, with the exception of its original location (the order of the frequency components within the spectrum is reversed, but this is easily corrected by re-ordering the output of the FFT).

![Diagram of undersampling zones](image)

**A**

ZONE 1

0.5fs, fs, 1.5fs, 2fs, 2.5fs, 3fs, 3.5fs

**B**

ZONE 2

0.5fs, fs, 1.5fs, 2fs, 2.5fs, 3fs, 3.5fs

**C**

ZONE 3

0.5fs, fs, 1.5fs, 2fs, 2.5fs, 3fs, 3.5fs

Figure 4.6C shows the sampled signal restricted to the third Nyquist zone. Note that the first Nyquist zone image has no frequency reversal. In fact, the sampled signal frequencies may lie in any unique Nyquist zone, and the first Nyquist zone image is still an accurate representation (with the exception of the frequency reversal which occurs when the signals are located in even Nyquist zones). At this point we can clearly state the Nyquist criteria:

*A signal must be sampled at a rate equal to or greater than twice its **bandwidth** in order to preserve all the signal information.*

Notice that there is no mention of the absolute *location* of the band of sampled signals within the frequency spectrum relative to the sampling frequency. The only constraint is that the band of sampled signals be restricted to a single Nyquist zone, i.e., the signals must not overlap any multiple of $f_s/2$ (this, in fact, is the primary function of the antialiasing filter).

Sampling signals above the first Nyquist zone has become popular in communications because the process is equivalent to analog demodulation. It is becoming common practice to sample IF signals directly and then use digital techniques to process the signal, thereby eliminating the need for the IF.
demodulator. Clearly, however, as the IF frequencies become higher, the dynamic performance requirements on the ADC become more critical. The ADC input bandwidth and distortion performance must be adequate at the IF frequency, rather than only baseband. This presents a problem for most ADCs designed to process signals in the first Nyquist zone, therefore an ADC suitable for undersampling applications must maintain dynamic performance into the higher order Nyquist zones.

**ANTIALIASING FILTERS IN UNDERSAMPLING APPLICATIONS**

Figure 4.7 shows a signal in the second Nyquist zone centered around a carrier frequency, \( f_c \), whose lower and upper frequencies are \( f_1 \) and \( f_2 \). The antialiasing filter is a bandpass filter. The desired dynamic range is \( DR \), which defines the filter stopband attenuation. The upper transition band is \( f_2 \) to \( 2f_s - f_2 \), and the lower is \( f_1 \) to \( f_s - f_1 \). As in the case of baseband sampling, the antialiasing filter requirements can be relaxed by proportionally increasing the sampling frequency, but \( f_c \) must also be increased so that it is always centered in the second Nyquist zone.

**ANTIALIASING FILTER FOR UNDERSAMPLING**

![Diagram of antialiasing filter](image)

**BANDPASS FILTER SPECIFICATIONS:**

- **STOPBAND ATTENUATION** = \( DR \)
- **TRANSITION BAND:** \( f_2 \) to \( 2f_s - f_2 \)
- \( f_1 \) to \( f_s - f_1 \)
- **CORNER FREQUENCIES:** \( f_1, f_2 \)

Two key equations can be used to select the sampling frequency, \( f_s \), given the carrier frequency, \( f_c \), and the bandwidth of its signal, \( \Delta f \). The first is the Nyquist criteria:

\[
f_s > 2\Delta f \quad \text{Eq. 1}
\]

The second equation ensures that \( f_c \) is placed in the center of a Nyquist zone:

\[
f_s = \frac{4f_c}{2NZ - 1}, \quad \text{Eq. 2}
\]
where \( NZ = 1, 2, 3, 4, \ldots \) and \( NZ \) corresponds to the Nyquist zone in which the carrier and its signal fall (see Figure 4.8).

\( NZ \) is normally chosen to be as large as possible while still maintaining \( f_s > 2\Delta f \). This results in the minimum required sampling rate. If \( NZ \) is chosen to be odd, then \( f_c \) and its signal will fall in an odd Nyquist zone, and the image frequencies in the first Nyquist zone will not be reversed. Tradeoffs can be made between the sampling frequency and the complexity of the antialiasing filter by choosing smaller values of \( NZ \) (hence a higher sampling frequency).

**CENTERING AN UNDERSAMPLED SIGNAL WITHIN A NYQUIST ZONE**

As an example, consider a 4MHz wide signal centered around a carrier frequency of 71MHz. The minimum required sampling frequency is therefore 8MSPS. Solving Eq. 2 for \( NZ \) using \( f_c = 71\text{MHz} \) and \( f_s = 8\text{MSPS} \) yields \( NZ = 18.25 \). However, \( NZ \) must be an integer, so we round 18.25 to the next lowest integer, 18. Solving Eq. 2 again for \( f_s \) yields \( f_s = 8.1143\text{MSPS} \), \( f_c = 71\text{MHz} \), and \( NZ = 18 \).

Now assume that we desire more margin for the antialiasing filter, and we select \( f_s \) to be 10MSPS. Solving Eq. 2 for \( NZ \), using \( f_c = 71\text{MHz} \) and \( f_s = 10\text{MSPS} \) yields \( NZ = 14.7 \). We round 14.7 to the next lowest integer, giving \( NZ = 14 \). Solving Eq. 2 again for \( f_s \) yields \( f_s = 10.519\text{MSPS} \). The final values are therefore \( f_s = 10.519\text{MSPS} \), \( f_c = 71\text{MHz} \), and \( NZ = 14 \).

The above iterative process can also be carried out starting with \( f_s \) and adjusting the carrier frequency to yield an integer number for \( NZ \).

**DISTORTION AND NOISE IN AN IDEAL N-BIT ADC**
Thus far we have looked at the implications of the sampling process without considering the effects of ADC quantization. We will now treat the ADC as an ideal sampler, but include the effects of quantization.

The only errors (DC or AC) associated with an ideal N-bit ADC are those related to the sampling and quantization processes. The maximum error an ideal ADC makes digitizing a DC input signal is ±1/2LSB. Any AC signal applied to an ideal N-bit ADC will produce quantization noise whose rms value (measured over the Nyquist bandwidth, DC to \( f_s/2 \)) is approximately equal to the weight of the least significant bit (LSB), \( q \), divided by \( \sqrt{12} \). (See Reference 2). This assumes that the signal is at least a few LSBs in amplitude so that the ADC output always changes state. The quantization error signal from a linear ramp input is approximated as a sawtooth waveform with a peak-to-peak amplitude equal to \( q \), and its rms value is therefore \( q/\sqrt{12} \) (see Figure 4.9).

\[
\text{SNR} = 6.02N + 1.76\text{dB} + 10\log \left( \frac{f_s}{2\cdot \text{BW}} \right) \quad \text{FOR FS SINEWAVE}
\]

It can be shown that the ratio of the rms value of a full scale sinewave to the rms value of the quantization noise (expressed in dB) is:

\[
\text{SNR} = 6.02N + 1.76\text{dB},
\]

where \( N \) is the number of bits in the ideal ADC. This equation is only valid if the noise is measured over the entire Nyquist bandwidth from DC to \( f_s/2 \). If the signal bandwidth, \( \text{BW} \), is less than \( f_s/2 \), then the SNR within the signal bandwidth \( \text{BW} \) is increased because the amount of quantization noise within the signal bandwidth is smaller. The correct expression for this condition is given by:

\[
\text{SNR} = 6.02N + 1.76\text{dB} + 10\log \left( \frac{f_s}{2\cdot \text{BW}} \right).
\]
The above equation reflects the condition called *oversampling*, where the sampling frequency is higher than twice the signal bandwidth. The correction term is often called *processing gain*. Notice that for a given signal bandwidth, doubling the sampling frequency increases the SNR by 3dB.

Although the rms value of the noise is accurately approximated $\frac{q}{\sqrt{12}}$, its frequency domain content may be highly correlated to the AC input signal. For instance, there is greater correlation for low amplitude periodic signals than for large amplitude random signals. Quite often, the assumption is made that the theoretical quantization noise appears as white noise, spread uniformly over the Nyquist bandwidth DC to $f_s/2$. Unfortunately, this is not true. In the case of strong correlation, the quantization noise appears concentrated at the various harmonics of the input signal, just where you don’t want them.

In most applications, the input to the ADC is a band of frequencies (usually summed with some noise), so the quantization noise tends to be random. In spectral analysis applications (or in performing FFTs on ADCs using spectrally pure sinewaves - see Figure 4.10), however, the correlation between the quantization noise and the signal depends upon the ratio of the sampling frequency to the input signal. This is demonstrated in Figure 4.11, where an ideal 12-bit ADCs output is analyzed using a 4096-point FFT. In the left-hand FFT plot, the ratio of the sampling frequency to the input frequency was chosen to be exactly 32, and the worst harmonic is about 76dB below the fundamental. The right hand diagram shows the effects of slightly offsetting the ratio, showing a relatively random noise spectrum, where the SFDR is now about 92dBc. In both cases, the rms value of all the noise components is $\frac{q}{\sqrt{12}}$, but in the first case, the noise is concentrated at harmonics of the fundamental.

**DYNAMIC PERFORMANCE ANALYSIS OF AN IDEAL N-BIT ADC**

![Diagram](analogdevices.png)
EFFECT OF RATIO OF SAMPLING CLOCK TO INPUT FREQUENCY ON SFDR FOR IDEAL 12-BIT ADC

Note that this variation in the apparent harmonic distortion of the ADC is an artifact of the sampling process and the correlation of the quantization error with the input frequency. In a practical ADC application, the quantization error generally appears as random noise because of the random nature of the wideband input signal and the additional fact that there is a usually a small amount of system noise which acts as a dither signal to further randomize the quantization error spectrum. (For further discussions on dither, see Section 5 of this book).

It is important to understand the above point, because single-tone sinewave FFT testing of ADCs is a universally accepted method of performance evaluation. In order to accurately measure the harmonic distortion of an ADC, steps must be taken to ensure that the test setup truly measures the ADC distortion, not the artifacts due to quantization noise correlation. This is done by properly choosing the frequency ratio and sometimes by injecting a small amount of noise (dither) with the input signal.

Now, return to Figure 4.11, and note that the average value of the noise floor of the FFT is greater than 100dB below full scale, but the theoretical SNR of a 12-bit ADC is 74dB. The FFT noise floor is not the SNR of the ADC, because the FFT acts like an analog spectrum analyzer with a bandwidth of $f_s/M$, where $M$ is the number of points in the FFT, rather than $f_s/2$. The theoretical FFT noise floor is therefore $10\log_{10}(M/2)$dB below the quantization noise floor due to the so-called processing gain of the FFT (see Figure 4.12). In the case of an ideal 12-bit ADC with an SNR of 74dB, a 4096-point FFT would result in a processing gain of $10\log_{10}(4096/2) = 33$dB, thereby resulting in an overall FFT noise floor of $74+33=107$dBc. In fact, the FFT noise floor can be reduced even further by going to larger and larger FFTs, just as an analog spectrum analyzer’s noise floor can be reduced by narrowing the bandwidth.
**DISTORTION AND NOISE IN PRACTICAL ADCs**

A practical sampling ADC (one that has an integral sample-and-hold), regardless of architecture, has a number of noise and distortion sources as shown in Figure 4.13. The wideband analog front-end buffer has wideband noise, non-linearity, and also finite bandwidth. The SHA introduces further non-linearity, bandlimiting, and aperture jitter. The actual quantizer portion of the ADC introduces quantization noise, and both integral and differential non-linearity. In this discussion, assume that sequential outputs of the ADC are loaded into a buffer memory of length M and that the FFT processor provides the spectral output. Also assume that the FFT arithmetic operations themselves introduce no significant errors relative to the ADC. However, when examining the output noise floor, the FFT processing gain (dependent on M) must be considered.
Equivalent Input Referred Noise (Thermal Noise)

The wideband ADC internal circuits produce a certain amount of wideband rms noise due to thermal effects. This noise is present even for DC input signals, and accounts for the fact that the output of most wideband ADCs is a distribution of codes, centered around the nominal value of a DC input (see Figure 4.14). To measure its value, the input of the ADC is grounded, and a large number of output samples are collected and plotted as a histogram (sometimes referred to as a grounded-input histogram). Since the noise is approximately Gaussian, the standard deviation of the histogram is easily calculated (see Reference 3), corresponding to the effective input rms noise. It is common practice to express this rms noise in terms of LSBs, although it can be expressed as an rms voltage.
Integral and Differential Non-Linearity

The overall integral non-linearity of an ADC is due to the integral non-linearity of the front-end and SHA as well as the overall integral non-linearity in the ADC transfer function. However, differential non-linearity is due exclusively to the encoding process and may vary considerably dependent on the ADC encoding architecture. Overall integral non-linearity produces distortion products whose amplitude varies as a function of the input signal amplitude. For instance, second-order intermodulation products increase 2dB for every 1dB increase in signal level, and third-order products increase 3dB for every 1dB increase in signal level.

QUANTIFYING ADC DYNAMIC PERFORMANCE

- Harmonic Distortion
- Worst Harmonic
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion Plus Noise (THD + N)
- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
The differential non-linearity in the ADC transfer function produces distortion products which not only depend on the amplitude of the signal but the positioning of the differential non-linearity along the ADC transfer function. Figure 4.16 shows two ADC transfer functions containing differential non-linearity. The left-hand diagram shows an error which occurs at midscale. Therefore, for both large and small signals, the signal crosses through this point producing a distortion product which is relatively independent of the signal amplitude. The right-hand diagram shows another ADC transfer function which has differential non-linearity errors at 1/4 and 3/4 full scale. Signals which are above 1/2 scale peak-to-peak will exercise these codes, while those less and 1/2 scale peak-to-peak will not.

The design of most high-speed ADCs is such that differential non-linearity is spread across the entire ADC range. Therefore, for signals which are within a few dB of full scale, the overall integral non-linearity of the transfer function determines the distortion products. For lower level signals, however, the harmonic content becomes dominated by the differential non-linearities and does not generally decrease proportionally with decreases in signal amplitude.
Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD + N)

There are a number of ways to quantify the distortion of an ADC. An FFT analysis can be used to measure the amplitude of the various harmonics of a signal as shown in Figure 4.17. The harmonics of the input signal can be distinguished from other distortion products by their location in the frequency spectrum. The figure shows a 7MHz input signal sampled at 20MSPS and the location of the first 9 harmonics. Aliased harmonics of $f_a$ fall at frequencies equal to $| \pm Kf_s \pm nf_a |$, where $n$ is the order of the harmonic, and $K = 0, 1, 2, 3, \ldots$. The second and third harmonics are generally the only ones specified on a data sheet because they tend to be the largest, although some data sheets may specify the value of the worst harmonic. Harmonic distortion is normally specified in dBc (decibels below carrier), although at audio frequencies it may be specified as a percentage. Harmonic distortion is specified with an input signal near full scale (generally 0.5 to 1dB below full scale to prevent clipping). For signals much lower than full scale, other distortion products (not direct harmonics) may limit performance.

LOCATION OF HARMONIC DISTORTION PRODUCTS:
INPUT SIGNAL = 7MHz, SAMPLING RATE = 20MSPS

Total harmonic distortion (THD) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics (generally, only the first 5 are significant). THD of an ADC is also generally specified with the input signal close to full scale.

Total harmonic distortion plus noise (THD+N) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding DC). The bandwidth over which the noise is measured must be specified. In the case of an FFT, the bandwidth is DC to $f_s/2$. (If
the bandwidth of the measurement is DC to $f_s/2$, THD+N is equal to SINAD - see below).

**Signal-to-Noise-and-Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), and Effective Number of Bits (ENOB)**

SINAD and SNR deserve careful attention, because there is still some variation between ADC manufacturers as to their precise meaning. Signal-to-noise-and Distortion (SINAD, or S/N+D) is the ratio of the rms signal amplitude to the mean value of the root-sum-square (RSS) of all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC as a function of input frequency because it includes all components which make up noise (including thermal noise) and distortion. It is often plotted for various input amplitudes. SINAD is equal to THD+N if the bandwidth for the noise measurement is the same. A typical plot for the AD9220 12-bit, 10MSPS ADC is shown in Figure 4.19.

**SINAD, ENOB, AND SNR**

- **SINAD (Signal-to-Noise-and-Distortion Ratio):**
  The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC

- **ENOB (Effective Number of Bits):**
  
  $$ENOB = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

- **SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics):**
  The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first 5 harmonics and DC
The SINAD plot shows where the AC performance of the ADC degrades due to high-frequency distortion and is usually plotted for frequencies well above the Nyquist frequency so that performance in undersampling applications can be evaluated. SINAD is often converted to effective-number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC: $\text{SNR} = 6.02N + 1.76\text{dB}$. The equation is solved for $N$, and the value of SINAD is substituted for SNR:

$$\text{ENOB} = \frac{\text{SINAD} - 176\text{dB}}{6.02}.$$ 

Signal-to-noise ratio (SNR, or $\text{SNR-without-harmonics}$) is calculated the same as SINAD except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first 5 harmonics since they dominate. The SNR plot will degrade at high frequencies also, but not as rapidly as SINAD because of the exclusion of the harmonic terms.

Many current ADC data sheets somewhat loosely refer to SINAD as SNR, so the engineer must be careful when interpreting these specifications.

**Analog Bandwidth**

The analog bandwidth of an ADC is that frequency at which the spectral output of the fundamental swept frequency (as determined by the FFT analysis) is reduced by 3dB. It may be specified for either a small signal (SSBW- small signal bandwidth), or a full scale signal (FPBW- full power bandwidth), so there can be a wide variation in specifications between manufacturers.
Like an amplifier, the analog bandwidth specification of a converter does not imply that the ADC maintains good distortion performance up to its bandwidth frequency. In fact, the SINAD (or ENOB) of most ADCs will begin to degrade considerably before the input frequency approaches the actual 3dB bandwidth frequency. Figure 4.20 shows ENOB and full scale frequency response of an ADC with a FPBW of 1MHz, however, the ENOB begins to drop rapidly above 100kHz.

**ADC GAIN (BANDWIDTH) AND ENOB VERSUS FREQUENCY SHOWS IMPORTANCE OF ENOB SPECIFICATION**

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**Spurious Free Dynamic Range (SFDR)**

Probably the most significant specification for an ADC used in a communications application is its spurious free dynamic range (SFDR). The SFDR specification is to ADCs what the third order intercept specification is to mixers and LNAs. SFDR of an ADC is defined as the ratio of the rms signal amplitude to the rms value of the peak spurious spectral content (measured over the entire first Nyquist zone, DC to \(f_s/2\)). SFDR is generally plotted as a function of signal amplitude and may be expressed relative to the signal amplitude (dBc) or the ADC full scale (dBFS).

For a signal near full scale, the peak spectral spur is generally determined by one of the first few harmonics of the fundamental. However, as the signal falls several dB below full scale, other spurs generally occur which are not direct harmonics of the input signal. This is because of the differential non-linearity of the ADC transfer function as discussed earlier. Therefore, SFDR considers all sources of distortion, regardless of their origin.

The AD9042 is a 12-bit, 41MSPS wideband ADC designed for communications applications where high SFDR is important. The SFDR for a 19.5MHz input and a sampling frequency of 41MSPS is shown in Figure 4.21. Note that a minimum of
80dBc SFDR is obtained over the entire first Nyquist zone (DC to 20MHz). The plot also shows SFDR expressed as dBFS.

SFDR is generally much greater than the ADCs theoretical N-bit SNR (6.02N + 1.76dB). For example, the AD9042 is a 12-bit ADC with an SFDR of 80dBc and a typical SNR of 65dBc (theoretical SNR is 74dB). This is because there is a fundamental distinction between noise and distortion measurements. The process gain of the FFT (33dB for a 4096-point FFT) allows frequency spurs well below the noise floor to be observed. Adding extra resolution to an ADC may serve to increase its SNR but may or may not increase its SFDR.

**Two Tone Intermodulation Distortion**

Two tone IMD is measured by applying two spectrally pure sinewaves to the ADC at frequencies f1 and f2, usually relatively close together. The amplitude of each tone is set slightly more than 6dB below full scale so that the ADC does not clip when the two tones add in-phase. The location of the second and third-order products are shown in Figure 4.22. Notice that the second-order products fall at frequencies which can be removed by digital filters. However, the third-order products 2f2–f1 and 2f1–f2 are close to the original signals and are more difficult to filter. Unless otherwise specified, two-tone IMD refers to these third-order products. The value of the IMD product is expressed in dBc relative to the value of *either* of the two original tones, and not to their sum.
Note, however, that if the two tones are close to $f_s/4$, then the aliased third harmonic of the fundamental can make the identification of the actual $2f_2-f_1$ and $2f_1-f_2$ products difficult. Similarly, if the two tones are close to $f_s/3$, the aliased second harmonic may interfere with the measurement.

The concept of second and third-order intercept points is not valid for an ADC, because the distortion products do not vary in a predictable manner (as a function of signal amplitude). The ADC does not gradually begin to compress signals approaching full scale (there is no 1dB compression point), it acts as a hard limiter as soon as the signal exceeds the ADC input range, thereby suddenly producing extreme amounts of distortion because of clipping.

On the other hand, for signals much below full scale, the distortion floor remains relatively constant and is independent of signal level. This is illustrated in Figure 4.23 for the AD9042, where two-tone SFDR is plotted as a function of signal level. The plot indicates that the distortion floor ranges from 85 to 90dBFS regardless of the input signal amplitude.
Noise Power Ratio (NPR)

Noise power ratio testing has been used extensively to measure the transmission characteristics of Frequency Division Multiplexed (FDM) communications links (see Reference 4). In a typical FDM system, 4kHz wide voice channels are "stacked" in frequency bins for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDM data is demultiplexed and returned to 4kHz individual baseband channels. In an FDM system having more than approximately 100 channels, the FDM signal can be approximated by Gaussian noise with the appropriate bandwidth. An individual 4kHz channel can be measured for "quietness" using a narrow-band notch (bandstop) filter and a specially tuned receiver which measures the noise power inside the 4kHz notch (see Figure 4.24).
Noise Power Ratio (NPR) measurements are straightforward. With the notch filter out, the rms noise power of the signal inside the notch is measured by the narrowband receiver. The notch filter is then switched in, and the residual noise inside the slot is measured. The ratio of these two readings expressed in dB is the NPR. Several slot frequencies across the noise bandwidth (low, midband, and high) are tested to characterize the system adequately. NPR measurements on ADCs are made in a similar manner except the analog receiver is replaced by a buffer memory and an FFT processor.

NPR is usually plotted on an NPR curve. The NPR is plotted as a function of rms noise level referred to the peak range of the system. For very low noise loading level, the undesired noise (in non-digital systems) is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1dB increase in noise loading level causes a 1dB increase in NPR. As the noise loading level is increased, the amplifiers in the system begin to overload, creating intermodulation products which cause the noise floor of the system to increase. As the input noise increases further, the effects of "overload" noise predominate, and the NPR is reduced dramatically. FDM systems are usually operated at a noise loading level a few dB below the point of maximum NPR.

In a digital system containing an ADC, the noise within the slot is primarily quantization noise when low levels of noise input are applied. The NPR curve is linear in this region. As the noise level increases, there is a one-for-one correspondence between the noise level and the NPR. At some level, however, "clipping" noise caused by the hard-limiting action of the ADC begins to dominate. A theoretical curve for 10, 11, and 12-bit ADCs is shown in Figure 4.25 (see Reference 5). Peak NPR and corresponding loading levels are shown in Figure 4.26.
THEORETICAL NPR FOR 10, 11, 12-BIT ADCs

ADC RANGE = ±V₀

k = V₀ / σ

σ = RMS NOISE LEVEL

THEORETICAL NPR SUMMARY

<table>
<thead>
<tr>
<th>BITS</th>
<th>k OPTIMUM</th>
<th>k(dB)</th>
<th>MAX NPR (dB)</th>
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</tr>
<tr>
<td>16</td>
<td>5.94</td>
<td>15.47</td>
<td>85.40</td>
</tr>
</tbody>
</table>

ADC Range = ±V₀

k = V₀ / σ

σ = RMS Noise Level

In multi-channel high frequency communication systems, NPR can also be used to simulate the distortion caused by a large number of individual channels, similar to
an FDM system. A notch filter is placed between the noise source and the ADC, and an FFT output is used in place of the analog receiver. The width of the notch filter is set for several MHz as shown in Figure 4.27 for the AD9042. NPR is the “depth” of the notch. An ideal ADC will only generate quantization noise inside the notch, however a practical one has additional noise components due to intermodulation distortion caused by ADC non-linearity. Notice that the NPR is about 60dB compared to 62.7dB theoretical.

Aperture Jitter and Aperture Delay

Another reason that the SNR of an ADC decreases with input frequency may be deduced from Figure 4.28, which shows the effects of phase jitter (or aperture time jitter) on the sampling clock of an ADC (or internal in the sample-and-hold). The phase jitter causes a voltage error which is a function of slew rate and results in an overall degradation in SNR as shown in Figure 4.29. This is quite serious, especially at higher input/output frequencies. Therefore, extreme care must be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system. This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. A very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry.
A decade or so ago, sampling ADCs were built up from a separate SHA and ADC. Interface design was difficult, and a key parameter was aperture jitter in the SHA. Today, most sampled data systems use sampling ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a
cause of concern if the SNR or ENOB is clearly specified, since a guarantee of a specific SNR is an implicit guarantee of an adequate aperture jitter specification. However, the use of an additional high-performance SHA will sometimes improve the high-frequency ENOB of a even the best sampling ADC by presenting "DC" to the ADC, and may be more cost-effective than replacing the ADC with a more expensive one.

It should be noted that there is also a fixed component which makes up the ADC aperture time. This component, usually called effective aperture delay time, does not produce an error. It simply results in a time offset between the time the ADC is asked to sample and when the actual sample takes place (see Figure 4.30), and may be positive or negative. The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications such as I and Q demodulation where two ADCs are required to track each other.

**EFFECTIVE APERTURE DELAY TIME**

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**HIGH SPEED ADC ARCHITECTURES**

**Successive Approximation ADCs**

The successive approximation (SAR) ADC architecture has been used for decades and is still a popular and cost effective form of converter for sampling frequencies of 1MSPS or less. A simplified block diagram of a SAR ADC is shown in Figure 4.31. On the START CONVERT command, all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1". Bit 1 is then tested in the following manner: If the DAC output is greater than the analog input, the MSB is reset, otherwise it is left set. The next most significant bit is then tested by setting it to "1". If the DAC output is greater than the analog input, this bit is reset,
otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the digital value of the analog input, and the conversion is complete.

**SUCCESSIVE APPROXIMATION ADC**

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have a conversion time that is twice as long as an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

The classic SAR ADC is only a quantizer: no sampling takes place, and for an accurate conversion, the input must remain constant for the entire conversion period. Most modern SAR ADCs are sampling types and have an internal sample-and-hold so that they can process AC signals. They are specified for both AC and DC applications. A SHA is required in a SAR ADC because the signal must remain constant during the entire N-bit conversion cycle.

The accuracy of a SAR ADC depends primarily on the accuracy (differential and integral linearity, gain, and offset) of the internal DAC. Until recently, this accuracy was achieved using laser trimmed thin film resistors. Modern SAR ADCs utilize CMOS switched capacitor charge redistribution DACs. This type of DAC depends on the accurate ratio matching and stability of on-chip capacitors rather than thin film resistors. For resolutions greater than 12-bits, on-chip autocalibration techniques using an additional *calibration DAC* and the accompanying logic can accomplish the same thing as thin film laser trimmed resistors, at much less cost. Therefore, the entire ADC can be made on a standard sub-micron CMOS process.
The successive approximation ADC has a very simple structure, is low power, and has reasonably fast conversion times (<1MSPS). It is probably the most widely used ADC architecture, and will continue to be used for medium speed and medium resolution applications.

Current 12-bit SAR ADCs achieve sampling rates up to about 1MSPS, and 16-bit ones up to about 300kSPS. Examples of typical state-of-the-art SAR ADCs are the AD7892 (12-bits at 600kSPS), the AD976/977 (16-bits at 100kSPS), and the AD7882 (16-bits at 300kSPS).

Flash Converters

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of $2^N$ resistors and $2^N - 1$ comparators arranged as in Figure 4.32. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The $2^N - 1$ comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since $2^N - 1$ data outputs are not really practical, they are processed by a decoder to an N-bit binary output.

**FLASH OR PARALLEL ADC**
The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. However, the architecture uses large numbers of resistors and comparators and it limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (>10 mA).

In practice, flash converters are available up to 10-bits, but more commonly they have 8-bits of resolution. Their maximum sampling rate can be as high as 500 MSPS, and input full-power bandwidths in excess of 300 MHz.

But as mentioned earlier, full-power bandwidths are not necessarily full-resolution bandwidths. Ideally, the comparators in a flash converter are well matched both for DC and AC characteristics. Because the strobe is applied to all the comparators simultaneously, the flash converter is inherently a sampling converter. In practice, there are delay variations between the comparators and other AC mismatches which cause a degradation in ENOB at high input frequencies. This is because the inputs are slewing at a rate comparable to the comparator conversion time.

The input to a flash ADC is applied in parallel to a large number of comparators. Each has a voltage-variable junction capacitance, and this signal-dependent capacitance results in all flash ADCs having reduced ENOB and higher distortion at high input frequencies. A model is shown in Figure 4.33, where the input capacitance is modeled as a fixed 10pF capacitor in parallel with a variable capacitor (modeled as a diode with a zero-bias junction capacitance of 6pF). As the input changes from –FS to +FS, the total input capacitance changes from about 12.5 to 16pF. The wideband external drive amplifier is isolated from the flash converter by a 50Ω series resistor. The distortion of this circuit degrades from about 70dBc at 1MHz to 35dBc at 100MHz.
High data rate digital communications applications such as set-top boxes for direct broadcast satellites (DBS) require dual 6 or 8-bit high speed ADCs to perform quadrature demodulation. A dual flash converter ensures good matching between the two ADCs. The AD9066 (dual 6-bit, 60MSPS) flash converter is representative of this type of converter. The AD9066 is fabricated on a BiCMOS process, operates on a single +5V supply, and dissipates 400mW. The effective bit performance of the device is shown in Figure 4.34. Note that the device maintains greater than 5 ENOBs up to 60MSPS analog input.
Part of the reason for the excellent performance of the AD9066 is the use of an interpolation scheme that reduces the number of differential amplifiers required by a factor of two (see Reference 6). The architecture enables 64 possible quantization levels to be determined with only 32 preamplifiers which drive 63 latches. This keeps the input capacitance to a minimum (10pF) and reduces total power dissipation of the device. The basic interpolation circuit is shown in Figure 4.35.
"INTERPOLATING" FLASH REDUCES THE NUMBER OF PREAMPLIFIERS BY FACTOR OF TWO

The preamplifiers are low-gain $g_m$ stages whose bandwidth is proportional to the tail currents of the differential pairs. Consider the case for a positive-going ramp input which is initially below the reference to AMP A1, V1. As the input signal approaches V1, the differential output of A1 approaches zero (i.e., $A = \overline{A}$), and the decision point is reached. The output of A1 drives the differential input of LATCH 1. As the input signals continue to go positive, A continues to go positive, and $\overline{B}$ begins to go negative. The interpolated decision point is determined when $A = \overline{B}$. As the input continues positive, the third decision point is reached when $B = \overline{B}$. This novel architecture reduces the ADC input capacitance and thereby minimizes its change with signal level and the associated distortion. The input capacitance of the AD9066 is only about 10pF. Key specifications for the device are summarized in Figure 4.36.

**AD9066 DUAL 6-BIT, 60MSPS FLASH ADC**

**KEY SPECIFICATIONS**

- **Input Range**: 500mV p-p
- **Input Impedance**: $50k\Omega \parallel 10pF$
- **ENOB**: 5.7 bits @ 15.5MHz Input
- **On-Chip Reference**
- **Power Supply**: Single +5V
- **Power Dissipation**: 400mW
Subranging (Pipelined) ADCs

Although it is not practical to make flash ADCs with high resolution, flash ADCs are often used as subsystems in "subranging" ADCs (sometimes known as "half-flash ADCs"), which are capable of much higher resolutions (up to 16-bits).

A block diagram of an 8-bit subranging ADC based upon two 4-bit flash converters is shown in Figure 4.37. Although 8-bit flash converters are readily available at high sampling rates, this example will be used to illustrate the theory. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit DAC (again, better than 8-bit accurate). The DAC output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the residue signal range does not exactly fill the range of the second flash converter, non-linearities and perhaps missing codes will result.

Modern subranging ADCs use a technique called digital correction to eliminate problems associated with the architecture of Figure 4.37. A simplified block diagram...
of a 12-bit digitally corrected subranging (DCS) ADC is shown in Figure 4.38. The architecture is similar to that used in the AD9042 12-bit, 41MSPS ADC. Note that a 6-bit and an 7-bit ADC have been used to achieve an overall 12-bit output. These are not flash ADCs, but utilize a magnitude-amplifier (MagAmp™) architecture which will be described shortly.

If there were no errors in the first-stage conversion, the 6-bit "residue" signal applied to the 7-bit ADC by the summing amplifier would never exceed one-half of the range of the 7-bit ADC. The extra range in the second ADC is used in conjunction with the error correction logic (usually just a full adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter architecture. It is important to note that the 6-bit DAC must be better than 12-bit accurate, because the digital error correction does not correct for DAC errors. In practice, "thermometer" or "fully-decoded" DACs using one current switch per level (63 switches in the case of a 6-bit DAC) are often used instead of a "binary" DAC to ensure excellent differential and integral linearity and minimum switching transients.

The second SHA delays the held output of the first SHA while the first-stage conversion occurs, thereby maximizing throughput. The third SHA serves to deglitch the residue output signal, thereby allowing a full conversion cycle for the 7-bit ADC to make its decision (the 6 and 7-bit ADCs in the AD9042 are bit-serial MagAmp ADCs which require more settling time than a flash converter).

This multi-stage conversion technique is sometimes referred to as "pipelining." Additional shift registers in series with the digital outputs of the first-stage ADC ensure that its output is ultimately time-aligned with the last 7 bits from the second ADC when their outputs are combined in the error correction logic. A
pipelined ADC therefore has a specified number of clock cycles of latency, or pipeline delay associated with the output data. The leading edge of the sampling clock (for sample N) is used to clock the output register, but the data which appears as a result of that clock edge corresponds to sample N – L, where L is the number of clock cycles of latency. In the case of the AD9042, there are two clock cycles of latency. Key specifications for the AD9042 are shown in Figure 4.39.

**AD9042 12-BIT, 41MSPS ADC KEY SPECIFICATIONS**

- Input Range: 1V peak-to-peak, $V_{cm} = +2.4V$
- Input Impedance: 250Ω to $V_{cm}$
- Effective Input Noise: 0.33LSBs rms
- SFDR at 20MHz Input: 80dB minimum
- SINAD ($S/N+D$) at 20MHz Input = 67dB
- Digital Outputs: TTL Compatible
- Power Supply: Single +5V
- Power Dissipation: 595mW
- Fabricated on High Speed Dielectrically Isolated Complementary Bipolar Process

The error correction scheme described above is designed to correct for errors made in the first conversion. Internal ADC gain, offset, and linearity errors are corrected as long as the residue signal fall within the range of the second-stage ADC. These errors will not affect the linearity of the overall ADC transfer characteristic. Errors made in the final conversion, however, do translate directly as errors in the overall transfer function. Also, linearity errors or gain errors either in the DAC or the residue amplifier will not be corrected and will show up as nonlinearities or non-monotonic behavior in the overall ADC transfer function.

So far, we have considered only two-stage subranging ADCs, as these are easiest to analyze. There is no reason to stop at two stages, however. Three-pass and four-pass subranging pipelined ADCs are quite common, and can be made in many different ways, usually with digital error correction.

A simplified block diagram of the AD9220 12-bit, 10MSPS single-supply, 250mW CMOS ADC is shown in Figure 4.40. The AD9221 (1.25MSPS, 60mW) and the AD9223 (3MSPS, 100mW) ADCs use the identical architecture but operate at lower power and lower sampling rates. This is a four-stage pipelined architecture with an additional bit in the second, third, and fourth stage for error correction. Because of
the pipelined architecture, these ADCs have a 3 clock-cycle latency (see Figure 4.41). Key specifications for the AD9220/9221/9223 are given in Figure 4.42.

**AD9220/9221/9223 12-BIT PIPELINED CMOS ADC**

![Diagram of AD9220/9221/9223 ADC]

**LATENCY (PIPELINE DELAY) OF AD9220/9221/9223 ADC**

![Diagram showing latency of AD9220/9221/9223 ADC]

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AD9220, AD9221, AD9223
CMOS 12-BIT ADCs KEY SPECIFICATIONS

- Family Members:
  AD9221 (1.25MSPS), AD9223 (3MSPS), AD9220 (10MSPS)
- Power Dissipation: 60, 100, 250mW, Respectively
- FPBW: 25, 40, 60MHz, Respectively
- Effective Input Noise: 0.1LSB rms (Span = 5V)
- SINAD: 71dB
- SFDR: 88dBc
- On-Chip Reference
- Differential Non-Linearity: 0.3LSB
- Single +5V Supply
- 28-Pin SOIC Package

Bit-Per-Stage (Serial, or Ripple) ADCs

Various architectures exist for performing A/D conversion using one stage per bit. In fact, a multistage subranging ADC with one bit per stage and no error correction is one form. Figure 4.43 shows the overall concept. The SHA holds the input signal constant during the conversion cycle. There are N stages, each of which have a bit output and a residue output. The residue output of one stage is the input to the next. The last bit is detected with a single comparator as shown.
The basic stage for performing a single binary bit conversion is shown in Figure 4.44. It consists of a gain-of-two amplifier, a comparator, and a 1-bit DAC. The comparator detects the zero-crossing of the input and is the binary bit output for that stage. The comparator also switches a 1-bit DAC whose output is summed with the output of the gain-of-two amplifier. The resulting residue output is then applied to the next stage.
A simplified 3-bit serial-binary ADC is shown in Figure 4.45, and the residue outputs are shown in Figure 4.46. Each residue output signal has discontinuities which correspond to the point where the comparator changes state and causes the DAC to switch. The fundamental problem with this architecture is the discontinuity in the residue output waveforms. Adequate settling time must be allowed for these transients to propagate through all the stages and settle at the final comparator input. The prospects of making this architecture operate at high speed are therefore dismal.
A much better bit-per-stage architecture was developed by F.D. Waldhauer (Reference 7) based on absolute value amplifiers (magnitude amplifiers, or simply MagAmps™). This scheme has often been referred to as serial-Gray (since the output coding is in Gray code), or folding converter (References 8, 9, 10). The basic stage is
shown functionally in Figure 4.47. The comparator detects the polarity of the input signal and provides the Gray bit output for the stage. It also determines whether the overall stage gain is +2 or –2. The reference voltage $V_R$ is summed with the switch output to generate the residue signal which is applied to the next stage. The transfer function for the folding stage is also shown in Figure 4.47.

**MagAmp STAGE FUNCTIONAL EQUIVALENT CIRCUIT**

A 3-bit MagAmp folding ADC is shown in Figure 4.48, and the corresponding residue waveforms in Figure 4.49. Notice that there is no abrupt transition in any of the folding stage output waveforms.
The key to operating this architecture at high speeds is the folding stage. Early designs (see References 7, 8, 9) used discrete op amps with diodes inside the feedback loop to generate the folding transfer function. Modern IC circuit designs implement the transfer function using current-steering open-loop gain techniques.
which can be made to operate much faster. Fully differential stages (including the SHA) also provide speed, lower distortion, and yield 8-bit accurate folding stages with no requirement for thin film resistor laser trimming.

An example of a fully differential gain-of-two MagAmp folding stage is shown in Figure 4.50 (see References 11, 12, 13). The differential input signal is applied to the degenerated-emitter differential pair Q1, Q2 and the comparator. The differential input voltage is converted into a differential current which flows in the collectors of Q1, Q2. If +IN is greater than −IN, cascode-connected transistors Q3, Q6 are on, and Q4, Q5 are off. The differential signal currents therefore flow through the collectors of Q3, Q6 into level-shifting transistors Q7, Q8 and into the output load resistors, developing the differential output voltage between +OUT and −OUT. The overall differential voltage gain of the circuit is two.

If +IN is less than −IN (negative differential input voltage), the comparator changes stage and turns Q4, Q5 on and Q3, Q6 off. The differential signal currents flow from Q5 to Q7 and from Q4 to Q8, thereby maintaining the same relative polarity at the differential output as for a positive differential input voltage. The required offset voltage is developed by adding a current I_{OFF} to the emitter current of Q7 and subtracting it from the emitter current of Q8.

The differential residue output voltage of the stage drives the next stage input, and the comparator output represents the Gray code output for the stage.

![Circuit Details of MagAmp Stage](image)

The MagAmp architecture can be extended to sampling rates previously dominated by flash converters. The AD9059 8-bit, 60MSPS dual ADC is shown in Figure 4.51. The first five bits (Gray code) are derived from five differential MagAmp stages. The differential residue output of the fifth MagAmp stage drives a 3-bit flash converter, rather than a single comparator. The Gray-code output of the five MagAmps and the
binary-code output of the 3-bit flash are latched, all converted into binary, and latched again in the output data register. Key specifications for the AD9059 are shown in Figure 4.52.

**AD9059 DUAL 8-BIT, 60MSPS ADC FUNCTIONAL DIAGRAM**

**AD9059 DUAL 8-BIT, 60MSPS ADC KEY SPECIFICATIONS**

- Input Range: 1V p-p, Vcm = +2.5V
- Input Impedance: 200kΩ || 5pF
- ENOB: 7.3 @ 10.3MHz Input
- On-Chip Reference
- Power Supply: Single +5V Supply (+5 or +3V Digital)
- Power Dissipation: 375mW (Power Down: 10mW)
- Package: 28-lead SSOP
- Ideal for Quadrature Demodulation in DBS Set-Top Boxes
REFERENCES

1. **Active and Passive Electrical Wave Filter Catalog**, Vol. 34, TTE, Incorporated, 2251 Barry Avenue, Los Angeles, CA 90064.


32. **HP Product Note** 5180A-2.


41. Mathcad™ 4.0 software package available from MathSoft, Inc., 201 Broadway, Cambridge MA, 02139.

SECTION 5
HIGH SPEED ADC APPLICATIONS
Walt Kester, Brad Brannon, Paul Hendricks

DRIVING ADC INPUTS FOR LOW DISTORTION AND WIDE DYNAMIC RANGE

In order to achieve wide dynamic range in high speed ADC applications, careful attention must be given to the analog interface. Many ADCs are designed so that analog signals can be interfaced directly to their inputs without the necessity of a drive amplifier. This is especially true in ADCs such as the AD9220/21/23 family and the AD9042, where even a low distortion drive amplifier may result in some degradation in AC performance. If a buffer amplifier is required, it must be carefully selected so that its distortion and noise performance is better than that of the ADC.

Single-supply ADCs generally yield optimum AC performance when the common-mode input voltage is centered between the supply rails (although the optimum common-mode voltage may be skewed slightly in either direction about this point depending upon the particular design). This also eases the drive requirement on the input buffer amplifier (if required) since even “rail-to-rail” output op amps give best distortion performance if their output is centered about mid-supply, and the peak signals are kept at least 1V from either rail.

Typical high speed single-supply ADC peak-to-peak input voltage ranges may vary from about 0.5V to 5V, but in most cases, 1V to 2V peak-to-peak represents the optimum tradeoff between noise and distortion performance.

In single-supply applications requiring DC coupling, careful attention must be given to the input and output common-mode range of the driving amplifier. Level shifting is often required in order to center a ground-referenced signal within the allowable common-mode input range of the ADC.

Small RF transformers are quite useful in AC coupled applications, especially if the ADC has differential inputs. Significant improvement in even-order distortion products and common-mode noise rejection may be realized, depending upon the characteristics of the ADC.

An understanding of the input structure of the ADC is therefore necessary in order to properly design the analog interface circuitry. ADCs designed on CMOS processes typically connect the sample-and-hold switches directly to the analog input, thereby generating transient current pulses. These transients may significantly degrade performance if the settling time of the op amp is not sufficiently fast. On the other hand, ADCs designed on bipolar processes may present a relatively benign load to the drive amplifier with minimal transient currents.

The data sheet for the ADC is the prime source an engineer should use in designing the interface circuits. It should contain recommended interface circuits and spell out relevant tradeoffs. However, no data sheet can substitute for a fundamental understanding of what’s inside the ADC.
HIGH SPEED ADC INPUT CONSIDERATIONS

- Selection of Drive Amplifier (Only if Needed!)
- Single Supply Implications
- Input Range (Span): Typically 1V to 2V peak-to-peak for best distortion / noise tradeoff
- Input Common-Mode Range: \( V_S / 2 \) (Nominally) for Single Supply ADCs
- Differential vs. Single-Ended
- AC Coupling Using Transformers
- Input Transient Currents

Switched-Capacitor Input ADCs

The AD9220/21/23-series of ADCs are excellent examples of the progress that has been made in utilizing low-cost CMOS processes to achieve a high level of performance. A functional block diagram is shown in Figure 5.2. This family of ADCs offers sampling rates of 1.25MSPS (AD9221), 3MSPS (AD9223), and 10MSPS (AD9220) at power dissipations of 60, 100, and 250mW respectively. Key specifications for the family of ADCs are given in Figure 5.3. The devices contain an on-chip reference voltage which allows the full scale span to be set at 2V or 5V peak-to-peak (full scale spans between 2V and 5V can be set by adding two external gain setting resistors).
AD9220, AD9221, AD9223
CMOS 12-BIT ADCs KEY SPECIFICATIONS

- Family Members:
  AD9221 (1.25MSPS), AD9223 (3MSPS), AD9220 (10MSPS)

- Power Dissipation: 60, 100, 250mW, Respectively

- FPBW: 25, 40, 60MHz, Respectively

- Effective Input Noise: 0.1LSB rms (Span = 5V)

- SINAD: 71dB

- SFDR: 88dBc

- On-Chip Reference

- Differential Non-Linearity: 0.3LSB

- Single +5V Supply

- 28-Pin SOIC Package
The input circuit of the AD9220/21/23-series of CMOS ADCs contains the differential sample-and-hold as shown in Figure 5.4. The switches are shown in the track mode. They open and close at the sampling frequency. The 16pF capacitors represent the effective capacitance of switches S1 and S2 plus the stray input capacitance. The $C_S$ capacitors (4pF) are the sampling capacitors, and the $C_H$ capacitors are the hold capacitors. Although the input circuit is completely differential, the ADC can be driven either single-ended or differential. Optimum SFDR, however, is obtained using a differential transformer drive.

**SIMPLIFIED INPUT CIRCUIT OF AD922X ADC FAMILY**

In the track mode, the differential input voltage is applied to the $C_S$ capacitors. When the circuit enters the hold mode, the voltage across the sampling capacitors is transferred to the $C_H$ hold capacitors and buffered by the amplifier A. (The switches are controlled by the appropriate phases of the sampling clock). When the SHA returns to the track mode, the input source must charge or discharge the voltage stored on $C_S$ to the new input voltage. This action of charging and discharging $C_S$, averaged over a period of time and for a given sampling frequency $f_s$, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_s$), the input impedance is dynamic, and hence certain precautions on the input drive source should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by $C_H$ from the input drive source. It can be shown that if $C_S$ is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a
resistor equal to \(1/(C_s f_s)\) connected between the inputs. Since \(C_s\) is only a few picofarads, this resistive component is typically greater than several k\(\Omega\) for an \(f_s = 10\text{MSPS}\).

If one considers the SHA’s input impedance over a sampling period, it appears as a dynamic load to the input drive source. When the SHA returns to the track mode, the input source should ideally provide the charging current through the \(R_{on}\) of switches S1 and S2 in an exponential manner. The requirement of exponential charging means that the source impedance should be both low and resistive up to and beyond the sampling frequency.

The output impedance of an op amp can be modeled as a series inductor and resistor. When a capacitive load is switched onto the output of the op amp, the output will momentarily change due to its effective high frequency output impedance. As the output recovers, ringing may occur. To remedy this situation, a series resistor can be inserted between the op amp and the SHA input. The optimum value of this resistor is dependent on several factors including the sampling frequency and the op amp selected, but in most applications, a 30 to 50\(\Omega\) resistor is optimum.

The input voltage span of the AD922X-family is set by pin-strap options using the internal voltage reference (see Figure 5.5). The common-mode voltage can be set by either pin strap or applying the common-mode voltage to the VINB pin. Tradeoffs can be made between noise and distortion performance. Maximum input range allowable is 5V peak-to-peak, in which case, the common-mode input voltage must be one-half the supply voltage, or +2.5V. The minimum input range is 2V peak-to-peak, in which case the common-mode input voltage can be set from +1V to +4V. For best DC linearity and maximum signal-to-noise ratio, the ADC should be operated with an input signal of 5V peak-to-peak. However, for best high frequency noise and distortion performance, 2V peak-to-peak with a common-mode voltage of +2.5V is preferred. This is because the CMOS FET on-resistance is a minimum at this voltage, and the non-linearity caused by the signal-dependence of \(R_{on}\) (\(R_{on}\) modulation effect) is also minimal.

### AD922X ADC INPUT VOLTAGE RANGE OPTIONS

#### SINGLE-ENDED INPUT

<table>
<thead>
<tr>
<th>Input Signal Range (Volts)</th>
<th>Peak-to-Peak Signal (Volts)</th>
<th>Common-Mode Voltage (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +2</td>
<td>2</td>
<td>+1</td>
</tr>
<tr>
<td>0 to +5</td>
<td>5</td>
<td>+2.5</td>
</tr>
<tr>
<td>+1.5 to +3.5</td>
<td>2</td>
<td>+2.5</td>
</tr>
</tbody>
</table>

#### DIFFERENTIAL INPUT

<table>
<thead>
<tr>
<th>Input Signal Range</th>
<th>Peak-to-Peak Signal</th>
<th>Common-Mode Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Volts)</td>
<td>Differential (Volts)</td>
<td>(Volts)</td>
</tr>
<tr>
<td>--------------</td>
<td>----------------------</td>
<td>---------</td>
</tr>
<tr>
<td>+2 to +3</td>
<td>2</td>
<td>+2.5</td>
</tr>
<tr>
<td>+1.25 to +3.75</td>
<td>5</td>
<td>+2.5</td>
</tr>
</tbody>
</table>

Figure 5.6 shows the THD performance of the AD9220 for a 2V peak-to-peak input signal span and common-mode input voltage of 2.5V and 1V. The data was taken with a single-ended drive. Note that the performance is significantly better for $V_{cm} = +2.5V$.

**AD9220 THD VS. INPUT FREQUENCY: SINGLE-ENDED DRIVE**

2V p-p INPUT, $V_{cm} = +1V$ AND $V_{cm} = +2.5V$, $f_s = 10$MSPS

A simple single-ended circuit for AC coupling into the inputs of the AD9220-family is shown in Figure 5.7. Note that the common-mode input voltage is set for +2.5V by the 4.99kΩ resistors. The input impedance is also balanced for optimum distortion performance.
If the input to the ADC is coming from a long coaxial cable run, it may be desirable to buffer the transient currents at the ADC inputs from the cable to prevent problems resulting from reflections, especially if the cable is not source-terminated. The circuit shown in Figure 5.8 uses the low distortion AD8011 op amp as a buffer which can optionally provide signal gain. In all cases, the feedback resistor should be fixed at 1kΩ for best op amp performance, since the AD8011 is a current-feedback type. In this type of arrangement, care must be taken to observe the allowable input and output range of the op amp. The AD8011 input common-mode range (operating on a single +5V supply) is from +1.5 to +3.5V, and its output +1V to +4V. The ADC should be operated with a 2V peak-to-peak input range. The 33Ω series resistor is required to isolate the output of the AD8011 from the effective input capacitance of the ADC. The value was empirically determined to yield the best high-frequency SINAD.
Direct coupling of ground-referenced signals using a single supply requires the use of an op amp with an acceptable common-mode input voltage, such as the AD8041 (input can go to 200mV below ground). The circuit shown in Figure 5.9 level shifts the ground-referenced bipolar input signal to a common-mode voltage of +2.5V at the ADC input. The common-mode bias voltage of +2.5V is developed directly from an AD780 reference, and the AD8041 common-mode voltage of +1.25V is derived with a simple divider.
Transformer coupling provides the best CMR and the lowest distortion. Figure 5.10 shows the suggested circuit. The transformer is a Mini-Circuits RF transformer, model #T4-6T which has an impedance ratio of four (turns ratio of 2). The schematic assumes that the signal source has a 50Ω source impedance. The 1:4 impedance ratio requires the 200Ω secondary termination for optimum power transfer and VSWR. The Mini-Circuits T4-6T has a 1dB bandwidth from 100kHz to 100MHz. The center tap of the transformer provides a convenient means of level shifting the input signal to the optimum common-mode voltage. The AD922X CML pin is used to provide the +2.5 common-mode voltage.
Transformers with other turns ratios may also be selected to optimize the performance for a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio (i.e. Mini-Circuits #T16-6T with a 1:16 impedance ratio, turns ratio 1:4) effectively "steps up" the signal level thus reducing the driving requirements of the signal source.

Note the 33Ω series resistors inserted between the transformer secondary and the ADC input. These values were specifically selected to optimize both the SFDR and the SNR performance of the ADC. They also provide isolation from transients at the ADC inputs. Transients currents are approximately equal on the VINA and VINB inputs, so they are isolated from the primary winding of the transformer by the transformer's common-mode rejection.

Transformer coupling using a common-mode voltage of +2.5V provides the maximum SFDR when driving the AD922X-series. By driving the ADC differentially, even-order harmonics are reduced compared with the single-ended circuit. Figure 5.11 shows a plot of SFDR and SNR for the transformer-coupled differential drive circuit using 2V p-p and 5V p-p inputs and a common-mode voltage of +2.5V. Note that the SFDR is greater than 80dBc for input signals up to full scale with a 5MHz input signal.
Figure 5.11 also shows differences between the SFDR and SNR performance for 2V p-p and 5V p-p inputs. Note that the SNR with a 5V p-p input is approximately 2dB to 3dB better than that for a 2V p-p input because of the additional dynamic range provided by the larger input range. Also, the SFDR performance using a 5V p-p input is 3 to 5dB better for signals between about –6dBFS and –36dBFS. This improvement in SNR and SFDR for the 5V p-p input range may be advantageous in systems which require more than 6dB headroom to minimize clipping of the ADC.

**Driving Bipolar Input ADCs**

Bipolar technology is typically used for extremely high performance ADCs with wide dynamic range and high sampling rates such as the AD9042. The AD9042 is a state-of-the-art 12-bit, 41MSPS two stage subranging ADC consisting of a 6-bit coarse ADC and a 7-bit residue ADC with one bit of overlap to correct for any DNL, INL, gain or offset errors of the coarse ADC, and offset errors in the residue path. A block diagram is shown in Figure 5.12 and key specifications in Figure 5.13. A proprietary gray-code architecture is used to implement the two internal ADCs. The gain alignments of the coarse and residue, likewise the subtraction DAC, rely on the statistical matching of the devices on the process. As a result, 12-bit integral and differential linearity is obtained without laser trim. The internal DAC consists of 126 interdigitated current sources. Also on the DAC reference, there are an additional 20 interdigitated current sources to set the coarse gain, residue gain, and full scale gain. The interdigitization removes the requirement for laser trim. The AD9042 is fabricated on a high speed dielectrically isolated complementary bipolar process. The total power dissipation is only 575mW when operating on a single +5V supply.
The outstanding performance of the AD9042 is partly due to the use of differential techniques throughout the device. The low distortion input amplifier converts the single-ended input signal into a differential one. If maximum SFDR performance is
desired, the signal source should be coupled directly into the input of the AD9042 without using a buffer amplifier. Figure 5.14 shows a method using capacitive coupling. Transformer coupling can also be used if desired.

**INPUT STRUCTURE OF AD9042 ADC IS DESIGNED TO BE DRIVEN DIRECTLY FROM 50Ω SOURCE FOR BEST SFDR**

The AD9050 is a 10-bit, 40MSPS single supply ADC designed for wide dynamic range applications such as ultrasound, instrumentation, digital communications, and professional video. Like the AD9042, it is fabricated on a high speed complementary bipolar process. A block diagram of the AD9050 (Figure 5.15) illustrates the two-step subranging architecture, and key specifications are summarized in Figure 5.16.
The analog input circuit of the AD9050 (see Figure 5.17) is differential, but can be driven either single-endedly or differentially with equal performance. The input signal range of the AD9050 is ±0.5V centered around a common-mode voltage of...
+3.3V, which makes single supply op amp selection more difficult since the amplifier has to drive +3.8V peak signals with low distortion.

**AD9050 SIMPLIFIED INPUT CIRCUIT**

The input circuit of the AD9050 is a relatively benign and constant 5kΩ in parallel with approximately 5pF. Because of its well-behaved input, the AD9050 can be driven directly from 50, 75, or 100Ω sources without the need for a low-distortion buffer amplifier. In ultrasound applications, it is normal to AC couple the signal (generally between 1MHz and 15MHz) into the AD9050 differential inputs using a wideband transformer as shown in Figure 5.18. The Mini-Circuits T1-1T transformer has a 1dB bandwidth from 200kHz to 80MHz. Signal-to-noise plus distortion (SINAD) values of 57dB (9.2 ENOB) are typical for a 10MHz input signal. If the input signal comes directly from a 50, 75, or 100Ω single-ended source, capacitive coupling as shown in Figure 5.18 can be used.
If DC coupling is required, the AD8041 (zero-volt in, rail-to-rail output) op amp can be used as a low distortion driver. The circuit shown in Figure 5.19 level shifts a ground-referenced video signal to fit the $+3.3\,\text{V} \pm 0.5\,\text{V}$ input range of the AD9050. The source is a ground-referenced 0 to $+2\,\text{V}$ signal which is series-terminated in $75\,\Omega$. The termination resistor, $R_T$, is chosen such that the parallel combination of $R_T$ and $R_1$ is $75\,\Omega$. The AD8041 op amp is configured for a signal gain of $-1$. Assuming that the video source is at zero volts, the corresponding ADC input voltage should be $+3.8\,\text{V}$. The common-mode voltage, $V_{cm}$, is determined from the following equation:

$$V_{cm} = 3.8 \left( \frac{R_S \parallel R_T + R_1}{R_S \parallel (R_T + R_1 + R_2)} \right) = 3.8 \left( \frac{38.8 + 1000}{38.8 + 1000 + 1000} \right) = 1.94\,\text{V}$$

The common-mode voltage, $V_{cm}$, is derived from the common-mode voltage at the inverting input of the AD9050. The $+3.3\,\text{V}$ is buffered by the AD820 single-supply FET-input op amp. A divider network generates the required $+1.94\,\text{V}$ for the AD8011, and a potentiometer provides offset adjustment capability.

The AD8041 voltage feedback op amp was chosen because of its low power (26mW), wide bandwidth (160MHz), and low distortion (–69dBc at 10MHz). It is fully specified for both $\pm 5\,\text{V}$, $+5\,\text{V}$, and $+3\,\text{V}$ operation. When operating on a single $+5\,\text{V}$ supply, the input common-mode range is $-0.2\,\text{V}$ to $+4\,\text{V}$, and the output swing is $+0.1\,\text{V}$ to $+4.9\,\text{V}$. Distortion performance of the entire circuit including the ADC is better than $-60\,\text{dBc}$ for an input frequency of 10MHz and a sampling rate of 40MSPS.
DC-COUPLED SINGLE-SUPPLY DRIVE CIRCUIT FOR AD9050 10-BIT, 40MSPS ADC USING AD8041 OP AMP

$V_{CM} = +1.94V$

$72mV TO 1.072V$

$R_S = 75\Omega$

$0 \text{ TO } +2V$

AD8041

$R_1 = 1000\Omega$

$R_2 = 10\text{ k}\Omega$

$0.1\mu F$

$+5V$

AD9050

$+3.3V$

$+5V$

$8k\Omega$

$16k\Omega$

$3.8V \text{ TO } 2.8V$

$0.1\mu F$

$8k\Omega$

$+5V$

$16k\Omega$

$+3.8V \text{ TO } 2.8V$

$V_{CM} = +1.94V$

$72mV \text{ TO } 1.072V$

$R_S = 75\Omega$

$0 \text{ TO } +2V$

AD8041

$R_1 = 1000\Omega$

$R_2 = 10\text{ k}\Omega$

$0.1\mu F$

$+5V$

AD9050

$+3.3V$

$+5V$

$8k\Omega$

$16k\Omega$

$3.8V \text{ TO } 2.8V$

$0.1\mu F$

$8k\Omega$

$+5V$

$16k\Omega$
APPLICATIONS OF HIGH SPEED ADCs IN CCD IMAGING

Charge coupled devices (CCDs) contain a large number of small photocells called photosites or pixels which are arranged either in a single row (linear arrays) or in a matrix (area arrays). CCD area arrays are commonly used in video applications, while linear arrays are used in facsimile machines, graphics scanners, and pattern recognition equipment.

The linear CCD array consists of a row of image sensor elements (photosites, or pixels) which are illuminated by light from the object or document. During one exposure period each photosite acquires an amount of charge which is proportional to its illumination. These photosite charge packets are subsequently switched simultaneously via transfer gates to an analog shift register. The charge packets on this shift register are clocked serially to a charge detector (storage capacitor) and buffer amplifier (source follower) which convert them into a string of photo-dependent output voltage levels (see Figure 5.20). While the charge packets from one exposure are being clocked out to the charge detector, another exposure is underway. The analog shift register typically operates at frequencies between 1 and 10MHz.

![Linear CCD Array Diagram](image)

The charge detector readout cycle begins with a reset pulse which causes a FET switch to set the output storage capacitor to a known voltage. Switching the FET causes capacitive feedthrough which results in a reset glitch at the output as shown in Figure 5.21. The switch is then opened, isolating the capacitor, and the charge from the last pixel is dumped onto the capacitor causing a voltage change. The difference between the reset voltage and the final voltage (video level) shown in Figure 5.21 represents the amount of charge in the pixel. CCD charges may be as
low as 10 electrons, and a typical CCD output sensitivity is 0.6µV/electron. Most CCDs have a saturation output voltage of about 1V (see Reference 1).

Since CCDs are generally fabricated on MOS processes, they have limited capability to perform on-chip signal conditioning. Therefore, the CCD output is generally processed by external conditioning circuits.

CCD output voltages are small and quite often buried in noise. The largest source of noise is the thermal noise in the resistance of the FET reset switch. This noise may have a typical value of 100 to 300 electrons rms (approximately 60 to 180mV rms). This noise occurs as a sample-to-sample variation in the CCD output level and is common to both the reset level and the video level for a given pixel period. A technique called correlated double sampling (CDS) is often used to reduce the effect of this noise. Figure 5.22 shows two circuit implementations of the CDS scheme. In the top circuit, the CCD output drives both SHAs. At the end of the reset interval, SHA1 holds the reset voltage level. At the end of the video interval, SHA2 holds the video level. The SHA outputs are applied to a difference amplifier which subtracts one from the other. In this scheme, there is only a short interval during which both SHA outputs are stable, and their difference represents \( \Delta V \), so the difference amplifier must settle quickly to the desired resolution.

Another arrangement is shown in the bottom half of Figure 5.22, which uses three SHAs and allows either for faster operation or more time for the difference amplifier to settle. In this circuit, SHA1 holds the reset level so that it occurs simultaneously with the video level at the input to SHA2 and SHA3. When the video clock is applied simultaneously to SHA2 and SHA3, the input to SHA2 is the reset level, and the input to SHA3 the video level. This arrangement allows the entire pixel period (less the acquisition time of SHA2 and SHA3) for the difference amplifier to settle.
The AD9807 is a complete CCD imaging decoder and signal processor on a single chip (see Figure 5.23). The input of the AD9807 allows direct AC coupling of the CCD outputs and includes all the circuitry to perform three-channel correlated double sampling (CDS) and programmable gain adjustment (1X to 4X in 16 increments) of the CCD output. A 12-bit ADC quantizes the analog signal (maximum sampling frequency 6MSPS). After digitization, the on-board DSP allows pixel rate offset and gain correction. The DSP also corrects odd/even CCD register imbalance errors. A parallel control bus provides a simple interface to 8-bit microcontrollers. The device operates on a single +5V supply and dissipates 500mW. The AD9807 comes in a space saving 64-pin plastic quad flat pack (PQFP). By disabling the CDS, the AD9807 is also suitable for non-CCD applications that do not require CDS. The AD9807 is also offered in a pin-compatible 10-bit version, the AD9805, to allow upgradeability and simplify design issues across different scanner models.
**HIGH SPEED ADC APPLICATIONS IN DIGITAL RECEIVERS**

**Introduction**

Consider the analog superheterodyne receiver invented in 1917 by Major Edwin H. Armstrong (see Figure 5.24). This architecture represented a significant improvement over single-stage direct conversion (homodyne) receivers which had previously been constructed using tuned RF amplifiers, a single detector, and an audio gain stage. A significant advantage of the superheterodyne receiver is that it is much easier and more economical to have the gain and selectivity of a receiver at fixed intermediate frequencies (IF) than to have the gain and frequency-selective circuits "tune" over a band of frequencies.

**U.S. ADVANCED MOBILE PHONE SERVICE (AMPS) SUPERHETERODYNE ANALOG RECEIVER**

The frequencies shown in Figure 5.24 correspond to the AMPS (Advanced Mobile Phone Service) analog cellular phone system currently used in the U.S. The receiver is designed for AMPS signals at 900MHz RF. The signal bandwidth for the "A" or "B" carriers serving a particular geographical area is 12.5MHz (416 channels, each 30kHz wide). The receiver shown uses triple conversion, with a first IF frequency of 70MHz and a second IF of 10.7MHz, and a third of 455kHz. The image frequency at the receiver input is separated from the RF carrier frequency by an amount equal to twice the first IF frequency (illustrating the point that using relatively high first IF frequencies makes the design of the image rejection filter easier).

The output of the third IF stage is demodulated using analog techniques (discriminators, envelope detectors, synchronous detectors, etc.). In the case of AMPS the modulation is FM. An important point to notice about the above scheme
is that there is *one receiver required per channel*, and only the antenna, prefilter, and LNA can be shared.

It should be noted that in to make the receiver diagrams more manageable, the interstage amplifiers are not shown. They are, however, an important part of the receiver, and the reader should be aware that they must be present.

Receiver design is a complicated art, and there are many tradeoffs that can be made between IF frequencies, single-conversion vs. double-conversion or triple conversion, filter cost and complexity at each stage in the receiver, demodulation schemes, etc. There are many excellent references on the subject, and the purpose of this section is only to acquaint the design engineer with some of the emerging architectures, especially in the application of digital techniques in the design of advanced communications receivers.

**A Receiver Using Digital Processing at Baseband**

With the availability of high performance high speed ADCs and DSPs (such as ADSP-2181 and the ADSP-21062), it is now becoming common practice to use digital techniques in at least part of the receive and transmit path, and various chipsets are available from Analog Devices to perform these functions for GSM and other cellular standards. This is illustrated in Figure 5.25 where the output of the last IF stage is converted into a baseband in-phase (I) and quadrature (Q) signal using a quadrature demodulator. The I and Q signals are then digitized by two ADCs. The DSPs then perform the additional signal processing. The signal can then be converted into analog format using a DAC, or it can be processed, mixed with other signals, upconverted, and retransmitted.

![Digital Receiver Using Baseband Sampling and Digital Processing](image-url)
At this point, we should make it clear that a digital receiver is not the same thing as digital modulation. In fact, a digital receiver will do an excellent job of receiving an analog signal such as AM or FM. Digital receivers can be used to receive any type of modulation standard including analog (AM, FM) or digital (QPSK, QAM, FSK, GMSK, etc.). Furthermore, since the core of a digital radio is its digital signal processor (DSP), the same receiver can be used for both analog and digitally modulated signals (simultaneously if necessary), assuming that the RF and IF hardware in front of the DSP is properly designed. Since it is software that determines the characteristics of the radio, changing the software changes the radio. For this reason, digital receivers are often referred to as software radios.

The fact that a radio is software programmable offers many benefits. A radio manufacturer can design a generic radio in hardware. As interface standards change (as from FM to CDMA or TDMA), the manufacturer is able to make timely design changes to the radio by reprogramming the DSP. From a user or service-providers point of view, the software radio can be upgraded by loading the new software at a small cost, while retaining all of the initial hardware investment. Additionally, the receiver can be tailored for custom applications at very low cost, since only software costs are involved.

A digital receiver performs the same function as an analog one with one difference; some of the analog functions have been replaced with their digital equivalent. The main difference between Figure 5.24 and Figure 5.25 is that the FM discriminator in the analog radio has been replaced with two ADCs and a DSP. While this is a very simple example, it shows the fundamental beginnings of a digital, or software radio.

An added benefit of using digital techniques is that some of the filtering in the radio is now performed digitally. This eliminates the requirement of tight tolerances and matching for frequency-sensitive components such as inductors and capacitors. In addition, since filtering is performed within the DSP, the filter characteristics can be implemented in software instead of costly and sensitive SAW, ceramic, or crystal filters. In fact, many filters can be synthesized digitally that could never be implemented in a strictly analog receiver.

This simple example is only the beginning. With current technology, much more of the receiver can be implemented in digital form. There are numerous advantages to moving the digital portion of the radio closer to the antenna. In fact, placing the ADC at the output of the RF section and performing direct RF sampling might seem attractive, but does have some serious drawbacks, particularly in terms of selectivity and out-of-band (image) rejection. However, the concept makes clear one key advantage of software radios: they are programmable and require little or no component selection or adjustments to attain the required receiver performance.

**Narrowband IF-Sampling Digital Receivers**

A reasonable compromise in many digital receivers is to convert the signal to digital form at the output of the first or the second IF stage. This allows for out-of-band signals to be filtered before reaching the ADC. It also allows for some automatic gain control (AGC) in the analog stage ahead of the ADC to reduce the possibility of in-band signals overdriving the ADC and allows for maximum signal gain prior to the A/D conversion. This relieves some of the dynamic range requirements on the ADC.
Additionally, IF sampling and digital receiver technology reduce costs by elimination of further IF stages (mixers, filters, and amplifiers) and adds flexibility by the replacement of fixed analog filter components with programmable digital ones.

In analyzing an analog receiver design, much of the signal gain is after the first IF stage. This prevents front-end overdrive due to out-of-band signals or strong in-band signals. However, in an IF sampling digital receiver, all of the gain is in the front end, and great care must be taken to prevent in-band and out-of-band signals from saturating the ADC, which results in excessive distortion. Therefore, a method of attenuation must be provided when large in-band signals occur. While additional signal gain can be obtained digitally after the ADC, there are certain restrictions. Gain provided in the analog domain improves the SNR of the signal and only reduces the performance to the degree that the noise figure (NF) degrades noise performance.

Figure 5.26 shows a detailed IF sampling digital receiver for the GSM system. The receiver has RF gain, automatic gain control (AGC), a high performance ADC, digital demodulator/filter, and a DSP.

The heart of the system is the AD6600 dual channel, gain ranging 11-bit, 20MSPS ADC with RSSI (Received Signal Strength Indicator) and the AD6620 dual channel decimating receiver. A detailed block diagram of the AD6600 is shown in Figure 5.27 and key specifications in Figure 5.28.
AD6600 DUAL CHANNEL GAIN RANGING ADC WITH RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

AD6600 KEY SPECIFICATIONS

- Dual Input, 11-bit, 20MSPS ADC Plus 3-bits RSSI
- Dynamic Range > 100dB
  - 11-bit ADC → 62dB
  - 3-bits RSSI → 30dB (5 levels, 6dB / level)
  - Process Gain → 12dB (6.5MSPS Sampling, 200kHz Channel)
- On-Chip Reference and Timing
- Single +5V Supply, 400mW
- 44-pin TQFP Package
- Optimum Design for Narrowband Digital Receivers with IF Frequencies to 250MHz

The AD6600 is a mixed signal chip that directly samples narrow band signals at IF frequencies up to 250MHz. The device includes an 11-bit, 20MSPS ADC, input attenuators, automatic gain ranging circuitry, a 450MHz bandwidth track-and-hold,
digital RSSI outputs, references, and control circuitry. The device accepts two inputs (for use with diversity antennas) which are multiplexed to the single ADC.

The AD6600 provides greater than 92dB dynamic range from the ADC and the auto gain-ranging/RSSI circuits. The gain range is 36dB in 6dB increments (controlled by a 3-bit word from the RSSI circuit). This sets the smallest input range at 31mV peak-to-peak, and the largest at 2V peak-to-peak. SFDR is 70dBc @ 100MHz and 53dBc @ 250MHz. Channel isolation is 70dB @ 100MHz and 60dB @ 250MHz. The SNR performance of the AD6600 is shown in Figure 5.29. The dynamic range of the AD6600 is greater than the minimum GSM specification of 91dB.

AD6600 INPUT VS. SNR

The analog input to the AD6600 consists of two parallel attenuator stages followed by an output selection multiplexer. The attenuation levels can be set either by the on-chip automatic RSSI circuit (synchronous peak detector) or can be set digitally with external logic. The ADC T/H input can also be accessed directly by by-passing the front-end attenuators.

An external analog filter is required between the attenuator output and the track-and-hold input of the ADC section. This filter may be either a lowpass or a bandpass depending on the system architecture. Since the input bandwidth of the ADC is 450MHz, the filter minimizes the wideband noise entering the track-and-hold. The bandwidth of the filter should be set to allow sufficient settling time (1/2 the sampling period) during the RSSI peak detection period.
The ADC is based on the high dynamic range AD9042 architecture covered previously. The ADC input is designed to take advantage of the excellent small-signal linearity of the track-and-hold. Therefore, the full scale input to the ADC section is only 50mV peak-to-peak. The track-and-hold is followed by a gain block with a 6dB gain-select to increase the signal level for digitization by the 11-bit ADC. This amplifier only requires enough bandwidth to accurately settle to the next value during the sampling period (77ns for $f_s = 13$MSPS). Because of its reduced bandwidth, any high frequency track-and-hold feed through is also minimized.

The RSSI peak detector function consists of a bank of 5 high speed comparators with separate reference inputs. Each reference input is 6dB lower than the previous one. Each comparator has 6dB of built-in hysteresis to eliminate level uncertainty at the threshold points. Once one of the comparators is tripped, it stays in that state until it is reset by the negative-going edge of the sampling clock. The 5 comparator outputs are decoded into a 3-bit word that is used to select the proper input attenuation.

The RSSI follows the IF signal one clock cycle before the conversion is made. During this time period, the RSSI looks for the signal peaks. Prior to digitization, the RSSI word selects the correct attenuator factor to prevent the ADC from over-ranging on the following conversion cycle. The peak signal is set 6dB below the full scale range of the 11-bit ADC. The RSSI word can be read via the RSSI pins. The 11-bit ADC output functions as the mantissa, while the RSSI word is the exponent, and the combination forms a floating point number.

The AD6600 is ideal for use in a GSM narrowband basestation. Figure 5.30 shows a block diagram of the fundamental receiver. Two separate antennas and RF sections are used (this is often called diversity) to reduce the signal strength variations due to multipath effects. The IF output (approximately 70MHz) of each channel is digitized by the AD6600 at a sampling rate of 6.5MSPS (one-half the master GSM clock frequency of 13MHz). The two antennas need only be separated by a few feet to provide the required signal strength diversity (the wavelength of a 900MHz signal is about 1 foot). The DSP portion of the receiver selects the channel which has the largest signal amplitude.
The bandwidth of a single GSM channel is 200kHz, and each channel can handle up to 8 simultaneous callers for full-rate systems and 16 simultaneous callers for the newer one-half-rate systems. A typical basestation may be required to handle 50 to 60 simultaneous callers, thereby requiring 4 separate signal processing channels (assuming a one-half-rate system).

The IF frequency is chosen to be 69.875MHz, thus centering the 200kHz signal in the 22nd Nyquist zone (see Figure 5.31). The dual channel digital decimating receiver (AD6620) reverses the frequency sense of the signal and shifts it down to baseband.
We now have a 200kHz baseband signal (generated by undersampling) which is being oversampled by a factor of approximately 16.

The signal is then passed through a digital filter (part of the AD6620) which removes all frequency components above 200kHz, including the quantization noise which falls in the region between 200kHz and 3.25MHz (the Nyquist frequency) as shown in Figure 5.32. The resultant increase in SNR is 12dB (processing gain). There is now no information contained in the signal above 200kHz, and the output data rate can be reduced (decimated) from 6.5MSPS to 406.25kSPS, a data rate which the DSP can handle. The data corresponding to the 200kHz channel is transmitted to the DSP over a simple 3-wire serial interface. The DSP performs such functions as channel equalization, decoding, and spectral shaping.
The concept of processing gain is common to all communications systems, analog or digital. In a sampling system, the quantization noise produced by the ADC is spread over the entire Nyquist bandwidth which extends from DC to $f_s/2$. If the signal bandwidth, $BW$, is less than $f_s/2$, digital filtering can remove the noise components outside this bandwidth, thereby increasing the effective SNR. The processing gain in a sampling system can be calculated from the formula:

$$\text{Processing Gain} = 10 \log \left( \frac{f_s}{2 \cdot BW} \right).$$

The SINAD (noise and distortion measured over $f_s/2$ bandwidth) of the ADC at the bandwidth of the signal should be used to compute the actual SINAD by adding the processing gain determined by the above equation. If the ADC is an ideal N-bit converter, then its SNR (measured over the Nyquist bandwidth) is $6.02N + 1.76$dB.
SINAD in Signal Bandwidth = SINAD + \(10\log\left(\frac{f_s}{2 \cdot BW}\right)\)

SINAD (Theoretical) = 6.02N + 1.76dB + \(10\log\left(\frac{f_s}{2 \cdot BW}\right)\)

Processing Gain Increases 3dB each time \(f_s\) is doubled

Notice that as shown in the previous narrowband receiver example, there can be processing gain even if the original signal is an undersampled one. The only requirement is that the signal bandwidth be less than \(f_s/2\), and that the noise outside the signal bandwidth be removed with a digital filter.

**Wideband IF-Sampling Digital Receivers**

Thus far, we have avoided a detailed discussion of narrowband versus wideband digital receivers. A digital receiver can be either, but more detailed definitions are important at this point. By narrowband, we mean that sufficient pre-filtering has been done such that all undesired signals have been eliminated and that only the signal of interest is presented to the ADC input. This is the case for the GSM basestation example previously discussed.

Wideband simply means that a number of channels are presented to input of the ADC and further filtering, tuning, and processing is performed digitally. Usually, a wideband receiver is designed to receive an entire band; cellular or other similar wireless services such as PCS (Personal Communications Systems). In fact, one wideband digital receiver can be used to receive all channels within the band simultaneously, allowing almost all of the analog hardware (including the ADC) to be shared among all channels as shown in Figure 5.34 which compares the narrowband and the wideband approaches.
Note that in the narrowband digital radio, there is one front-end LO and mixer required per channel to provide individual channel tuning. In the wideband digital radio, however, the first LO frequency is fixed, and the “tuning” is done in the **digital channelizer** circuits following the ADC.

A typical wideband digital receiver may process a 5 to 25MHz band of signals simultaneously. This approach is frequently called **block conversion**. In the wideband digital receiver, the variable local oscillator in the narrowband receiver has been replaced with a fixed oscillator, so tuning must be accomplished digitally. Tuning is performed using a digital down converter (DDC) and filter chip frequently called a **channelizer**. The term channelizer is used because the purpose of these chips is to select one channel out of the many within the broadband spectrum actually present in the ADC output. A typical channelizer is shown in Figure 5.35.
It consists of an NCO (Numerically Controlled Oscillator) with tuning capability, dual mixer, and matched digital filters. These are the same functions that would be required in an analog receiver, but implemented in digital form. The digital output from the channelizer is the demodulated signal in I and Q format, and all other signals have been filtered and removed. Since the channelizer output consists of one selected RF channel, one channelizer is required for each channel. The channelizer also serves to decimate the output data rate such that it can be processed by a DSP such as the ADSP-2181 or the ADSP-21062. The DSP extracts the signal information from the I and Q data and performs further processing. Another effect of the filtering provided by the channelizer is to increase the SNR by adding processing gain.

In the case of an AMPS signal, there are 416 channels, each 30kHz wide, for a total bandwidth of 12.5MHz (each of the two carriers in a given region are allocated 12.5MHz of the total 25MHz cellular band). Each channel carries one call, so there is a clear advantage in using the wideband approach versus the narrowband one in an AMPS basestation which must handle between 50 and 60 simultaneous calls. On the other hand, a 200kHz GSM channel can carry 16 calls simultaneously (for half-rate systems), so only three or four channels are required in the typical GSM basestation, and the narrowband approach is more cost-effective. Using today’s technology (1996), the break-even cost point between narrowband and wideband ranges from two and eight channels.

In an ADC used for narrowband applications, the key specifications are SINAD, SFDR, and SNR. The narrowband ADC can take advantage of automatic gain ranging (as in the AD6600) to account for signal amplitude variations between individual channels and thereby achieve extra dynamic range.
On the other hand, an ADC used in a wideband receiver must digitize all channels simultaneously, thereby eliminating the possibility of per-channel analog gain ranging. For example, the GSM (European Digital Cellular) system specification requires the receiver to process signals between −13dBm and −104dBm (with a noise floor of −114dBm) in the presence of many other signals. This is a dynamic range of 91dB! This implies that the SFDR of the ADC and the analog front end must be approximately 95 to 100dBFS, allowing for additional headroom. In addition, the GSM system has 124 channels, each having a bandwidth of 200kHz for a total signal bandwidth of 25MHz. The minimum required sampling rate for an ADC suitable for wideband GSM is therefore greater than 50MSPS.

SFDR is a very important specification when a mobile phone is near the basestation because it is an indication of how strong signals interfere with signals in other channels. Strong signals usually produce the largest spurs due to front-end distortion, and these spurs can mask weaker signals from mobile phones near the cell fringes. The SFDR for weak signals provides an indication of the overall noise floor, or SINAD which can ultimately be related to the receiver bit error rate (BER).

When digitizing a wideband signal, full scale single-tone evaluations are no longer sufficient. Two-tone and multiple-tone intermodulation testing in conjunction with SFDR amplitude sweeps are better indicators of performance.

### GSM VERSUS AMPS COMPARISONS

<table>
<thead>
<tr>
<th></th>
<th>GSM</th>
<th>AMPS</th>
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</thead>
<tbody>
<tr>
<td><strong>Digital Receiver</strong></td>
<td>Narrowband</td>
<td>Wideband</td>
</tr>
<tr>
<td><strong># of Channels</strong></td>
<td>124</td>
<td>416</td>
</tr>
<tr>
<td><strong>Channel BW</strong></td>
<td>200kHz</td>
<td>30kHz</td>
</tr>
<tr>
<td><strong>Total BW</strong></td>
<td>25MHz</td>
<td>12.5MHz</td>
</tr>
<tr>
<td><strong>Callers/Channel</strong></td>
<td>16 (one-half rate)</td>
<td>1</td>
</tr>
<tr>
<td><strong>ADC Requirements</strong></td>
<td>11-bits with RSSI</td>
<td>12-bits</td>
</tr>
<tr>
<td></td>
<td>6.5 MSPS</td>
<td>30.72 MSPS</td>
</tr>
<tr>
<td></td>
<td>92dB Dynamic Range</td>
<td>80dB SFDR</td>
</tr>
<tr>
<td><strong>Process Gain</strong></td>
<td>12dB</td>
<td>27dB</td>
</tr>
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</table>

The AMPS cellular system basestation is ideally suited to the wideband digital receiver design, and a simplified diagram of one is shown in Figure 5.37. The AD9042 sampling frequency of 30.72MSPS is chosen to be a power-of-two multiple
of the channel bandwidth (30kHz x 1024). Another popular AMPS wideband receiver sampling frequency is 40.96MSPS. The choice of IF frequency is flexible, and a second IF stage may be required if lower IF frequencies are chosen.

**AMPS WIDEBAND DIGITAL RECEIVER**

With a sampling frequency of 30.72MSPS, the 12.5MHz bandwidth signal can be positioned in the first Nyquist zone (DC to 15.36MHz) with an IF frequency of 7.68MHz, or in the second Nyquist zone (15.36MHz to 30.72MHz) with an IF frequency of 23.04MHz.

With a sampling frequency of 40.96MSPS, the 12.5 MHz bandwidth signal can be positioned in the first Nyquist zone (DC to 20.48MHz) with an IF frequency of 10.24MHz, or in the second Nyquist zone (20.48MHz to 40.96MHz) with an IF frequency of 30.72MHz.

The digital channelizers provide the receiver tuning and demodulate the signal into the I and Q components. The output data rate to the DSPs after decimation is 60kSPS. The processing gain incurred is calculated as follows:

\[
\text{Processing Gain} = 10 \log \left( \frac{30.72}{2 \times 0.03} \right) = 27.1 \text{dB}.
\]

**AMPS WIDEBAND RECEIVER PROCESS GAIN**

- \(f_s = 30.72 \text{MSPS} \quad (1024 \cdot 30\text{kHz})\)
- Channel BW = 30kHz
In addition to SFDR, two-tone and multi-tone intermodulation distortion is important in an ADC for wideband receiver applications. Figure 5.39 shows two strong signals in two adjacent channels at frequencies $f_1$ and $f_2$. If the ADC has third-order intermodulation distortion, these products will fall at $2f_2 - f_1$ and $2f_1 - f_2$ and are indistinguishable from signals which might be present in these channels. This is one reason the GSM system is difficult to implement using the wideband approach, since the dynamic range requirement is greater than 91dB.

The two-tone SFDR of the AD9042 is greater than 80dB with input tones at 15.3MHz and 19.5MHz as shown in Figure 5.40. Note than the amplitude of each tone must be 6dB below full scale in order to prevent the ADC from being overdriven. The two-tone SFDR as a function of input signal amplitude is shown in Figure 5.41 for tone frequencies of 19.3MHz and 19.51MHz. The upper curve is in dBFS, and the lower in dBc. Note that the SFDR is greater than 80dBFS for all input amplitudes. Figure 5.42 shows a multitone FFT output for the AD9042, and the ADC still maintains 85dBFS of SFDR.
AD9042 TWO-TONE FFT OUTPUT
F1 = 15.3MHz, F2 = 19.5MHz, f_s = 41MSPS

AD9042 TWO-TONE SFDR
F1 = 19.3MHz, F2 = 19.51MHz, f_s = 41MSPS
Direct IF-to-Digital Considerations

The dynamic performance of the AD9042 extends well beyond 20MHz analog input signals (see Figure 5.43). Therefore it can be used to perform direct IF-to-digital conversions using a wide range of IF frequencies. These IF signals can be undersampled as previously described, and the minimum sampling frequency required is determined by the bandwidth of the IF signal. Figure 5.44 shows a 21.4MHz signal sampled at 10MSPS using the AD9042. Note that under these conditions, the SFDR performance is greater than 80dBFS.
The AD6640 represents the next generation in IF sampling ADCs. Key specifications for the AD6640 are summarized in Figure 5.45. The architecture is similar to that of the AD9042, but the device is fabricated on a faster XFCB process. The input structure is fully differential and designed for transformer coupling for
minimum distortion. Maximum sampling frequency is 65MSPS, and the SINAD performance is 67dB at 60MHz analog input. SFDR is greater than 80dBFS for frequencies up to 25MHz. This device allows direct IF sampling in wideband communications systems having bandwidths up to 25MHz (such as the AMPS system, where each carrier is allocated 12.5MHz of spectrum). For systems with smaller bandwidths, the higher sampling frequency provided by the AD6640 will allow analog antialiasing filter requirements to be relaxed and provide processing gain. In undersampling applications, the device can be used to digitize 70MHz IF signals which lie in the second or third Nyquist zone. For instance, a 30MHz wideband signal bandwidth centered around a carrier frequency of 48.75MHz can be digitized at 65MSPS as shown in Figure 5.46. In narrowband applications, the high sampling frequency can be used to achieve additional processing gain.

**AD6640 12-BIT, 65MSPS ADC KEY SPECIFICATIONS**

- 12-bit, 65MSPS IF-SAMPLING ADC
- Based on AD9042 architecture, but 1.5X faster CB process
- Fully differential inputs for optimum distortion performance
- SFDR Greater than 80dB up to 25MHz Input
- 68dB SINAD for 60MHz IF input
- Single +5V Supply, 695mW
- 44-Lead TQFP Package
Achieving Wide Dynamic Range in High Speed ADCs Using Dither

There are two fundamental limitations to maximizing SFDR in a high speed ADC. The first is the distortion produced by the front-end amplifier and the sample-and-hold circuit. The second is that produced by non-linearity in the actual transfer function of the encoder portion of the ADC. The key to wide SFDR is to minimize the non-linearity of each.

There is nothing that can be done externally to the ADC to significantly reduce the inherent distortion caused by the ADC front end. However, the non-linearity in the ADC encoder transfer function can be reduced by the proper use of dither (external noise which is summed with the analog input signal to the ADC).

Dithering improves ADC SFDR under certain conditions. For example, even in a perfect ADC, there is some correlation between the quantization noise and the input signal. This can reduce the SFDR of the ADC, especially if the input signal is an exact sub-multiple of the sampling frequency. Summing broadband noise (about 1/2 LSB rms in amplitude) with the input signal tends to randomize the quantization noise and minimize this effect (see Figure 5.47). In most systems, however, there is enough noise riding on top of the signal so that adding additional dither noise is not required. Increasing the wideband rms noise level beyond an LSB will proportionally reduce the ADC SNR.
Other schemes have been developed which use larger amounts of dither noise to randomize the transfer function of the ADC. Figure 5.47 also shows a dither noise source comprised of a pseudo-random number generator which drives a DAC. This signal is subtracted from the ADC input signal and then digitally added to the ADC output, thereby causing no significant degradation in SNR. An inherent disadvantage of this technique is that the allowable input signal swing is reduced as the amplitude of the dither signal is increased. This reduction in signal amplitude is required to prevent overdriving the ADC. It should be noted that this scheme does not significantly improve distortion created by the front-end of the ADC, only that produced by the non-linearity of the ADC encoder transfer function.

Another method which is easier to implement, especially in wideband receivers, is to inject a narrowband dither signal outside the signal band of interest as shown in Figure 5.48. Usually, there are no signal components located in the frequency range near DC, so this low-frequency region is often used for such a dither signal. Another possible location for the dither signal is slightly below f_s/2. Because the dither signal occupies only a small bandwidth relative to the signal bandwidth, there is no significant degradation in SNR, as would occur if the dither was broadband.
A subranging ADC such as the AD9042 (see Figure 5.49) has small differential non-linearity errors that occur at specific regions across the ADC range. For instance, the AD9042 uses a 6-bit ADC followed by a 7-bit one. There are 64 decision points associated with the main-range 6-bit ADC, and they occur every 15.625mV for a 1V full scale input range. Figure 5.50 shows a greatly exaggerated representation of these non-linearities.
The distortion components produced by the front end of the AD9042 up to about 20MHz analog input are negligible compared to those produced by the encoder. That
The static non-linearity of the AD9042 transfer function is the chief limitation to SFDR.

The goal is to select the proper amount of out-of-band dither so that the effect of these small DNL errors are randomized across the ADC input range, thereby reducing the average DNL error. The first plot shown in Figure 5.51 shows the undithered DNL over a small portion of the input signal range. The horizontal axis has been expanded to show two of the subranging points which are spaced 15.625mV (64 LSBs) apart. The second plot shows the DNL after adding 5.3mV rms (22 LSBs rms) of dither. This amount of dither corresponds to –32.5dBm (1V p-p full scale corresponds to +4dBm). It was determined that further increases in dither amplitude provided no improvement in the AD9042 SFDR and would only serve to cause a loss in headroom and a decrease in SNR.

![AD9042 UNDITHERED AND DITHERED DNL](image)

The dither signal was generated using a voltage feedback op amp (AD8048, 3.8nV/√Hz input voltage noise, 200MHz gain-bandwidth product) as the noise source (see Figure 5.52). The op amp is configured for a gain of +26, and the output noise spectral density is about 100nV/√Hz over an 8MHz bandwidth. The output of the noise generator is then amplified by the AD600 dual wideband VCA which provides a gain (in dB) which is proportional to the control voltage. The control voltage can be fixed, or programmed using a DAC as shown. The gain of the AD600 can be set from 0dB to 80dB by varying the control voltage from 0 to +1V. The bandwidth of the noise is limited to about 300kHz with a lowpass filter. The filter can be either passive or active, but requires at least 4 poles in order to attenuate the out-of-band noise. The output of the lowpass filter is buffered with the AD797 low-noise op amp which also provides a gain of +2. The filtered noise is summed directly into the input circuit of the AD9042 through a capacitor and a 1kΩ series resistor. The net input impedance of the AD9042 is 50Ω (61.9Ω in parallel with the 250Ω AD9042 internal impedance).
The dramatic improvement in SFDR obtained with out-of-band dither is shown in Figure 5.53 using a 4k FFT, where the AD9042 is sampling a 19.5MHz signal (–29dBFS) at 41MSPS. Note that the SFDR without dither is approximately 80dBFS compared to 94dBFS with dither, representing a 14dB improvement! This improvement is also shown in the SFDR amplitude sweeps shown in Figure 5.54. Note the similar improvement.
At lower frequencies, the FFT size must be increased from 4k to 128k (reducing the FFT noise floor by 15dB) in order to measure the dithered SFDR. Figure 5.55 shows the effects of dither using a 128k FFT and a 2.5MHz input signal. The SFDR with dither is greater than 100dBFS.
High Speed ADC Applications in Digital Communications Systems and Direct Broadcast Satellite (DBS) Set-Top Boxes

In a digital communications system, digital data (which can be digitized analog signals) is formatted and transmitted serially over an appropriate medium. The GSM cellular telephone system is an example. The ubiquitous modem (modulator/demodulator), which PCs and FAX machines use to transmit and receive data over the standard dial-up telephone connection, uses sophisticated modulation techniques to place huge amounts of data in the 4kHz bandwidth telephone channel.

Most digital transmission schemes use some form of in-phase and quadrature (I and Q) modulation to maximize the amount of data transmitted over a given channel bandwidth. Two examples are shown in Figure 5.56 and Figure 5.57. The first is called Quadrature Phase Shift Keying (QPSK) and is used in Direct Broadcast Satellite systems. The diagram (constellation) shows the four possible data points, each representing 2-bits of binary information. Each point in the constellation is called a symbol and has a specific I and Q value. In the case of QPSK, there are two bits of information per symbol. The symbol rate is often referred to as the baud rate. For example, in QPSK, if the symbol (or baud) rate is 30Mbaud (1baud = 1symbol/sec), the bit rate is 60Mbits/sec. It is common practice to sample these types of signals at twice the symbol (or baud) rate. The I and Q ADC and DSP must identify the signal as representing one of two possible levels, and ADCs of 4, 5, or 6-bits are commonly used in this application for additional noise margin and to achieve the overall system bit-error-rate (BER) requirement.
In the QPSK system, the magnitude of each symbol is equal, and only the phase is modulated. More complex modulation schemes such as QAM (Quadrature Amplitude Modulation), use more symbols on the constellation and thereby transmit more bits of information per symbol (at the expense of more sensitivity to noise and more complex digital signal processing). Figure 5.57 shows a 16-QAM constellation which contains 4-bits of information per symbol. Note that the I and Q channel receiver DSP must now identify the signal as representing one of the four possible levels. Although the 16-QAM signal carries more bits per symbol, it is more sensitive to noise, and the ADC requires more resolution (typically 8-bits) than for QPSK modulation (typically 4, 5, or 6 bits).
In the digital receiver, the I and Q components are separated by a quadrature demodulator and digitized by two ADCs operating in parallel. The ADC sampling rate is generally twice the symbol rate. In the case of Direct Broadcast Satellite (DBS), the symbol rate is 30Mbaud (1baud = 1symbol/sec), the bit rate 60Mbits/sec, and the ADC sampling rate is 60MSPS. The actual signals at the ADC input are called "eye patterns" because the intersymbol interference due to noise and limited bandwidth smears the level transitions so that the regions where the data is valid are located in the center of the eye opening. Figure 5.58 shows a typical I/Q demodulator followed by a dual ADC such as the AD9066 (6-bits, 60MSPS).
A recent popular consumer application of digital communications is in Direct Broadcast Satellite (DBS) systems. A simplified block diagram of a DBS system is shown in Figure 5.59. The objective is to transmit up to 150 channels of video programming to home receivers which use a small (18 inch) dish and an inexpensive (less than $500) receiver (set-top box). The subscription costs of the services is compatible with cable TV, but picture quality (because of digital transmission inherent noise immunity) is generally superior over all 150 channels.
MPEG encoding and decoding reduces the data rates to fit the channel bandwidth. The MPEG (Motion Picture Experts Group) standard supports various data rates and minimizes the bandwidth used. For example, a typical 24-frame-per-second NTSC-quality movie needs about 3Mbits/sec after encoding. A more complex and fast-moving show, such as a soccer game, requires 5 to 6 Mbits/sec. In a DBS system, the MPEG encoding rate is kept at a minimum value compatible with the anticipated video signal characteristics. Multiple MPEG data streams are multiplexed and sent through a single satellite transponder. In addition, statistical multiplexing dynamically varies the data rate given to each source as the program content changes.

The satellite downlink frequency is Ku-band (12.2 to 12.7GHz), and the transponder output power is about 120W (10 to 20 times that of a typical communications satellite which is designed for much larger receiver antennas). The LNB (Low Noise Block Converter) converts the 12.2 to 12.7GHz untuned band down to 950MHz to 1450MHz, where the signal is easier to tune, filter, and bring into the home over standard coaxial cable. The lower frequency signal (1GHz) incurs less loss over standard coaxial cable from the outside antenna to the inside of the house (generally 50 feet or more) than the Ku-band signal (12GHz).

The set-top box mixes the RF (1GHz) signal down to the first fixed IF frequency of 480MHz. The LO which drives the mixer is used for channel tuning. A second fixed-frequency IF stage brings the tuned signal down to 70MHz where it is synchronously demodulated into baseband I and Q components. The modulation scheme is QPSK, the symbol rate is 30Mbaud, and the ADC sampling rate 60MSPS.

Figure 5.60 shows a two-chip solution to the front-end of the set-top box using the AD6461 (quadrature demodulator and baseband filter) and the AD6462 (dual 5-bit
ADC and digital receiver). The input to the AD6461 is the 480MHz DBS IF signal. The chip-set is designed to support symbol rates up to 42.5Mbaud. The AD6461 utilizes Analog Devices' XFCB process and is packaged in 28-pin SOIC dissipating about 500mW. The AD6462 utilizes a 0.6 micron CMOS process and is packaged in an 80-pin PQFP dissipating approximately 1.2W (operating dynamically).
REFERENCES


A frequency synthesizer generates multiple frequencies from one or more frequency references. These devices have been used for decades, especially in communications systems. Many are based upon switching and mixing frequency outputs from a bank of crystal oscillators. Others have been based upon well understood techniques utilizing phase-locked loops (PLLs). This mature technology is illustrated in Figure 6.1. A fixed-frequency reference drives one input of the phase comparator. The other phase comparator input is driven from a divide-by-N counter which is in turn driven by a voltage-controlled-oscillator (VCO). Negative feedback forces the output of the internal loop filter to a value which makes the VCO output frequency N-times the reference frequency. The time constant of the loop is controlled by the loop filter.

There are many tradeoffs in designing a PLL, such as phase noise, tuning speed, frequency resolution, etc., and there are many good references on the subject (see References 1, 2, and 3).

With the widespread use of digital techniques in instrumentation and communications systems, a digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The basic architecture is shown in Figure 6.2. In this simplified model, a stable clock drives a programmable-read-only-memory (PROM) which stores one or more integral number of cycles of a sinewave (or other arbitrary
As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal. The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock.

The DDS system differs from the PLL in several ways. Because a DDS system is a sampled data system, all the issues involved in sampling must be considered: quantization noise, aliasing, filtering, etc. For instance, the higher order harmonics of the DAC output frequencies fold back into the Nyquist bandwidth, making them unfilterable, whereas, the higher order harmonics of the output of PLL-based synthesizers can be filtered. There are other considerations which will be discussed shortly.

A fundamental problem with this simple DDS system is that the final output frequency can be changed only by changing the reference clock frequency or by reprogramming the PROM, making it rather inflexible. A practical DDS system implements this basic function in a much more flexible and efficient manner using digital hardware called a Numerically Controlled Oscillator (NCO). A block diagram of such a system is shown in Figure 6.3.
The heart of the system is the phase accumulator whose contents is updated once each clock cycle. Each time the phase accumulator is updated, the digital number, $M$, stored in the delta phase register is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator is 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, $2^{32}$ clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. (Actually, only data for 90° is required because the quadrature data is contained in the two MSBs). The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC.

Consider the case for $n=32$, and $M=1$. The phase accumulator steps through each of $2^{32}$ possible outputs before it overflows. The corresponding output sinewave frequency is equal to the clock frequency divided by $2^{32}$. If $M=2$, then the phase accumulator register "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows.

For an $n$-bit phase accumulator ($n$ generally ranges from 24 to 32 in most DDS systems), there are $2^n$ possible phase points. The digital word in the delta phase register, $M$, represents the amount the phase accumulator is incremented each clock cycle. If $f_c$ is the clock frequency, then the frequency of the output sinewave is equal to:

$$f_o = \frac{M \cdot f_c}{2^n}$$
\[ f_0 = \frac{M \cdot f_c}{2^n}. \]

This equation is known as the DDS "tuning equation." Note that the frequency resolution of the system is equal to \( f_c/2^n \). For \( n=32 \), the resolution is greater than one part in four billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are truncated, leaving only the first 13 to 15 MSBs. This reduces the size of the lookup table and does not affect the frequency resolution. The phase truncation only adds a small but acceptable amount of phase noise to the final output.

The resolution of the DAC is typically 2 to 4 bits less than the width of the lookup table. Even a perfect N-bit DAC will add quantization noise to the output. Figure 6.4 shows the calculated output spectrum for a 32-bit phase accumulator, 15-bit phase truncation, and a 12-bit DAC. The value of \( M \) was chosen so that the output frequency was slightly offset from 0.25 times the clock frequency. Note that the spurs caused by the phase truncation and the finite DAC resolution are all at least 90dB below the fullscale output. This performance far exceeds that of any commercially available 12-bit DAC and is adequate for most applications.

CALCULATED OUTPUT SPECTRUM SHOWS 90dB SFDR FOR 15-BIT PHASE TRUNCATION AND 12-BIT OUTPUT DATA TRUNCATION

The basic DDS system described above is extremely flexible and has high resolution. The frequency can be changed instantaneously with no phase discontinuity by simply changing the contents of the M-register. However, practical DDS systems first require the execution of a serial, or byte-loading sequence to get the new frequency word into an internal buffer register which precedes the parallel-output M-register. This is done to minimize package pin count. After the new word is loaded...
into the buffer register, the parallel-output delta phase register is clocked, thereby changing all the bits simultaneously. The number of clock cycles required to load the delta-phase buffer register determines the maximum rate at which the output frequency can be changed.

**ALIASING IN DDS SYSTEMS**

There is one important limitation to the range of output frequencies that can be generated from the simple DDS system. The Nyquist Criteria states that the clock frequency (sample rate) must be at least twice the output frequency. Practical limitations restrict the actual highest output frequency to about 1/3 the clock frequency. Figure 6.5 shows the output of a DAC in a DDS system where the output frequency is 30MHz and the clock frequency is 100MHz. An antialiasing filter must follow the reconstruction DAC to remove the lower image frequency (100–30=70MHz) as shown in the figure.

**ALIASING IN A DDS SYSTEM**

![Graph showing Aliasing in a DDS System](image)

Note that the amplitude response of the DAC output (before filtering) follows a \( \sin(x)/x \) response with zeros at the clock frequency and multiples thereof. The exact equation for the normalized output amplitude, \( A(f_o) \), is given by:

\[
A(f_o) = \frac{\sin \left( \frac{\pi f_o}{f_c} \right)}{\frac{\pi f_o}{f_c}},
\]

where \( f_o \) is the output frequency and \( f_c \) is the clock frequency.
This rolloff is because the DAC output is not a series of zero-width impulses (as in a perfect re-sampler), but a series of rectangular pulses whose width is equal to the reciprocal of the update rate. The amplitude of the \( \text{sin}(x)/x \) response is down 3.92dB at the Nyquist frequency (1/2 the DAC update rate). In practice, the transfer function of the antialiasing filter is designed to compensate for the \( \text{sin}(x)/x \) rolloff so that the overall frequency response is relatively flat up to the maximum output DAC frequency (generally 1/3 the update rate).

Another important consideration is that, unlike a PLL-based system, the higher order harmonics of the fundamental output frequency in a DDS system will fold back into the baseband because of aliasing. These harmonics cannot be removed by the antialiasing filter. For instance, if the clock frequency is 100MHz, and the output frequency is 30MHz, the second harmonic of the 30MHz output signal appears at 60MHz (out of band), but also at 100–60=40MHz (the aliased component. Similarly, the third harmonic (90MHz) appears in band at 100–90=10MHz, and the fourth at 120–100MHz=20MHz. Higher order harmonics also fall within the Nyquist bandwidth (DC to \( f_c/2 \)). The location of the first four harmonics is shown in the diagram.

**125MSPS DDS SYSTEM (AD9850)**

The AD9850 125MSPS DDS system (Figure 6.6) uses a 32-bit phase accumulator which is truncated to 14-bits (MSBs) before being passed to the lookup table. The final digital output is 10-bits to the internal DAC. The AD9850 allows the output phase to be modulated using an additional register and an adder placed between the output of the phase accumulator register and the input to the lookup table. The AD9850 uses a 5-bit word to control the phase which allows shifting the phase in increments of 180°, 90°, 45°, 22.5°, 11.25°, and any combination thereof. The device also contains an internal high speed comparator which can be configured to accept the (externally) filtered output of the DAC to generate a low-jitter output pulse suitable for driving the sampling clock input of an ADC. The full scale output current can be adjusted from 10 to 20mA using a single external resistor, and the output voltage compliance is +1V. Key specifications are summarized in Figure 6.7.
AD9850 CMOS 125MSPS DDS/DAC SYNTHESIZER

AD9850 DDS/DAC SYNTHESIZER KEY SPECIFICATIONS

- 125MSPS Clock Rate
- On-Chip 10-bit DAC and High Speed Comparator
- DAC SFDR > 50dBc @ 40MHz Output
- 32-bit Frequency Tuning
- 5-bit Phase Modulation
- Simplified Control Interface: Byte-Parallel or Serial Load
- +5V or +3.3V Supplies
- 380mW Dissipation @ 125MSPS on +5V Supply (30mW Power-Down Mode)
- 28-Pin Shrink Small Outline Package (SSOP)

The frequency tuning (delta-phase register input word) and phase modulation words are loaded into the AD9850 via a parallel or serial loading format. The parallel load
format consists of five consecutive loads of an 8-bit control word (byte). The first 8-bit byte controls phase modulation (5-bits), power-down enable (1-bit), and loading format (2-bits). Bytes 2-5 comprise the 32-bit frequency tuning word. The maximum control register update frequency is 23MHz. Serial loading of the AD9850 is accomplished via a 40-bit serial data stream on a single pin. Maximum update rate of the control register in the serial-load mode is 3MHz.

The AD9850 consumes only 380mW of power on a single +5V supply at a maximum 125MSPS clock rate. The device is available in a 28-pin surface mount SSOP (Shrink Small Outline Package).

**DDS SYSTEMS AS ADC CLOCK DRIVERS**

DDS systems such as the AD9850 provide an excellent method of generating the sampling clock to the ADC, especially when the ADC sampling frequency must be under software control and locked to the system clock (see Figure 6.8). The true DAC output current $I_{out}$, drives a 200Ω, 42MHz lowpass filter which is source and load terminated, thereby making the equivalent load 100Ω. The filter removes spurious frequency components above 42MHz. The filtered output drives one input of the AD9850 internal comparator. The complementary DAC output current drives a 100Ω load. The output of the 100kΩ resistor divider placed between the two outputs is decoupled and generates the reference voltage for the internal comparator.

The comparator output has a 2ns rise and fall time and generates a TTL/CMOS-compatible square wave. The jitter of the comparator output edges is less than 20ps rms. True and complementary outputs are available if required.

In the circuit shown (Figure 6.8), the total output rms jitter for a 40MSPS ADC clock is 50ps rms, and the resulting degradation in SNR must be considered in wide dynamic range applications.
6.8

AMPLITUDE MODULATION IN A DDS SYSTEM

Amplitude modulation in a DDS system can be accomplished by placing a digital multiplier between the lookup table and the DAC input as shown in Figure 6.9. Another method to modulate the DAC output amplitude is to vary the reference voltage to the DAC. In the case of the AD9850, the bandwidth of the internal reference control amplifier is approximately 1MHz. This method is useful for relatively small output amplitude changes as long as the output signal does not exceed the +1V compliance specification.
The AD9830/9831 CMOS DDS systems (see Figure 6.10) contain two frequency registers and four phase registers thereby allowing both frequency and phase modulation. The registers are loaded through a parallel microprocessor port. The DDS chips contain a 32-bit phase accumulator register, 12-bit sin ROM lookup table, and a 10-bit DAC. The AD9830 operates at 50MSPS and dissipates 250mW on the +5V supply. The AD9831 operates at 25MSPS and dissipates 150mW on a +5V supply and 35mW on +3V. Key specifications for the devices are summarized in Figure 6.11.

AD9830/9831, 50/25MSPS COMPLETE DDS SYSTEMS
AD9830/9831 DDS SYSTEMS KEY SPECIFICATIONS

- 50MSPS (AD9830), 25MSPS (AD9831) Update Rate
- Single +5V (AD9830), +5V/+3V (AD9831) Supply
- 32-bit Phase Accumulator, 12-bit Address Sine ROM
- On Chip 10-bit DAC (70dB SFDR)
- Two On-Chip Frequency Modulation Registers
- Four On-Chip Phase Modulation Registers
- On-Chip Reference
- Power Dissipation: 250mW (AD9830), 150mW (AD9831 @ +5V), 35mW (AD9831 @ +3V)
- 48-pin TQFP
SPURIOUS FREE DYNAMIC RANGE CONSIDERATIONS IN DDS SYSTEMS

In many DDS applications, the spectral purity of the DAC output is of primary concern. Unfortunately, the measurement, prediction, and analysis of this performance is complicated by a number of interacting factors.

Even an ideal N-bit DAC will produce harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. This is because the spectral content of the DAC quantization noise varies as this ratio varies, even though its theoretical rms value remains equal to $q/\sqrt{12}$ (where $q$ is the weight of the LSB). The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is simply not true in a DDS system (it is more apt to be a true assumption in an ADC-based system, because the ADC adds a certain amount of noise to the signal which tends to "dither" or randomize the quantization error. However, a certain amount of correlation still exists). For instance, if the DAC output frequency is set to an exact submultiple of the clock frequency, then the quantization noise will be concentrated at multiples of the output frequency, i.e., it is highly signal dependent. If the output frequency is slightly offset, however, the quantization noise will become more random, thereby giving an improvement in the effective SFDR.

This is illustrated in Figure 6.12, where a 4096 point FFT is calculated based on digitally generated data from an ideal 12-bit DAC. In the left-hand diagram, the ratio between the clock frequency and the output frequency was chosen to be exactly 32 (128 cycles of the sinewave in the FFT record length), yielding an SFDR of about 78dBc. In the right-hand diagram, the ratio was changed to 32.25196850394 (127 cycles of the sinewave within the FFT record length), and the effective SFDR is now increased to 92dBc. In this ideal case, we observed a change in SFDR of 14dB just by slightly changing the frequency ratio.
EFFECT OF RATIO OF CLOCK TO OUTPUT FREQUENCY ON THEORETICAL 12-BIT DAC SFDR USING 4096-POINT FFT

Best SFDR can therefore be obtained by the careful selection of the clock and output frequencies. However, in some applications, this may not be possible. In ADC-based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system as shown in Figure 6.13 (Reference 5). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about 1/2 LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that dithering is not required.
A non-ideal DAC will introduce several other mechanisms of distortion. First, the overall integral non-linearity of the DAC transfer function will introduce harmonic distortion. This distortion behaves much like that produced by the non-linearity of an amplifier. The distortion due to the differential non-linearity of the DAC is highly dependent upon the nature of the differential non-linearity and is difficult to predict mathematically. The third source of DAC distortion are code-dependent output glitches. In a DAC there is a transient (or glitch) produced whenever the DAC input code changes. This glitch is usually worst at mid-scale, where the DAC makes the transition between the codes 1000...000 and 0111...111, and all the DAC bits must switch. These glitches occur because of the unequal turn-on/turn-off times of the DAC current switches. They also occur at 1/4 scale, 1/8 scale, etc., with decreasing amplitude. Because the glitches are code-dependent (hence signal-dependent) they produce harmonics of the fundamental output DAC frequency. For instance, each time the sinewave crosses through mid-scale, a glitch occurs, thereby producing a second harmonic - since the sinewave passes through midscale twice each cycle. The harmonics produced by these code-dependent glitches fold back into the Nyquist bandwidth due to aliasing and thereby affect the SFDR.

**CONTRIBUTORS TO DDS DAC DISTORTION**

- Resolution
- Integral Non-Linearity
- Differential Non-Linearity
- Code-Dependent Glitches
- Ratio of Clock Frequency to Output Frequency
Low distortion high-speed DACs generally have a specification for the area of the worst glitch (called *glitch impulse area*). In general, the smaller the glitch area, the better the distortion—but it is difficult to mathematically relate the distortion performance to the glitch area. The glitch impulse area for low distortion DACs is usually less than 30pV-sec. A typical midscale glitch impulse is shown for the AD9721 DAC in Figure 6.15.

The best way to measure DAC performance is with a spectrum analyzer, with a DDS system used to drive the DAC (Figure 6.16). Because there are nearly an infinite combination of possible clock and output frequencies, SFDR is generally specified for only a few selected combinations. One method is to plot the SFDR as a function of clock frequency for the output frequency slightly offset from 1/3 or 1/4 the clock frequency. The small frequency offset randomizes the quantization noise and also allows the distortion products to be easily observed.
Note that for the output slightly offset from $f_c/3$, the even harmonics will be aliased very close to the output signal as shown in Figure 6.17. Similarly, for the output slightly offset from $f_c/4$, the odd harmonics will fall close to the output frequency (Figure 6.18). The SFDR at $f_c/3$ is usually considered a worse case condition and is often plotted as a function of clock frequency as shown in Figure 6.19 for the AD9721 10-bit, 100MSPS TTL-compatible DAC.
LOCATION OF EVEN HARMONICS FOR
\[ f_0 = \frac{f_c}{3} - \Delta f \]

LOCATION OF ODD HARMONICS FOR
\[ f_0 = \frac{f_c}{4} - \Delta f \]
HIGH SPEED LOW DISTORTION DAC ARCHITECTURES

Because of the emphasis in communications systems for DDS DACs with high SFDR, much effort has been placed on determining optimum DAC architectures. Practically all low distortion high speed DACs make use of some form of non-saturating current-mode switching. A straight binary DAC with one current switch per bit produces code-dependent glitches as discussed above and is certainly not the most optimum architecture (Figure 6.20). A DAC with one current source per code level can be shown not to have code-dependent glitches, but it is not practical to implement for high resolutions. However, this performance can be approached by decoding the first few MSBs into a "thermometer" code and have one current switch per level. For example, a 5-bit thermometer DAC would have an architecture similar to that shown in Figure 6.21.
The input binary word is latched and then decoded into 31 outputs which drive a second latch. The output of the second latch drives 31 equally weighted current switches whose outputs are summed together. This scheme effectively removes nearly all the code-dependence of the output glitch. The residual glitch that does occur at the output is equal regardless of the output code change and can be filtered.
The distortion mechanisms associated with the full-decoded architecture are primarily asymmetrical output slewing, finite switch turn-on and turn-off times, and integral nonlinearity.

The obvious disadvantage of this type of thermometer DAC is the large number of latches and switches required to make a 12, 10, or even 8-bit DAC. However, if this technique is used on the 5 MSBs of an 8, 10, or 12-bit DAC, a significant reduction in the code-dependent glitch is possible. This process is called *segmentation* and is quite common in low distortion DACs.

Figure 6.22 shows a scheme whereby the first 5 bits of a 10-bit DAC are decoded as described above and drive 31 equally weighted switches. The last 5 bits are derived from binarily weighted current sources. Equally weighted current sources driving an R/2R resistor ladder could be used to derive the LSBs, however, this approach requires thin film resistors which are not generally available on a low-cost CMOS process. Also, the use of R/2R networks lowers the DAC output impedance, thereby requiring more drive current to develop the same voltage across a fixed load resistance.

![10-BIT SEGMENTED DAC](image)

The AD9850 internal 10-bit DAC uses two major stages of segmentation as shown in Figure 6.23. The first 5 bits (MSBs) are fully decoded and drive 31 equally weighted current switches (320µA each). The next 4 bits are decoded into 15 lines which drive 15 current switches, each supplying 20µA (1/16 the current supplied by each MSB switch). The LSB is latched and drives a single current switch which supplies 10µA (1/32 the current supplied by each MSB switch). A total of 47 current switches and latches are required to implement this architecture.
The basic current switching cell is made up of a differential PMOS transistor pair as shown in Figure 6.24. The differential pairs are driven with low-level logic to minimize switching transients and time skew. The DAC outputs are symmetrical differential currents which help to minimize even-order distortion products (especially which driving a differential output such as a transformer or an op amp differential I/V converter).

The overall architecture of the AD9850 is an excellent tradeoff between power/performance and allows the entire DDS function to be implemented on a standard CMOS process with no thin film resistors. Single-supply operation on +3.3V or +5V makes the device extremely attractive for portable and low power applications. The SFDR performance is typically 60, 55, and 45dBc for output frequencies of 1, 20, and 40MHz, respectively (clock frequency = 125MSPS).
The AD9760 (10-bit), AD9762 (12-bit) and AD9764 (14-bit) 100MSPS DACs utilize the same basic switching core as the AD9850. This family of DACs is pin-compatible, and offers exceptional AC and DC performance. They operate on single +5V or +3V supplies and contain on-chip latches, reference, and are ideal for the transmit channel in wireless basestations, ADSL/HFC modems, and DDS applications. Key specifications for the family are summarized in Figure 6.25.

### AD9760/9762/9764 FAMILY OF 100MSPS DACs

- Pin-Compatible 10-bit (AD9760), 12-bit (AD9762), and 14-bit (AD9764)
- SFDR for 15MHz Output: -60dBc
- Low Glitch Impulse: 5pVsec
- On-Chip Reference
- Single +5V or +3V Supplies
- Power Dissipation: 175mW @ 5V
- Power-Down Mode: 30mW
**IMPROVING SFDR USING SAMPLE-AND-HOLD DEGLITCHERS**

High-speed sample-and-hold amplifiers (such as the AD9100 and AD9101) can be used to deglitch DAC outputs as shown in Figure 6.26. Just prior to latching new data into the DAC, the SHA is put into the *hold* mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the clock frequency and hence are easily filtered. However, great care must be taken so that the relative timing between the SHA clock and the DAC update clock is optimum. In addition, the distortion performance of the SHA must be at least 6 to 10dB better than the DAC, or no improvement in SFDR will be realized. Achieving good results using an external SHA deglitcher becomes increasingly more difficult as clock frequencies approach 100MSPS.

**SAMPLE-AND-HOLD (SHA) USED AS DAC DEGLITCHER**

The AD6742 is a 12-bit, 65MSPS low distortion DAC with on-chip SHA deglitcher designed for communications applications. This DAC is fabricated on the XFCB process and provides 75dB SFDR for a 20MHz output. A functional diagram is shown in Figure 6.27, and key specifications in Figure 6.28.

**AD6742 12-BIT, 65MSPS DEGLITCHED DAC**
AD6742 12-BIT, 65MSPS DAC KEY SPECIFICATIONS

- 12-bit, 65MSPS Communications DAC
- Ideal for Wideband Multichannel Transmit Path
- High SFDR: 78dB (typ) @ 20MHz Output, 65MSPS Update
- Fabricated on XFCB process
- On-Chip Reference
- Dual 5V Supplies, 900mW power dissipation

HIGH SPEED INTERPOLATING DACs

Consider a DDS system which operates at a clock frequency of 100MSPS and outputs a 30MHz sinewave (see Figure 6.29). The first aliased (or image) frequency occurs at 100–30 = 70MHz. Assume we wish the antialiasing filter to attenuate this image frequency component by 60dB. The filter must go from a passband of 30MHz to 60dB stopband attenuation over the transition band lying between 30 and 70MHz (approximately one octave). A Butterworth filter design gives 6dB attenuation per octave for each pole. Therefore, a minimum of 10 poles is required to provide the desired attenuation. Filters become even more complex as the transition band becomes narrower.
In ADC-based systems, oversampling can ease the requirements on the antialiasing filter, and a sigma-delta ADC has this inherent advantage. In a DAC-based system (such as DDS), the concept of interpolation can be used in a similar manner. This concept is common in digital audio CD players, where the basic update rate of the data from the CD is about 44kSPS. "Zeros" are inserted into the parallel data, thereby increasing the effective update rate to 4-times, 8-times, or 16-times the fundamental throughput rate. The 4x, 8x, or 16x data stream is passed through a digital interpolation filter which generates the extra data points. The high oversampling rate moves the image frequencies higher, thereby allowing a less complex filter with a wider transition band.

The same concept can be applied to a high speed DDS DAC. Assume a traditional DAC is driven at an input word rate of 30MSPS (see Figure 6.30). The maximum realizable DAC output frequency is about 10MHz. The image frequency component at 30–10 = 20MHz must be attenuated by the analog antialiasing filter, and the transition band of the filter is 10 to 20MHz.

Assume that we increase the update rate to 60MSPS by inserting a "zero" between each original data sample. The parallel data stream is now 60MSPS and is passed through the digital interpolation filter which computes the additional data points. The response of the digital filter relative to the 2-times oversampling frequency is shown in Figure 6.30. The analog antialiasing filter transition zone is now 10 to 50MHz (the first image occurs at $2f_c-f_o=60-10=50$MHz).
The AD977x is a 4-times oversampling interpolating 10-bit DAC, and a simplified block diagram is shown in Figure 6.31. The device is designed to handle 10-bit input word rates up to about 30MSPS. The internal digital filter consists of a 15-tap filter operating at 2fc followed by a 7-tap filter operating at 4fc. The output word rate is 120MSPS, putting the image frequency at 4fc−fo=120−10=110MHz. SFDR of the DAC for a 10MHz output is approximately 60dBc.
The AD9853 is a digital Quadrature Phase Shift Keying (QPSK) modulator useful in the 5 to 40MHz return path transmitter in a hybrid fiber coax (HFC) CATV cable modem application (see Figure 6.32). This allows asynchronous data transfer over the HFC cable plant. The device takes the serial QPSK data input, splits it into an in-phase (I) and quadrature (Q) signal. The I and Q channel data is then filtered and passed through a digital quadrature modulator. The quadrature modulators are driven by the sine and cosine outputs from the DDS section. The modulator outputs are then recombined digitally and then converted into analog by an internal 10-bit DAC. The resulting QPSK constellation is shown in Figure 6.33. This scheme of modulation is quite common, and results in relatively high noise immunity. Key specifications for the AD9853 are given in Figure 6.34.
AD9853 DIGITAL QPSK MODULATOR

QPSK CONSTELLATION

AD9853 DIGITAL QPSK MODULATOR KEY SPECIFICATIONS
- Performs Transmit Function for QPSK 5-40MHz Hybrid Fiber Coax (HFC) Return Path
- Includes Raised Cosine Pulse-Shaping Filter (Alpha = 0.5) and Interpolation Filters
- 140MSPS Clock Frequency
- 46dBc SFDR @ 40MHz Output
- +5V or +3.3V Operation
- 300mW Dissipation @ 125MSPS Clock Frequency (30mW Power-Down Mode)
- 28-Pin SSOP Surface-Mount Package
REFERENCES


SECTION 7

HIGH SPEED HARDWARE DESIGN TECHNIQUES
Walt Kester, James Bryant, Walt Jung, Adolfo Garcia, John McDonald, Joe Buxton

ANALOG CIRCUIT SIMULATION
Walt Kester, Joe Buxton

In recent years there has been much pressure placed on system designers to verify their designs with computer simulations before committing to actual printed circuit board layouts and hardware. Simulating complex digital designs is extremely beneficial, and very often, the prototype phase can be eliminated entirely. However, bypassing the prototype phase in high-speed/high-performance analog or mixed-signal circuit designs can be risky for a number of reasons.

For the purposes of this discussion, an analog circuit is any circuit which uses ICs such as op amps, instrumentation amps, programmable gain amps (PGAs), voltage controlled amps (VCAs), log amps, mixers, analog multipliers, etc. A mixed-signal circuit is an A/D converter (ADC), D/A converter (DAC), or combinations of these in conjunction with some amount of digital signal processing which may or may not be on the same IC as the converters.

Consider a typical IC operational amplifier. It may contain some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE (Simulation Program with Integrated Circuit Emphasis, see Reference 1) model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the various junctions in the op-amp chip. For high-speed ICs, the package and wirebond parasitics may also be included. This is the type of model that the IC designer uses to optimize the device during the design phase and is typically run on a CAD workstation. Because it is a detailed model, it will be referred to as a micromodel. In simulations, such a model will behave very much like the actual op-amp, but not exactly.

The IC designer uses transistor and other device models based on the actual process upon which the component is fabricated. Semiconductor manufacturers invest considerable time and money developing and refining these device models so that the IC designers can have a high degree of confidence that the first silicon will work and that mask changes (costing additional time and money) required for the final manufactured product are minimized.

However, these device models are not published, neither are the IC micromodels, as they contain proprietary information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing several ICs (each represented by its own micromodel) to reach a useful result. SPICE micromodels of analog ICs often
fail to converge (especially under transient conditions), and multiple IC circuits make this a greater possibility.

For these reasons, the SPICE models of analog circuits published by manufacturers or software companies are *macromodels* (as opposed to *micromodels*), which simulate the major features of the component, but lack fine detail. Most manufacturers of linear ICs (including Analog Devices) provide these macromodels for components such as operational amplifiers, analog multipliers, references, etc. (Reference 2 and 3). These models represent *approximations* to the actual circuit, and parasitic effects such as package capacitance and inductance and PC board layout are rarely included. The models are designed to work with various versions of SPICE simulation programs such as PSpice® (Reference 4) and run on workstations or personal computers. The models are simple enough so that circuits using multiple ICs can be simulated in a reasonable amount of computation time and with good certainty of convergence. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally using a carefully built prototype.

Finally, there are mixed-signal ICs such as A/D and D/A converters which have no SPICE models, or if they exist, the models do not simulate dynamic performance (Signal-to-noise, effective bits, etc.), and prototypes of circuits using them should always be built.

### SPICE SIMULATIONS: MACROMODEL OR MICROMODEL?

<table>
<thead>
<tr>
<th>METHODOLOGY</th>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
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<tr>
<td><strong>MACROMODEL</strong></td>
<td>Ideal Elements</td>
<td>Fast Simulation Time, Easy to Modify</td>
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<tr>
<td>Model the Device Behavior</td>
<td></td>
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<tr>
<td><strong>MICROMODEL</strong></td>
<td>Fully Characterized Transistor Level</td>
<td>Most Complete Model</td>
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The ADSpice Model

The ADSpice model was developed to advance the state-of-the-art in op amp macromodelling and provide a tool for designers to simulate accurately their circuits. Previously, the dominant model architecture was the Boyle model (Reference 3). However, this model was developed over 20 years ago and does not accurately model many of today's higher speed amplifiers. The primary reason for this is that the Boyle model has only two frequency shaping poles and no zeroes. In contrast, the
ADSpice model has an open architecture that allows for unlimited poles and zeroes, leading to much more accurate AC and transient responses.

The ADSpice model is comprised of three main portions: the input and gain stage, the pole/zero stages, and the output stage. The input stage shown in Figure 7.2 uses the only two transistors in the entire model. These are needed to model properly an op amp’s differential input stage characteristics. Although the example here uses NPN transistors, the input stage can easily be modified to include PNP, JFET, or CMOS devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

**ADSpice INPUT AND GAIN STAGE MODEL**

An example of a controlled source is $gm_1$ in the gain stage, which is a voltage controlled current source. It senses the differential collector voltage from the input stage and converts that to a current. When the current flows through $R_7$, a single-ended voltage is produced. By making the product of $gm_1$ and $R_7$ equal to the open loop gain, the entire open-loop gain is produced in the gain stage, which means that all other stages are set to unity gain. This leads to significant flexibility in adding and deleting stages.

Following the gain stage are an unlimited number of pole/zero stages and their combinations. The typical topology of these stages is shown in Figure 7.3, which is similar to the gain stage. The main difference is that now the product of $gm_2$ times $R_8$ is equal to unity. The pole or zero frequency is set by the parallel combination of the resistor and capacitor, $R_8-C_4$ for the pole and $R_g-C_5$ for the zero. Because these stages are unity gain, any number of them can be added or deleted without affecting the low frequency response of the model. Instead, the high frequency gain and phase response can be tailored to match accurately the actual amplifier’s response. The benefits are especially apparent in closed loop pulse response and stability analysis.
The output stage in Figure 7.4 not only models the open loop output impedance at DC but with the inclusion of an inductor also models the rise in impedance at high frequencies. Additionally, the output current is correctly reflected in the supply currents. This is a significant improvement over the Boyle model because now the power consumption of the circuit under load can be analyzed accurately. Furthermore, circuits that use the supply currents for feedback can also be simulated.
As an illustration of using the ADSpice model to predict circuit performance, the AD847 op amp (50MHz unity gain-bandwidth product) output was loaded in a 65pF capacitor and the response measured (both in ADSpice and in the circuit). The results shown in Figure 7.5 illustrate good correlation between the simulated and the actual response. As an additional example, extra parasitic capacitances were added as shown in Figure 7.6, and the simulated and actual responses compared. Again, note the excellent general agreement.
AD847 PULSE RESPONSE

Properly laid out PC board and simulation agree closely

PC BOARD PARASITICS WILL ALTER THE RESULTS

- Parasitic capacitances worsen the circuit's response
- Properly modelling the parasitics in SPICE yields good results

Other Features of ADSpice Models

In addition to offering models of op amps (both voltage and current feedback), which allow simulation of AC and DC performance, Analog Devices has included noise in many of its amplifier models. The capability to model a circuit’s noise performance in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A
complete analysis is a very involved and tedious task which requires calculating all
the individual noise contributors and reflecting them to the input or output. The
procedure is further complicated by the fact that noise gain is generally a function of
frequency and can significantly affect results if not carefully considered.

To greatly simplify this task, the ADSpice model was enhanced to include noise
generators which accurately predict the broadband and 1/f noise of the actual
amplifier. Noise is currently modeled in a number of ADI op amps, variable gain
amplifiers, and voltage references. For further discussion on the noise model details,
see Reference 2.

In addition to amplifiers, ADSpice models exist for instrumentation amplifiers,
analog multipliers, voltage references, analog switches, multiplexers, matched
transistors, and buffers. A complete set of ADSpice models is available from Analog
Devices upon request.

ADSpice will give good approximations to actual performance, if used correctly.
However, the user must include the external components and parasitics which may
affect the device performance in the circuit. This becomes a difficult task at
frequencies much above 100MHz, and caution must be used in interpreting the
simulation results. There is no substitute for prototyping at these frequencies.

While pulse and frequency response can be successfully simulated using the
ADSpice models, distortion performance cannot be predicted since non-linear effects
are not included in the models. As mentioned previously, models for ADCs and DACs
are not available due to the difficulty in modeling their AC performance.

**SUMMARY: ADSpice FEATURES**

- Transistor-Level Input Stage Model
- Unlimited Poles and Zeros
- Noise is Included in Some Models
- Distortion is not Modeled
- Over 500 Models Exist for:
  - Amplifiers
  - Instrumentation Amplifiers
  - Analog Multipliers
  - Voltage References
  - VCAs
  - Multiplexers and Switches
- But There is no Substitute for a Good Prototype!!
The basic principle of a breadboard or prototype is that it is a temporary structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial prototyping systems, but almost all of them are designed to facilitate the prototyping of digital systems, where noise immunities are hundreds of millivolts or more. Non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems are, without exception, unsuitable for high performance or high frequency analog prototyping because their resistance, inductance, and capacitance are too high. Even the use of standard IC sockets is inadvisable in many prototyping applications.

An important consideration in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between high-speed and high-precision mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100kSPS. Successful prototyping of these circuits requires that equal attention be given to good high-speed and high-precision circuit techniques.

The simplest technique for analog prototyping uses a solid copper-clad board as a ground plane (Reference 5 and 6). The ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as deadbug prototyping because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 7.8 shows a hand-wired breadboard using two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not
taken, however, this may result in unexpected ground loops between the two sides of
the board, especially at RF frequencies.

"DEADBUG" PROTOTYPE

Pieces of copper-clad board may be soldered at right angles to the main ground
plane to provide screening, or circuitry may be constructed on both sides of the board
(with connections through holes) with the board itself providing screening. In this
case, the board will need standoffs at the corners to protect the components on the
underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air
(a type of construction strongly advocated by Robert A. Pease of National
Semiconductor (Reference 6) and sometimes known as "bird's nest" construction)
there is always the risk of the circuitry being crushed and resulting short-circuits.
Also, if the circuitry rises high above the ground plane, the screening effect of the
ground plane is diminished, and interaction between different parts of the circuit is
more likely. Nevertheless, the technique is very practical and widely used because
the circuit may easily be modified (assuming the person doing the modifications is
adapts at using a soldering iron, solder-wick, and a solder-sucker).

Another prototype breadboard is shown in Figure 7.9. The single-sided copper-clad
board has pre-drilled holes on 0.1" centers (Reference 7). Power busses are at the top
and bottom of the board. The decoupling capacitors are used on the power pins of
each IC. Because of the loss of copper area due to the pre-drilled holes, this
technique does not provide as low a ground impedance as a completely covered
copper-clad board.
In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each hole used for a via must be drilled out to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (Reference 8).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50Ω, 60Ω, 75Ω or 100Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned
copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors. A few of the many types of Solder-Mount building-block components are shown in Figure 7.10.

![SAMPLES OF "SOLDER-MOUNT" COMPONENTS](image)

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PC board, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Figure 7.11 shows an example of a 2.5GHz phase-locked-loop prototype built with Solder-Mount. This is a high speed circuit, but the technique is equally suitable for the construction of high resolution low frequency analog circuitry. A particularly convenient feature of Solder-Mount at VHF is the ease with which it is possible to make a transmission line.

"SOLDER-MOUNT" PROTOTYPE
If a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50Ω, 60Ω, 75Ω, and 100Ω). These strips may be used as transmission lines, for impedance matching, or simply as power buses. (Glass fiber/epoxy PCB is somewhat lossy at VHF and UHF, but the losses will probably be tolerable if microstrip runs are short.)

Both the "deadbug" and the "Solder-Mount" prototyping techniques become somewhat tedious for complex analog or mixed-signal circuits. Larger circuits are often better prototyped using more formal layout techniques.

An approach to prototyping more complex analog circuits is to actually lay out a double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (Reference 9). Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their desired positions, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (Reference 10). These systems produce single and double-sided circuit boards directly by drilling all holes and using a milling technique to remove copper and create insulation paths and finally, the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there is no
"plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils. An example of such a prototype board is shown in Figure 7.12 (top view) and Figure 7.13 (bottom view).
IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even low-profile sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used in high speed circuits, an IC socket made of individual pin sockets (sometimes called cage jacks) mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board). Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections between them (see Figure 7.14).

The spring-loaded gold-plated contacts within the pin socket makes good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket. The uncapped versions allow the IC pins to extend out the bottom of the socket. After the prototype is functional and no further changes are to be made, the IC pins can be soldered directly to the bottom of the socket, thereby making a permanent and rugged connection.

**PIN SOCKETS (CAGE JACKS) HAVE MINIMUM PARASITIC RESISTANCE, INDUCTANCE, AND CAPACITANCE**

The prototyping techniques discussed so far have been limited to single or double-sided PC boards. Multilayer PC boards do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high
frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1pF) between the prototype and the final board may cause subtle differences in bandwidth and settling time. Oftentimes prototyping is done with DIP packages, when the final production package is an SOIC. This can account for differences between prototype and final PC board performance.

**EVALUATION BOARDS**

*Walt Kester*

Most manufacturers of analog ICs provide evaluation boards (usually at a nominal cost) which allow customers to evaluate products without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. The artwork or CAD file is usually made available free of charge, should the customer wish to copy the layout directly or make modifications to suit the application.

Figure 7.15 shows the schematic for the AD8001 (SOIC package) 800MHz op amp evaluation board. Figures 7.16 and 7.17, respectively, show the top and bottom side of the PCB. The amplifier is connected in the non-inverting mode. The top side (Figure 7.16) shows the top side of the SOIC package along with input and output SMA connectors. Notice that the ground plane is cut away around the SOIC in order to minimize parasitic capacitance. The bottom side of the board (Figure 7.17) shows the surface mount resistors and capacitors which comprise the op amp gain-setting and power supply decoupling circuits, respectively.
AD8001AR (SOIC) 800MHz OP AMP: NON-INVERTING MODE EVALUATION BOARD SCHEMATIC

AD8001AR (SOIC) EVALUATION BOARD - TOP VIEW

AD8001AR (SOIC) EVALUATION BOARD - BOTTOM VIEW
In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents, in turn, produce corresponding voltages across any parasitic impedance which may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output because of the op amp's finite power supply rejection at high frequencies.

A three-capacitor decoupling scheme was chosen for the AD8001 evaluation board to ensure a low impedance path to ground at all transient frequencies. The highest frequency transients are shunted to ground by the 1000pF and the 0.01µF ceramic capacitors. These are located as close to the power supply pins as possible to minimize any series inductance and resistance. Because the devices are surface mount, there is minimum stray inductance and resistance in the path to the ground plane. The lower frequency transient currents are shunted to ground by the 10µF tantalum capacitors.

The input and output signal traces are of the AD8001 evaluation board are 50Ω microstrip transmission lines. Notice that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points in order to maintain low impedance ground continuity at high frequencies.

Evaluation boards can range from relatively simple ones (op amps, for example) to rather complex ones for mixed-signal ICs such as A/D converters. ADC evaluation boards often have on-board memory and DSPs for analyzing the ADC performance. Software is often provided with these more complex evaluation boards so that they can interface with a personal computer to perform complex signal analysis such as histogram and FFT testing.
Complete evaluations of ADCs requires the use of FFTs to fully characterize the devices AC performance. A typical test setup is shown in Figure 7.18. The manufacturer's evaluation board is used as a means for interfacing to the ADC. The evaluation board is designed to allow easy access to the ADC inputs and outputs while also providing a good layout (including all necessary references, buffer amplifiers, and decoupling). The evaluation board allows the ADC output data to be captured on a parallel output connector. Most ADC evaluation boards contain an on-board DAC which can be used to check the functionality of the ADC, but is somewhat limited in performing meaningful AC testing. A block diagram of the AD9042 (12-bits, 41MSPS) evaluation board is shown in Figure 7.19, and a photo in Figure 7.20.

**TEST SETUP REQUIRED TO EVALUATE HIGH SPEED ADCs**

![Diagram of test setup](image)

1. LOW PHASE JITTER SINEWAVE SOURCE
2. BANDPASS FILTER
3. MEMORY OR LOGIC ANALYZER
4. PC
5. POWER SUPPLIES
6. CLOCK
7. PARALLEL OR SERIAL PORT
8. LOW PHASE JITTER SAMPLING CLOCK SOURCE
9. ADC ON EVALUATION BOARD

---

18
AD9042 12-BIT, 41MSPS ADC EVALUATION BOARD
FUNCTIONAL DIAGRAM

XTAL OSC 40.96MHz

EXTERNAL SAMPLING CLOCK

50Ω

60.4Ω

0.1µF

AD9042 ENCODE

ENCODE

74AC574 REGISTERS (2)

499Ω

499Ω

T1 - 1T MINICIRCUITS

50Ω

100Ω

74AS00

74AS00

CK

AD9042 EVALUATION BOARD - TOP VIEW

ANALOG DEVICES

7.19

7.20
The most complex part of the problem is usually designing the buffer memory module. A high speed logic analyzer is one method of capturing the ADC output data, and interfaces easily to the ADC evaluation board. Data from the logic analyzer can be loaded into a PC through either parallel or serial ports. Once the ADC data is inside the PC, software packages such as Mathcad can be used to perform the actual FFT.

Another alternative is to use a commercially-available data acquisition module that plugs directly into a card slot of the PC. These modules come complete with FFT and other ADC test software, but are not easily portable from one PC to another and are generally difficult to interface with laptop computers.

Although fast and relatively low power memories (FIFOs) are available commercially, designing a buffer memory, the interfaces to the ADC and the PC, and the necessary software can be a time-consuming project. Analog Devices has designed a simple 16-bit by 16k deep 100MHz memory board (3 x 4 inches) and the necessary software to allow high speed ADC evaluation boards to interface directly with the parallel printer port of most PCs. The core of the memory design is the IDT72265 16k by 18-bit wide FIFO or alternately, the IDT72255 is an 8k pin compatible device which may be substituted if the deeper memory is not required.

This FIFO chip features fully independent I/O ports that allow data to be loaded at up to 100MSPS and downloaded at the rate of a parallel printer port. Since the ports are independent, both can operate simultaneously, i.e., data may be read out while new data is being written. The chip takes care of all addressing, overhead and much of the hand-shaking for these operations. Included is circuitry that prevents unread data from being overwritten, eliminating the need for extensive write control circuitry.

A photograph of the Fifo Memory board is shown in Figure 7.21, and Figure 7.22 shows it connected to the AD9042 evaluation board.
Using this hardware and Windows-based software to capture the ADC data, many testing possibilities exist. Figure 7.23 shown a time-domain plot of data captured using the fifo memory. Once the data is captured, FFT analysis (Figure 7.24) or DNL histograms (Figure 7.25) are easily generated.

DATA CAPTURE PC OUTPUT DISPLAY
FFT OUTPUT

DNL HISTOGRAM
In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design and the simulation. The final PCB layout should be then be based on the prototype layout as much as possible.

Finally, evaluation boards can be extremely useful in evaluating new analog ICs, and allow designers to verify the IC performance with a minimum amount of effort. The layout of the components on the evaluation board can serve as a guide to both the prototype and the final PC board layout. Gerber files are generally available for all evaluation board layouts and may be obtained at no charge.
REFERENCES: SIMULATION, PROTOTYPING, AND EVALUATION BOARDS


4. PSpice® Simulation software. MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718, 714-770-3022


   Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

9. Schematic Capture and Layout Software:
   PADS Software, INC, 165 Forest St., Marlboro, MA, 01752 and ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121

10. Prototype Board Cutters:
    LPKF CAD/CAM Systems, Inc., 6190 Artic Dr, PO Box 6209, Beaverton, OR, 97005 and T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341


GROUNDING IN HIGH SPEED SYSTEMS

Walt Kester, James Bryant

The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially at high speeds. The ground plane not only acts as a low impedance return path for high frequency currents but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuits susceptibility to external EMI/RFI is also reduced.

All IC ground pins should be soldered directly to the ground plane to minimize series inductance. Power supply pins should be decoupled to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. Ferrite beads may be also required.

The ground plane allows the impedance of PCB traces to be controlled, and high frequency signals can be terminated in the characteristic impedance of the trace to minimize reflections when necessary.

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers and vias. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands." IC ground pins located in a ground "island" have no current return path to the ground plane.

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the mother card. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities: (1) The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. (2) The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is often used at very high frequencies and where the return currents are relatively constant. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. It is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

In other systems, especially high speed ones with large amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually desirable to use separate ground planes for the analog and the digital circuitry. On PCBs which have both analog and digital
cuits, there are two separate ground planes. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 7.26 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper brads for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged.

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog components and also grounded and decoupled to the analog ground plane. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 7.27 will help to explain this seeming dilemma.
Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 7.27 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C\text{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It’s the IC designer’s job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the analog ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name “DGND” on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout (they normally can’t by design). Minimizing the fanout on the converter’s digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic
supply pin (\(V_D\)) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 7.27. The internal digital currents of the converter will return to ground through the \(V_D\) pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 7.27) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

**POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS**

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (\(V_D\)), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious. The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

A low phase-noise crystal oscillator should be used to generate the ADC sampling clock, because sampling clock jitter modulates the input signal and raises the noise
and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

Ideally, the sampling clock generator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. If it is passed between its origin on the digital ground plane to the ADC on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential one using either a small RF transformer or a high speed differential driver and receiver as shown in Figure 7.29. The driver and receiver should be ECL to minimize phase jitter. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

**SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES**

![Diagram of sampling clock distribution](image)

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 7.30 shows a good layout for a data acquisition board.
where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

**A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING**

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board’s performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.
POWER SUPPLY NOISE REDUCTION AND FILTERING
Walt Jung and John McDonald

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers do have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the peak (or p-p) amplitudes of the switching spikes, with the output loading of your system.

The following section discusses filter techniques for rendering a noisy switcher output analog ready, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a source, a path, and a receptor [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 7.31. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small sized.

NOISE REDUCTION TOOLS
- Capacitors
- Inductors
Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; electrolytic, film, and ceramic. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 7.32.

### CAPACITOR SELECTION

<table>
<thead>
<tr>
<th></th>
<th>Aluminum Electrolytic (General Purpose)</th>
<th>Aluminum Electrolytic (Switching Type)</th>
<th>Tantalum Electrolytic</th>
<th>Polyester (Stacked Film)</th>
<th>Ceramic (Multilayer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>100 µF (1)</td>
<td>120 µF (1)</td>
<td>100 µF (1)</td>
<td>1 µF</td>
<td>0.1 µF</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>25 V</td>
<td>25 V</td>
<td>20 V</td>
<td>400 V</td>
<td>50 V</td>
</tr>
<tr>
<td>ESR</td>
<td>0.6 Ω @ 100 kHz</td>
<td>0.18 Ω @ 100 kHz</td>
<td>0.12 Ω @ 100 kHz</td>
<td>0.11 Ω @ 1 MHz</td>
<td>0.12 Ω @ 1 MHz</td>
</tr>
<tr>
<td>Operating Frequency (2)</td>
<td>≦ 100 kHz</td>
<td>≦ 500 kHz</td>
<td>≦ 1 MHz</td>
<td>≦ 10 MHz</td>
<td>≦ 1 GHz</td>
</tr>
</tbody>
</table>

(1) Types shown in Figure 7.33 data
(2) Upper frequency limit is strongly size and package dependent

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it
can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The **electrolytic** family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes **general purpose aluminum electrolytic** types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of µA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes **tantalum** types, generally limited to voltages of 100V or less, with capacitance of 500µF or less [Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the **switching** type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The **OS-CON** capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

**Film** capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10µF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the **stacked-film** type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of
dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

**Ceramic** is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several µF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1µF or less, with 0.01µF representing a more practical upper limit.

Multilayer ceramic “chip caps” are very popular for bypassing/filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency above the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor’s ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

Figure 7.33 illustrates the high frequency impedance characteristics of a number of electrolytic capacitor types, using nominal 100µF/20V samples. In these plots, the impedance, |Z|, vs. frequency over the 20Hz-200kHz range is displayed using a high resolution 4-terminal setup [Reference 8]. Shown in this display are performance samples for a 100µF/25V general purpose aluminum unit (top curve @ right), a 120µF/25V HFQ unit (next curve down @ right), a 100µF/20V tantalum bead type (next curve down @ right), and a 100µF/20V OS-CON unit (lowest curve @ right). While the HFQ and tantalum samples are close in 100kHz impedance, the
general purpose unit is about 4 times worse. The OS-CON unit is nearly an order of magnitude lower in 100kHz impedance than the tantalum and switching electrolytic types.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance. In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive (noted in Figure 7.33 by the 100Hz impedance). At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL (not shown). All electrolytics will display impedance curves similar in general shape. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

Regarding inductors, Ferrites (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 7.34 summarize a number ferrite characteristics.

**CHARACTERISTICS OF FERRITES**

- Good for frequencies above 25kHz
■ Many sizes and shapes available including leaded "resistor style"

■ Ferrite impedance at high frequencies is primarily resistive -- Ideal for HF filtering

■ Low DC loss: Resistance of wire passing through ferrite is very low

■ High saturation current

■ Low cost

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the bead of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite’s impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

**CHOOSING THE RIGHT FERRITE DEPENDS ON**

■ Source of Interference

■ Interference Frequency Range

■ Impedance Required at Interference Frequency

■ Environmental Conditions:

  Temperature, AC and DC Field Strength,
Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output so as to produce an analog ready 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a card entry filter providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

Figure 7.36 illustrates a card entry filter suitable for use with switching supplies. With a low rolloff point of 1.5kHz and mV level DC errors, it is effective for a wide variety of filter applications just as shown. This filter is a single stage LC low-pass filter covering the 1kHz to 1MHz range, using carefully chosen parts. Because of component losses, it begins to lose effectiveness above a few MHz, but is still able to achieve an attenuation approaching 60dB at 1MHz.

"CARD-ENTRY" SWITCHING SUPPLY FILTER

The key to low DC losses is the use of input choke, L1, a ferrite-core unit selected for a low DC resistance (DCR) of <0.25Ω at the 100µH inductance (either an axial lead
type 5250 or a radial style 6000-101K choke should give comparable results) [Reference 13]. These chokes have low inductance shift with a 300mA load current, and the low DCR allows the 300mA to be passed with no more than 75mV of DC error. Alternately, resistive filtering might be used in place of L1, but a basic tradeoff here is that load current capacity will be compromised for comparable DC errors. C1, a 100μF/20V tantalum type, provides the bulk of the capacitive filtering, shunted by a 1μF multilayer ceramic.

Figure 7.37 shows the frequency response of this filter in terms of SPICE simulation and lab measurements, with good agreement between the simulation and the measurements below 1MHz.

This type of filter does have some potential pitfalls, and one of them is the control of resonances. If the LCR circuit formed does not have sufficiently high resistance at the resonant frequency, amplitude peaking will result. This peaking can be minimized with resistance at two locations: in series with L1, or in series with C1+C2. Obviously, limited resistance is usable in series with L1, as this increases the DC errors.

In the filter, R1 is a damping resistor, used to control resonant peaks, and it should not be eliminated. A 1Ω value provides a slightly underdamped response, with peaking on the order of 1dB. Alternately, 1.5Ω can be used for less peaking, with a tradeoff of less attenuation below 1MHz. Note that for wide temperature range applications, all temperature sensitive filter components will need consideration.
A local high frequency filter useful with the card entry filter is shown in Figure 7.38. This simple filter can be considered an option, one which is exercised dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It uses Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, providing a resistance of more than $80\,\Omega$ at 10MHz, increasing to over $100\,\Omega$ at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a $0.1\mu F$ ceramic unit shown.

**HIGH FREQUENCY LOCALIZED DECOUPLING**

Both the card entry filter and the local high frequency decoupling filters are designed to filter differential-mode noise only, and use common, off the shelf components [Reference 14].

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

1. **Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits.** This minimizes ESR, and maximizes filter performance. Pick chokes for low $\Delta L$ at the rated DC current, as well as low DCR.

2. **Use short and wide PCB tracks to decrease voltage drops and minimize inductance.** Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.

3. **Use short leads or better yet, leadless components, to minimize lead inductance.** This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred.
(4) **Use a large-area ground plane for minimum impedance.**

(5) **Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not absolutely necessary, it does instill confidence in a design when correlation is achieved** (see Reference 15).

The discussion above assumes that the incoming AC power is relatively clean, an assumption not always valid. The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

*It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training!* All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment (see Figure 7.39). Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

**POWER LINE FILTERING IS ALSO IMPORTANT**

![Power Line Filter Diagram](image)

Power Line Filter Blocks EMI from Entering or Exiting Box Via Power Lines

Commercial power line filters can be quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections.
(black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).
REFERENCES: NOISE REDUCTION AND FILTERING


4. Type HFQ Aluminum Electrolytic Capacitor and type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

5. OS-CON Aluminum Electrolytic Capacitor 93/94 Technical Book, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, (501) 633-6634.


10. Fair-Rite Linear Ferrites Catalog, Fair-Rite Products, Box J, Wallkill, NY, 12886, (914) 895-2055.

11. Type EXCEL leaded ferrite bead EMI filter, and type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.


14. DIGI-KEY, PO Box 677, Thief River Falls, MN, 56701-0677, (800) 344-4539.

15. Tantalum Electrolytic Capacitor SPICE Models, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.

Many analog circuits require stable regulated voltages relatively close in potential to an unregulated source. An example would be a linear post regulator for a switching power supply, where voltage loss (dropout) is critical. This low dropout type of regulator is readily implemented with a rail-rail output op amp. The wide output swing and low saturation voltage enables outputs to come within a fraction of a volt of the source for medium current (<30mA) loads, such as reference applications. For higher output currents, the rail-rail voltage swing feature allows direct drive to low saturation voltage pass devices, such as power PNPs or P-channel MOSFETs. Op amps working from 3V up with the rail-rail features are most suitable here, providing power economy and maximum flexibility.

LOW DROPOUT REFERENCES

Basic references

Among the many problems in making stable DC voltage references work from 5V and lower supplies are quiescent power consumption, overall efficiency, the ability to operate down to 3V, low input/output (dropout) capability, and minimum noise output. Because low voltage supplies can’t support zeners of \( \approx 6V \), low voltage references must necessarily be bandgap based-- a basic \( \approx 1.2V \) potential. With low voltage systems, power conservation can be a critical issue with references, as can output DC precision.

For many applications, simple one-package fixed (or variable) voltage references with minimal external circuitry and high accuracy are attractive. Two unique features of the three terminal REF19X bandgap reference family are low power, and shutdown capability. The series allows fixed outputs from 2.048-5V to be controlled between ON and OFF, via a TTL/CMOS power control input. It provides precision reference quality for those popular voltages shown in Figure 7.40.
The REF19X family can be used as a simple three terminal fixed reference as per the table by tying pins 2 and 3 together, or as an ON/OFF controlled device, by programming pin 3 as noted. In addition to the shutdown capacity, the distinguishing functional features are a low dropout of 0.5V at 10mA, and a low current drain for both quiescent and shutdown states, 45 and 15μA (max.), respectively. For example, working from inputs in the range of 6.3 to 15V, a REF195 used as shown drives 5V loads at up to 30mA, with grade dependent tolerances of ±2 to ±5mV, and max TCs of 5 to 25ppm/°C. Other devices in the series provide comparable accuracy specifications, and all have low dropout features.

To maximize DC accuracy in this circuit, the output of U1 should be connected directly to the load with short heavy traces, to minimize IR drops. The common terminal (pin 4) is less critical due to lower current in this leg.

**Scaled References**

Another approach, one with the advantage of voltage flexibility, is to bufferSCALE a low voltage reference diode. With this approach, one difficulty is getting an amplifier to work well at 3V. A workhorse solution is the low power reference and scaling buffer shown in Figure 7.41. Here a low current 1.2V, two-terminal reference diode is used for D1, either the 1.235V AD589 or the 1.225V AD1580. Resistor R1 sets the diode current, chosen for 50μA at a minimum supply of 2.7V. Obviously, loading on the unbuffered diode must be minimized at the VREF node.
Amplifier U1 both buffers and optionally scales up the nominal 1.2V reference, allowing much higher source/sink currents. A higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach. Quiescent current is amplifier dependent, ranging from 45µA/channel with the OP196/296/496 series to 1000-2000µA/channel with the OP284 and OP279. The former series is most useful for very light loads (<2mA), while the latter series provide device dependent outputs up to 50mA. Various devices can be used in the circuit as shown, and their key specs are summarized in Figure 7.42.

### OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS

<table>
<thead>
<tr>
<th>Device*</th>
<th>Iq/channel</th>
<th>Vsat(+), V(min @ mA)</th>
<th>Vsat(-), V(max @ mA)</th>
<th>Isc, mA (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP193/293/493</td>
<td>0.017</td>
<td>4.20 @ 1</td>
<td>0.280 @ 1 (typ)</td>
<td>± 8</td>
</tr>
<tr>
<td>OP196/296/496</td>
<td>0.045</td>
<td>4.30 @ 1</td>
<td>0.430 @ 1</td>
<td>± 4</td>
</tr>
<tr>
<td>OP295/495</td>
<td>0.150 (max)</td>
<td>4.50 @ 1</td>
<td>0.110 @ 1</td>
<td>± 11</td>
</tr>
<tr>
<td>OP191/291/491</td>
<td>0.300</td>
<td>4.80 @ 2.5</td>
<td>0.075 @ 2.5</td>
<td>± 8.75</td>
</tr>
<tr>
<td>AD820/822/824</td>
<td>0.620</td>
<td>4.89 @ 2</td>
<td>0.055 @ 2</td>
<td>± 15</td>
</tr>
<tr>
<td>OP184/284/484</td>
<td>1.250 (max)</td>
<td>4.85 @ 2.5</td>
<td>0.125 @ 2.5</td>
<td>± 7.5</td>
</tr>
</tbody>
</table>
In Figure 7.41, without gain scaling resistors R2-R3, $V_{OUT}$ is simply equal to $V_{REF}$. With the scaling resistors, $V_{OUT}$ can be set anywhere between $V_{REF}$ and the positive rail, due to the op amp’s rail-rail output swing. Also, this buffered reference is inherently low dropout, allowing a $+4.5V$ reference output on a $+5V$ supply, for example. The general expression for $V_{OUT}$ is shown in the figure, where $V_{REF}$ is the reference voltage.

Amplifier standby current can be further reduced below 20µA, if an amplifier from the OP193/293/493 series is used. This will be at the expense of current drive and positive rail saturation, but does provide the lowest possible quiescent current if necessary. All devices in Figure 7.42 operate from voltages down to 3V (except the OP279, which operates at 5V).

**Low Dropout Regulators**

By adding a boost transistor to the basic rail-rail output low dropout reference of Figure 7.41, output currents of 100mA or more are possible, still retaining features of low standby current and low dropout voltage. Figure 7.43 shows a low dropout regulator with 800µA standby current, suitable for a variety of outputs at current levels of 100mA.
The 100mA output is achieved with a controlled gain bipolar power transistor for pass device Q1, an MJE170. Maximum output current control is provided by limiting base drive to Q1 via series resistor R3. This limits the base current to about 2mA, so the max HFE of Q1 then allows no more than 500mA. This limits Q1’s short circuit power dissipation to safe levels.

Overall, the circuit operates as a follower with gain, as was true in the case of Figure 7.41, so VOUT has a similar output expression. The circuit is adapted for different voltages simply by programming R1 via the table. Dropout with a 100mA load is about 200mV, thus a 5V output is maintained for inputs above 5.2V (see table), and VOUT levels down to 3V are possible. Step load response of this circuit is quite good, and transient error is only a few mVp-p for a 30-100mA load change. This is achieved with low ESR switching type capacitors at C1-C2, but the circuit also works with conventional electrolytics (with higher transient errors).

If desired, lowest output noise with the AD820 is reached by including the optional reference noise filter, R5-C3. Lower current op amps can also be used for lower standby current, but with larger transient errors due to reduced bandwidth.

While the 30mA rated output current of the REF19X series is higher than most reference ICs, it can be boosted to much higher levels if desired, with the addition of a PNP transistor, as shown in Figure 7.44. This circuit uses full time current limiting for protection of pass transistor shorts.

### 150 mA Boosted Output Regulator/Reference with Current Limiting

![Diagram of 150 mA Boosted Output Regulator/Reference with Current Limiting](image)

In this circuit the supply current of reference U1 flows in R1-R2, developing a base drive for pass device Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100-200mA loads, U1 is never required to furnish more than a few mA, and this factor minimizes temperature related drift.
Short circuit protection is provided by Q2, which clamps drive to Q1 at about 300mA of load current. With separation of control/power functions, DC stability is optimum, allowing best advantage of premium grade REF19X devices for U1. Of course, load management should still be exercised. A short, heavy, low resistance conductor should be used from U1-6 to the VOUT sense point “S”, where the collector of Q1 connects to the load.

Because of the current limiting, dropout voltage is raised about 1.1V over that of the REF19X devices. However, overall dropout typically is still low enough to allow operation of a 5 to 3.3V regulator/reference using the 3.3V REF-196 for U1, with a Vs of 4.5V and a load current of 150mA.

The heat sink requirements of Q1 depend upon the maximum power. With Vs = 5V and a 300mA current limit, the worst case dissipation of Q1 is 1.5W, less than the TO-220 package 2W limit. If TO-39 or TO-5 packaged devices such as the 2N4033 are used, the current limit should be reduced to keep maximum dissipation below the package rating, by raising R4. A tantalum output capacitor is used at C1 for its low ESR, and the higher value is required for stability. Capacitor C2 provides input bypassing, and can be an ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are in order. To enable shutdown control, the connection to U1-2 and U1-3 is broken at “X”, and diode D1 allows a CMOS control source to drive U1-3 for ON/OFF control. Startup from shutdown is not as clean under heavy load as it is with the basic REF19X series stand-alone, and can require several milliseconds under load. Nevertheless, it is still effective, and can fully control 150mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

Dedicated low dropout linear IC regulators offer all the virtues of the discrete approaches, but in a easier-to-use compact format. The ADP3367 is such a device, providing either a fixed output of 5V ±2%, or adjustable outputs over a range of 1.3 to 16.5V, with current outputs up to 300mA. Using a CMOS architecture with a PNP pass transistor, it has a quiescent current of 25µA (max., unloaded), and a dropout voltage of 175mV (max.) with a 100mA output.

Figure 7.45 shows the basic hookup for the ADP3367, which uses the "thermal coastline" 8 pin SOIC package, which is designed for power dissipation up to 960mW. For fixed 5V outputs, R1 and R2 aren’t used, and the SET pin is grounded as shown. With the SHDN pin also grounded, this simple hookup provides a constant 5V at VOUT, with the low dropout features mentioned.
The ADP3367’s useful output current capacity will be dependent upon the $V_{IN}-V_{OUT}$ differential, such that the resulting power it dissipates is contained to 960 mW or less. For example, at low input-output differences of 2.5V, up to 300mA is available. For higher input-output differences, the allowable current is reduced according to the curves shown in Figure 7.46. The upper shaded curve corresponds to the output current which is consistent with the ADP3367's package limitations. Note that the allowable output current is appreciably higher than that of a standard SO package, shown in the lower shaded curve.
The ADP3367 can be placed in a shutdown mode, which reduces the output voltage to zero and drops the standby current to less than 1µA. When implemented, shutdown is accomplished by applying a control voltage of more than 1.5V to \( V_{SHDN} \). Otherwise, this pin should be tied to ground as shown. The SET pin has a dual function, and can be used either to select an internal divider (which provides the fixed 5V output), or it can be used with an external divider, R1-R2. When the SET pin is grounded, the internal divider is active, and the 5 V output results. When the SET pin is used with the external divider, \( V_{OUT} \) is programmed as:

\[
V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)
\]

where \( V_{REF} \) is 1.255V, the internal reference voltage of the ADP3367. The divider’s absolute resistance values are not critical, since the input current at the SET pin is low, typically 10pA. This allows resistances of 100k - 1meg, consistent with the overall low standby power objectives. The example 1% values shown provide a 3.3V output. They can be further increased, if it is desired to lower standby current consumption below the \( \approx 12\mu A \) resulting with the values shown.

C2, the output capacitor, is a 10µF type, and is required for regulator stability. Larger sizes are permissible, and will help improve transient response. An input bypass is also recommended, C1.

To achieve the full power capability inherent to the design, the ADP3367 should be mounted on a PCB in such as way that internally-generated heat can flow outward easily from the die to the PCB. Large area PCB copper traces should be used beneath and around the IC, and mounting should be such that the part is exposed to unrestricted air flow [see Reference 5].
REFERENCES: POWER SUPPLY REGULATION/CONDITIONING


THERMAL MANAGEMENT

Walt Jung

For reliability reasons, modern semiconductor based systems are increasingly called upon to observe some form of thermal management. All semiconductors have some specified safe upper limit to junction temperature ($T_J$), usually on the order of 150°C (but sometimes 175°C). Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn’t be exceeded. In conservative designs, it won’t be approached by less than an ample safety margin. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. The cooler semiconductors can be kept during operation, the more closely they will approach maximum useful life.

Thermal basics

The general symbol $\theta$ is used for thermal resistance, that is:

$\theta = \text{thermal resistance, in units of °C/watt (or, °C/W)}.$

$\theta_{JA}$ and $\theta_{JC}$ are two more specific terms used in dealing with semiconductor thermal issues, which are further explained below.

In general, a device with a thermal resistance $\theta$ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1W, as measured between two reference points. Note that this is a linear relation, so a 500mW dissipation in the same part will produce a 50°C differential, and so forth. For any power $P$ (in watts), calculate the effective temperature differential ($\Delta T$) in °C as:

$\Delta T = P \times \theta$

where $\theta$ is the total applicable thermal resistance. Figure 7.47 summarizes these thermal relationships.

THERMAL BASICS

- $\theta = \text{Thermal Resistance (°C/W)}$
- $\Delta T = P \times \theta$
- $\theta_{JA} = \text{Junction - to - Ambient Thermal Resistance}$
- $\theta_{JC} = \text{Junction - to - Case Thermal Resistance}$
- $\theta_{CA} = \text{Case - to - Ambient Thermal Resistance}$
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $T_J = T_A + (P \times \theta_{JA})$, $P = \text{Total Device Power Dissipation}$
- $T_J(\text{Max}) = 150°C$ (Sometimes 175°C)
A real example illustrating this relationship is shown by Figure 7.48. These curves indicate the maximum power dissipation vs. temperature characteristic for a device using 8 pin DIP and SOIC packaging. For a $T_J(\text{max})$ of 150°C, the upper curve shows the allowable power in a DIP package. This corresponds to a $\theta$ which can be calculated by dividing the $\Delta T$ by $P$ at any point. For example, 1W of power is allowed at a $T_A$ of 60°C, so the $\Delta T$ is 150°C – 60°C = 90°C. Dividing by 1W gives this DIP package’s $\theta$ of 90°C/W. Similarly, the SOIC package yields 160°C/W. These figures are in fact the $\theta_{JA}$ for the AD823 op amp, but they also happen to be quite similar to other 8 pin devices. Given such data as these curves, the $\theta_{JA}$ for a given device can be readily determined, as above.

MAXIMUM POWER DISSIPATION VS. TEMPERATURE FOR 8-PIN MINI-DIP AND 8-PIN SOIC PACKAGES

As the relationship signifies, to maintain a low $T_J$, either $\theta$ or the power dissipated (or both) must be kept low. A low $\Delta T$ is the key to extending semiconductor lifetimes, as it leads to low maximum junction temperatures.

In semiconductors, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either the case of the device, or the ambient temperature, $T_A$, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, $\theta_{JA}$ and $\theta_{JC}$.
Taking the more simple case first, $\theta_{JA}$ is the thermal resistance of a given device measured between its junction and the ambient air. This thermal resistance is most often used with small, relatively low power ICs which do not dissipate serious amounts of power, that is 1W or less. $\theta_{JA}$ figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8 pin DIP package. It must be understood that thermal resistances are highly package dependent, as different materials have differing degrees of thermal conductivity. As a general rule of thumb, thermal resistance for the conductors within packaging materials is closely analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance (lowest $\theta$).

A summary of the thermal resistances of various IC packages is shown in Figures 7.49 and 7.50. In general, most of these packages do not lend themselves to easy heat sink attachment (with notable exceptions, such as the older round metal can types). Devices which are amenable to heat sink attachment will often be noted by a $\theta_{JC}$ dramatically lower than the $\theta_{JA}$. See for example the 15 pin SIP package (used by the AD815).

### STANDARD PACKAGE THERMAL RESISTANCES - 1

<table>
<thead>
<tr>
<th>Package</th>
<th>ADI designation</th>
<th>$\theta_{JA}$ (°C/W)</th>
<th>$\theta_{JC}$ (°C/W)</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 pin plastic DIP</td>
<td>N-8</td>
<td>90</td>
<td></td>
<td>AD823</td>
</tr>
<tr>
<td>8 pin ceramic DIP</td>
<td>D-8</td>
<td>110</td>
<td>22</td>
<td>AD712</td>
</tr>
<tr>
<td>8 pin SOIC</td>
<td>R-8</td>
<td>160</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>8 pin SOIC</td>
<td>R-8</td>
<td>90</td>
<td>60</td>
<td>ADP3367 Thermal Coastline</td>
</tr>
<tr>
<td>8 pin metal can</td>
<td>H-08A (TO-99)</td>
<td>150</td>
<td>45</td>
<td>OP07</td>
</tr>
<tr>
<td>10 pin metal can</td>
<td>H-10A (TO-100)</td>
<td>150</td>
<td>25</td>
<td>AD582</td>
</tr>
<tr>
<td>12 pin metal can</td>
<td>H-12A (TO-8)</td>
<td>100</td>
<td>30</td>
<td>AD841</td>
</tr>
<tr>
<td>14 pin plastic DIP</td>
<td>N-14</td>
<td>150</td>
<td></td>
<td>AD713</td>
</tr>
<tr>
<td>14 pin ceramic DIP</td>
<td>D-14</td>
<td>110</td>
<td>30</td>
<td>AD585</td>
</tr>
<tr>
<td>14 pin SOIC</td>
<td>R-14</td>
<td>120</td>
<td></td>
<td>AD813</td>
</tr>
<tr>
<td>15 pin SIP</td>
<td>Y-15</td>
<td>41</td>
<td>2</td>
<td>AD815 Through-Hole</td>
</tr>
<tr>
<td>16 pin plastic DIP</td>
<td>N-16</td>
<td>120</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>16 pin ceramic DIP</td>
<td>D-16</td>
<td>95</td>
<td>22</td>
<td>AD524</td>
</tr>
<tr>
<td>16 pin SOIC</td>
<td>R-16</td>
<td>85</td>
<td></td>
<td>AD811</td>
</tr>
</tbody>
</table>
\( \theta_{JC} \) is the thermal resistance of a given device as measured between its junction and the device case. This form is most often used with larger power semiconductors which do dissipate significant amounts of power, that is typically more than 1W. The reason for this is that a heat sink generally must be used with such devices, to maintain a sufficiently low internal junction temperature. A heat sink is simply an additional low thermal resistance device attached externally to a semiconductor part to aid in heat removal. It will have some additional thermal resistance of its own, also rated in °C/W.

Rather than just a single number, \( \theta \) in this case will be composed of more than one component, i.e., \( \theta_1, \theta_2, \) etc. Like series resistors, thermal impedances add, making a net calculation relatively simple. For example, to compute a net \( \theta_{JA} \) given a relevant \( \theta_{JC} \), the thermal resistance of the heat sink, \( \theta_{CA} \), or case to ambient is added to the \( \theta_{JC} \) as:

\[
\theta_{JA} = \theta_{JC} + \theta_{CA}
\]

and the result is the \( \theta_{JA} \) for that specific circumstance.

A second form of the general overall relationship between \( T_J, T_A, P \) and \( \theta \) is:

\[
T_J = T_A + (P \times \theta)
\]

To take a real world example, the AD815AVR power-tab packaged op amp has a \( \theta_{JA} \) of 41°C/W with no additional heat sinking (the device simply operating in still air). Using it just as this would allow a power of:

\[
P = (T_J - T_A)/ \theta_{JA}
\]

or, \((150°C - 70°C)/41°C/W\), which results in an allowable power of about 2W.
However, such a mode of operation falls short of the device’s full power handling capacity. The AD815AVR’s $\theta_{JC}$ is quite low at about 2°C/W, and if a heat sink of significantly less than 38°C/W is used with it, then it can dissipate much more power for a given junction temperature. A 20°C/W heat sink will allow almost twice the power to be dissipated by the same device, simply because of the lower net $\theta_{JA}$ only 22°C/W. This can be accomplished by a double-sided PCB copper plane area of 1k mm² [see Reference 1].

To illustrate, the general relationship of the AD815AVR and PCB heat sink net $\theta_{JA}$ is shown by Figure 7.51. In the first example cited above, full advantage of PCB heat sink area was not taken, and as the graph shows, the net $\theta_{JA}$ can be reduced to as low as $\pm 17°C/W$ by increasing the heat sink area further. The tradeoff is simply one of board area, and with a 2k mm² heat sink area, nearly 5W of power can be handled by the same device, assuming the same $\Delta T$ and max $T_J$. Of course, for the AD815 (and other devices) even more conservative operation is optionally possible by holding to a lower maximum $T_J$.

Note that for the data of Figure 7.51, these data assume that the AD815AVR is soldered directly to one of the dual copper PCB planes.

The power tab style package used with the AD815AVR can also be used with conventional PC mounted heat sinks, with $\theta_{JC}$ of 20°C/W and less. See Reference 2.
Calculating Power In Various Devices

In all instances of thermal calculations, a basic assumption is that the power is the total for a given package. With many modern devices now using more than one supply, the net total power dissipated will be the sum of all individual supply quiescent powers, plus any load dependent power. For many low output current opamps for example, total power will then be essentially the same as the quiescent. As long as this is safely less than the package can support, there is little worry. However, with some devices operable over a wide range of supply voltages, there are instances where high supply voltages and a medium to high quiescent current plus load current can be a problem.

The AD811 is such an example, being capable of operation from ±5V to ±15V, with a quiescent current of about 16mA. If operated at ±15V, the quiescent dissipation is nearly 500mW, which with a 90°C/W θJA, will push TJ to about 115°C in a 70°C ambient, high enough for concern. If the signal voltage output for such an amplifier doesn’t require the ±15V supplies, then reducing the supplies will lower the quiescent power, and TJ.

To illustrate a general relationship of the power dissipated in an op amp and the power in a load for family of supply voltages, Figure 7.52 was prepared. This is a test simulation of a standard gain-of-2 non inverting amplifier driving a 150Ω load, with 1kΩ gain and feedback resistors. Assuming an input voltage of 1V DC, the 2V output across the net resistor load of 150Ω || 2kΩ=140Ω will produce a power Pr of about 29mW. The AD817 amplifier operates over a supply range of ±5V to ±15V, which is the Vs sweep range for the test circuit. The op amp quiescent power Pq increases to 210mW at ±15V, while the signal power Ps dissipated by the op amp increases to 187mW at ±15V. The total power in the op amp is their sum, 397mW at ±15V. Clearly, operating relatively high current and low voltage loads from an op amp does waste considerable power, and lower voltage supplies will be much more efficient, where allowable.
Where appropriate, a clip on DIP compatible heat sink such as the AAVID 580100 can be used [Reference 3]. This series has sinks compatible with ICs of 8 through 40 pin sizes, using a staggered fin design. Performance of these (and all) heat sinks is enhanced by air movement, either through forced convection, or as a minimum, by arranging PCB cards vertically to enhance natural convection.

A/D converters can consume considerable power, although the trend is towards lower voltage and lower power dissipation. Like op amps, they are generally analyzed by adding up the total power in the package, which can then be used with the package’s $\theta_{JA}$ to compute junction temperature. In adding various power totals, some care should be made to ascertain if any power is clock dependent. In some CMOS based designs, there can be appreciable differences in power as a function high/low clock speed as shown in Figure 7.53 for the AD9220 12-bit, 10MSPS ADC.
For example, the AD9042 12 bit A/D consumes about 600mW total on two 5V supplies, and its 28 pin DIP package has a $\theta_{JA}$ of 34°C/W. What will be the max $T_J$ for this part in a $T_A$ of 70°C? You should get a $T_J$ of 90.4°C ($\Delta T = 0.6W \times 34°C/W = 20.4°C$, so $T_J$ for $T_A$ of 70°C = 70°C + 20.4°C). This particular part is therefore in good shape for this $T_A$, assuming that there are no adjacent “hot spot” sources to increase the device’s effective $T_A$.

**Airflow Control**

For large power dissipations and/or to maintain low $T_J$'s, forced air movement can be used to increase air flow and aid in heat removal. In its most simple form this can consist of a continuously or thermostatically operated fan, directed across high temperature, high wattage dissipation devices such as CPUs, DSP chips, etc.

Quite often however, more sophisticated temperature control is necessary. Recent temperature monitoring and control ICs such as the TMP12, an airflow temperature sensor IC, lend themselves to such applications.

The TMP12 includes on chip two comparators, a voltage reference, a temperature sensor and a heater. The heater is used to force a predictable internal temperature rise, to match a power IC such as a microprocessor. The temperature sensing and control portions of the IC can then be programmed to respond to the temperature changes and control an external fan, so as to maintain some range of temperature. Compared to a simple thermostat, this allows infinite resolution of user control for control points and ON/OFF hysteresis.

The device is placed in an airstream near the power IC, such that both see the same stream of air, and will thus have like temperature profiles, assuming proper control of the stream. This is shown in basic form by the layout diagram of Figure 7.54.
With the TMP12's internal 250mW heater ON and no airflow, the TMP12 thermal profile will look like the curve “A” of Figure 7.55, and will show a 20°C rise above $T_A$. When airflow is provided, this same dissipation results in a lower temperature, “D”. In programming the device for airspeed control, the designer can set up to two switch points, shown here symbolically by “B” and “C”, which are HIGH and LOW setpoints, respectively. The basic idea is that when the IC substrate reaches point B in temperature, the external fan will be turned on to create the airstream, and lower the temperature. If the overall system setup is reasonable in terms of thermal profiling, this small IC can thus be used to indirectly control another larger and independent power source with regard to its temperature. Note that the dual mode control need not necessarily be used, in all applications. An unused comparator is simply wired high or low.
Figure 7.56 shows a circuit diagram using the TMP12 as a general purpose controller. The device is connected to a 5V supply, which is also used to power a control relay and the TMP12’s internal heater at pin 5. Setpoint programming of the TMP12 is accomplished by the resistor string at pins 4 through 1, R1 - R3. These resistors establish a current drain from the internal reference source at pin 4, which sets up a reference current, $I_{REF}$, which is set as:

$$I_{REF} = (5\mu A/°C \times Thys) + 7\mu A$$

In this expression, $Thys$ is the hysteresis temperature swing desired about the setpoint, in °C, and the $7\mu A$ is recommended minimum loading of the reference. For a 2°C hysteresis for example, $I_{REF}$ is 17µA; for 5°C, it would be 32µA.

Given a desired setpoint temperature in °C, the setpoint can be converted to a corresponding voltage. Although not available externally, the internal temperature dependent voltage of the TMP12 is scaled at 5mV/°C, and is equal to 1.49V at 25°C.

To convert a setpoint temperature to a voltage $V_{SETPOINT}$,

$$V_{SETPOINT} = 1.49V + [ 5mV/°C \times (T_{SETPOINT} \text{-} T_{25}) ]$$

where $T_{SETPOINT}$ is the desired setpoint temperature, and $T_{25}$ is 25°C. For a 50°C high setpoint, this works out to be $V_{SETPOINT(HI)} = 1.615V$. For a lower setpoint of 35°C, the voltage $V_{SETPOINT(LO)}$ would be 1.59V.
The divider resistors are then chosen to draw the required current \( I_{\text{REF}} \) while setting the two tap voltages corresponding to \( V_{\text{SETPOINT(HI)}} \) and \( V_{\text{SETPOINT(LO)}} \).

\[
R_{\text{TOTAL}} = \frac{V_{\text{REF}}}{I_{\text{REF}}} = \frac{2.5V}{I_{\text{REF}}}
\]

\[
R_1 = \frac{(V_{\text{REF}} - V_{\text{SETPOINT(HI)}})}{I_{\text{REF}}}
= \frac{(2.5V - V_{\text{SETPOINT(HI)}})}{I_{\text{REF}}}
\]

\[
R_2 = \frac{(V_{\text{SETPOINT(HI)}} - V_{\text{SETPOINT(LO)}})}{I_{\text{REF}}}
\]

\[
R_3 = \frac{V_{\text{SETPOINT(LO)}}}{I_{\text{REF}}}
\]

In the example of the figure, the resulting standard values for \( R_1 \) - \( R_3 \) correspond to the temperature/voltage setpoint examples noted above. Ideal 1% values shown give resistor related errors of only 0.1°C from ideal. Note that this is error is independent of the TMP12 temperature errors, which are \( \pm 2^\circ \text{C} \).

As noted above, both comparators of the device need not always be used, and in this case the lower comparator output is not used. For a single point 50°C controller, the 35°C setpoint is superfluous. One resistor can be eliminated by making \( R_2 + R_3 \) a single value of 95.3kΩ and connecting pin 3 to GND. Pin 6 should be left as a no-connect. If a greater hysteresis is desired, the resistor values will be proportionally lowered.

It is also important to minimize potential parasitic temperature errors associated with the TMP12. Although the open-collector outputs can sink up to 20mA, it is advised that currents be kept low at this node, to limit any additional temperature rise. The Q1 - Q2 transistor buffer shown in the figure raises the current drive to 100mA, allowing a 50Ω/5V coil to be driven. The relay type shown is general purpose, and many other power interfaces are possible with the TMP12. If used as shown, the relay contacts would be used to turn on a fan for airflow when the active low output at pin 7 changes, indicating the upper setpoint threshold.

A basic assumption of the TMP12’s operation is that it will “mimic” another device in temperature rise. Therefore, a practical working system must be arranged and tested for proper airflow channeling, minimal disturbances from adjacent devices, etc. Some experimentation should be expected before a final setup will result.
**TMP12 50°C SETPOINT CONTROLLER**

**Diagram:**
- TMP12
- 0.1μF capacitor
- 5V
- IN4002 diode
- R1, R2, R3 resistors
- VPTAT
- Q1, Q2 transistors
- Hysteresis generator
- VREF
- R1 = 52.3kΩ
- R2 = 4.42kΩ
- R3 = 90.9kΩ or 95.3kΩ
- NC
- 100Ω
- 10kΩ
- 390Ω
- 5V coil, 50kΩ min
- OMRON G2R-14-DC5
- Q1, Q2 = 2N2222

**Equation:**
\[
I_{\text{REF}} = \frac{V_{\text{REF}}}{R_1 + R_2 + R_3}
\]

**Specifications:**
- FOR \( T_{\text{HYS}} = 2^\circ\text{C}, I_{\text{REF}} = 17\mu\text{A} \)
- SETPOINT (HI) = 50°C
- SETPOINT (LO) = 35°C (if used)
- R1 = 52.3kΩ
- R2 = 4.42kΩ
- R3 = 90.9kΩ or 95.3kΩ

**ANALOG DEVICES**

7.56
REFERENCES: THERMAL MANAGEMENT


EMI/RFI CONSIDERATIONS

Adolfo A. Garcia

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI hardened equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI hardened.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Elektrotechniker) in Germany. VDE regulations are more restrictive than the FCC’s with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and now requires mandatory compliance. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on radiated emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to conducted interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Table 7.1 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.
In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) now requires mandatory compliance to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Table 7.1. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory, EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically hostile, all equipment manufacturers will be required to comply with all European Community EMC regulations in 1996.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to
electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on each of the active components used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations’ Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

A DIAGNOSTIC FRAMEWORK FOR EMI/RFI PROBLEM SOLVING

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 7.57, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a source, a receptor or victim, and a path between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.
The RECEPTOR of interference

The PATH coupling the source to the receptor

<table>
<thead>
<tr>
<th>SOURCES</th>
<th>PATHS</th>
<th>RECEPTORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller</td>
<td>Radiated</td>
<td>Microcontroller</td>
</tr>
<tr>
<td></td>
<td>◆ Analog</td>
<td>◆ Analog</td>
</tr>
<tr>
<td></td>
<td>◆ Digital</td>
<td>◆ Digital</td>
</tr>
<tr>
<td>ESD</td>
<td>◆ EM Fields</td>
<td>Communications</td>
</tr>
<tr>
<td>Communications</td>
<td>◆ Crosstalk</td>
<td>◆ Receivers</td>
</tr>
<tr>
<td>Transmitters</td>
<td>◆ Capacitive</td>
<td></td>
</tr>
<tr>
<td>Power Disturbances</td>
<td>◆ Inductive</td>
<td>Other Electronic</td>
</tr>
<tr>
<td>Lightning</td>
<td>◆ Conducted</td>
<td>Systems</td>
</tr>
</tbody>
</table>

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30MHz and 300MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 7.58. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.
The second type of interference is circuit or system immunity. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is susceptibility, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is internal. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: frequency, amplitude, time, impedance, and distance.

The frequency of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI have shows that the time response of signals contains all the necessary
information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

\[ f_{\text{EMI}} = \frac{1}{\pi \cdot t_{\text{rise}}} \quad \text{Eq. 7.1} \]

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/μs and gain-bandwidth products greater than 500MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high-speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

**Passive Components: Your Arsenal against EMI**

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: passive components. To use successfully these components, the designer must understand their non-ideal behavior. For example, Figure 7.59 illustrates the real behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.
ALL PASSIVE COMPONENTS EXHIBIT "NON IDEAL" BEHAVIOR

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<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>LF BEHAVIOR</th>
<th>HF BEHAVIOR</th>
<th>RESPONSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>WIRE</td>
<td><img src="image" alt="Wire LF Behavior Diagram" /></td>
<td><img src="image" alt="Wire HF Behavior Diagram" /></td>
<td><img src="image" alt="Wire Response Graph" /></td>
</tr>
<tr>
<td>CAPACITOR</td>
<td><img src="image" alt="Capacitor LF Behavior Diagram" /></td>
<td><img src="image" alt="Capacitor HF Behavior Diagram" /></td>
<td><img src="image" alt="Capacitor Response Graph" /></td>
</tr>
<tr>
<td>INDUCTOR</td>
<td><img src="image" alt="Inductor LF Behavior Diagram" /></td>
<td><img src="image" alt="Inductor HF Behavior Diagram" /></td>
<td><img src="image" alt="Inductor Response Graph" /></td>
</tr>
<tr>
<td>RESISTOR</td>
<td><img src="image" alt="Resistor LF Behavior Diagram" /></td>
<td><img src="image" alt="Resistor HF Behavior Diagram" /></td>
<td><img src="image" alt="Resistor Response Graph" /></td>
</tr>
</tbody>
</table>

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02Ω/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20nH/inch, it becomes inductive at frequencies above 13kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of real components, a strategy can now be developed to find solutions to most EMI problems.

**Radio Frequency Interference**

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define immunity to be an instrument’s susceptibility to the applied RFI power density at the unit. In more general EMI analysis, the electric-field intensity is used to describe RFI stimulus.
For comparative purposes, Equation 7.2 can be used to convert electric-field intensity to power density and vice-versa:

\[
\tilde{E} \left( \frac{V}{m} \right) = 61.4 \sqrt[3]{\frac{P_T}{mW}} \text{ Eq. 7.2}
\]

where \( E \) = Electric Field Strength, in volts per meter, and 
\( P_T \) = Transmitted power, in milliwatts per cm\(^2\).

From the standpoint of the source-path-receptor model, the strength of the electric field, \( E \), surrounding the receptor is a function of transmitted power, antenna gain, and distance from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 7.3:

\[
\tilde{E} \left( \frac{V}{m} \right) = 5.5 \left( \sqrt[3]{\frac{P_T \cdot G_A}{d}} \right) \text{ Eq. 7.3}
\]

where \( E \) = Electric field intensity, in V/m; 
\( P_T \) = Transmitted power, in mW/cm\(^2\); 
\( G_A \) = Antenna gain (numerical); and 
\( d \) = distance from source, in meters.

For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 7.60, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.
There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 7.61). The three general points of RFI coupling are signal inputs, signal outputs, and power supplies. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1µF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.
Decouple all voltage supplies to analog chip with high-frequency capacitors
Use high-frequency filters on all lines that leave the board
Use high-frequency filters on the voltage reference if it is not grounded

Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 7.62, real low-pass filters may exhibit leakage at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to leak when the applied signal frequency is 100 to 1000 higher than the filter’s cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.
A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 $f_{3dB}$

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into low-band, mid-band, and high-band, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of woofer-midrange-tweeter for RFI low-pass filter design illustrated in Figure 7.63. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as feed-through protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.
MULTISTAGE FILTERS ARE MORE EFFECTIVE

Another cause of filter failure is illustrated in Figure 7.64. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.
The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate transient power-line disturbances.

Figure 7.65 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.
Commercial EMI filters, as illustrated in Figure 7.66, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering as in Figure 7.66. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they are not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.
Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), or for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 7.67, isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.
FARADAY SHIELDS IN ISOLATION TRANSFORMERS PROVIDE INCREASING LEVELS OF PROTECTION

- STANDARD TRANSFORMER - NO SHIELD
  - NOTE CONNECTION FROM SECONDARY TO SAFETY GROUND TO ELIMINATE GROUND-TO-NEUTRAL VOLTAGE

- SINGLE FARADAY SHIELD
  - CONNECT TO SAFETY GROUND FOR COMMON-MODE PROTECTION

- SINGLE FARADAY SHIELD
  - CONNECT TO NOISY-SIDE NEUTRAL WIRE FOR DIFFERENTIAL-MODE PROTECTION

- TRIPLE FARADAY SHIELD
  - CONNECT TO SAFETY GROUND FOR COMMON MODE
  - CONNECT TO NEUTRALS FOR DIFFERENTIAL MODE

PRINTED CIRCUIT BOARD DESIGN FOR EMI PROTECTION

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system’s susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 7.68 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.
A key point in minimizing noise problems in a design is to choose devices no faster than actually required by the application. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs and can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 7.69 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.
Once the system’s critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 7.70. These low-impedance planes form very high-frequency stripline transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.
"TO EMBED OR NOT TO EMBED"
THAT IS THE QUESTION

BEFORE AFTER
Route Power
Power Route
Ground Route
Route Ground

Advantages of Embedding
◆ Lower impedances, therefore lower emissions and crosstalk
  | Reduction in emissions and crosstalk is significant above 50MHz
◆ Traces are protected

Disadvantages of Embedding
| Lower interboard capacitance, harder to decouple
| Impedances may be too low for matching
| Hard to prototype and troubleshoot buried traces

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster). A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance and if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 7.71 for a number of logic families.

LINE TERMINATION SHOULD BE USED WHEN
LENGTH OF PCB TRACK EXCEEDS 2 inches / ns

<table>
<thead>
<tr>
<th>DIGITAL IC FAMILY</th>
<th>$t_r$, $t_f$ (ns)</th>
<th>PCB TRACK LENGTH (inches)</th>
<th>PCB TRACK LENGTH (cm)</th>
</tr>
</thead>
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<td>GaAs</td>
<td>0.1</td>
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<tr>
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<tr>
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<td>3</td>
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<tr>
<td>AS</td>
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<tr>
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<tr>
<td>TTL</td>
<td>10</td>
<td>20</td>
<td>50</td>
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</tbody>
</table>

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\( t_r = \text{rise time of signal in ns} \)
\( t_f = \text{fall time of signal in ns} \)

For analog signals @ \( f_{\text{max}} \), calculate \( t_r = t_f = 0.35 / f_{\text{max}} \)

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of \( f_{\text{max}} \), then the equivalent risetime, \( t_r \), can be calculated using the equation \( t_r = 0.35/f_{\text{max}} \). The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 7.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board’s dielectric (microstrip transmission line):

\[
Z_0(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left[ \frac{5.98d}{0.89w + t} \right] \quad \text{Eq. 7.4}
\]

where \( \varepsilon_r \) = dielectric constant of printed circuit board material;
\( d \) = thickness of the board between metal layers, in mils;
\( w \) = width of metal trace, in mils; and
\( t \) = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 7.5:

\[
t_{pd}(\text{ns/ft}) = 1.017 \sqrt{0.475\varepsilon_r + 0.67} \quad \text{Eq. 7.5}
\]

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021” FR-4 (\( \varepsilon_r=4.7 \)) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88\( \Omega \) and 1.7ns/ft (7”/ns), respectively. Transmission lines can be effectively terminated in several ways depending on the application, as described in Section 2 of this book.
REFERENCES ON EMI/RFI


SHIELDING CONCEPTS
Adolfo Garcia, John McDonald

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1, 2, and 6 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength ($\lambda$) of the interference divided by $2\pi$, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by $2\pi$ yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the reflection of the incident wave off the shielding material. Second is the loss due to the absorption of the transmitted wave within the shielding material. Both concepts are illustrated in Figure 7.72. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.
Reflection and absorption are the two principal shielding mechanisms.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

\[
R_e (dB) = 322 + 10\log_{10} \left( \frac{\sigma_r}{\mu_r f^2 r^2} \right) \quad \text{Eq. 7.6}
\]

where 
\( \sigma_r \) = relative conductivity of the shielding material, in Siemens per meter;
\( \mu_r \) = relative permeability of the shielding material, in Henries per meter;
\( f \) = frequency of the interference, and
\( r \) = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

\[
R_m (dB) = 14.6 + 10\log_{10} \left( \frac{f r^2 \sigma_r}{\mu_r} \right) \quad \text{Eq. 7.7}
\]

and, for plane waves ( \( r > \lambda/2\pi \)), the reflection loss is given by:

\[
R_{pw} (dB) = 168 + 10\log_{10} \left( \frac{\sigma_r}{\mu_r f} \right) \quad \text{Eq. 7.8}
\]
Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

\[ A_{dB} = 3.34 \, t \sqrt{\sigma_r \mu_r f} \quad \text{Eq. 7.9} \]

where \( t \) = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (\( \delta \)) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, \( Z_s \), increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 7.73.

### IMPEDANCE AND SKIN DEPTHS FOR VARIOUS SHIELDING MATERIALS

| Material | Conductivity \( \sigma_r \) | Permeability \( \mu_r \) | Shield Impedance \( |Z_s| \) | Skin Depth \( \delta \) (inch) |
|----------|-----------------|-----------------|-----------------|-----------------|
| Cu       | 1               | 1               | \( 3.68 \times 10^{-7} \sqrt{f} \) | \( \frac{2.6}{\sqrt{f}} \) |
| Al       | 1               | 0.61            | \( 4.71 \times 10^{-7} \sqrt{f} \) | \( \frac{3.3}{\sqrt{f}} \) |
| Steel    | 0.1             | 1,000           | \( 3.68 \times 5 \sqrt{f} \) | \( \frac{0.26}{\sqrt{f}} \) |
| \( \mu \) Metal | 0.03         | 20,000          | \( 3E - 4 \sqrt{f} \) | \( \frac{0.11}{\sqrt{f}} \) |

where \( \varepsilon_0 = 5.82 \times 10^7 \, \text{S/m} \),
\( \mu_0 = 4\pi \times 10^{-7} \, \text{H/m} \),
\( e_0 = 8.85 \times 10^{-12} \, \text{F/m} \)
A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 7.74). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

**ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS**

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The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 7.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

\[
\text{Shielding Effectiveness (dB)} = 20 \log_{10} \left( \frac{\lambda}{2 \cdot L} \right) \quad \text{Eq. 7.10}
\]

where \( \lambda \) = wavelength of the interference and
\( L \) = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is
preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

**Sensors and Cable Shielding**

The improper use of cables and their shields is a significant contributor to both radiated and conducted interference. As illustrated in Figure 7.75, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

**LENGTH OF SHIELDED CABLES DETERMINES AN "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION**

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![Diagram](7.75)

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a
low-impedance point. A generalized example of this mechanism is illustrated in Figure 7.76.

CONNECT THE SHIELD AT ONE POINT AT THE LOAD TO PROTECT AGAINST LOW FREQUENCY (50/60Hz) THREATS

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In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1Vrms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is electrically long, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01µF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.
Shielded Twisted Pair Cable Grounding Examples

The environments in which analog systems operate are often rich in sources of EMI. Common EMI noise sources include power lines, logic signals, switching power supplies, radio stations, electric lighting, and motors. Noise from these sources can easily couple into long analog signal paths, such as cables, which act as efficient antennas. Shielded cables protect signal conductors from electric field (E-field) interference by providing low impedance paths to ground at the offending frequencies. Aluminum foil, copper, and braided stainless steel are materials very commonly used for cable shields due to their low impedance properties.

Simply increasing the separation between the noise source and the cable will yield significant additional attenuation due to reduced coupling, but shielding is still required in most applications involving remote sensors.

There are two paths from an EMI source to a susceptible cable: capacitive (or E-field) and magnetic (or H-field) coupling. Capacitive coupling occurs when parasitic capacitance exists between a noise source and the cable. The amount of parasitic capacitance is determined by the separation, shape, orientation, and the medium between the source and the cable.

Magnetic coupling occurs through parasitic mutual inductance when a magnetic field is coupled from one conductor to another. Parasitic mutual inductance depends on the shape and relative orientation of the circuits in question, the magnetic properties of the medium, and is directly proportional to conductor loop area. Minimizing conductor loop area reduces magnetic coupling proportionally.

Shielded \textit{twisted pair} cables offer further noise immunity to magnetic fields. Twisting the conductors together reduces the net loop area, which has the effect of canceling any magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero.

To study the shielding problem, a precision \textit{RTD (Resistance Temperature Detector)} amplifier circuit was used as the basis for a series of experiments. A remote 100Ω RTD was connected to the bridge, bridge driver, and the bridge amplifier circuit (Figure 7.77) using 10 feet of a shielded twisted pair cable. The RTD is one element of a 4-element bridge (the three other resistor elements are located in the bridge and bridge driver circuit). The gain of the instrumentation amplifier was adjusted so that the sensitivity at the output was 10mV/°C, with a 5V full scale. Measurements were made at the output of the instrumentation amplifier with the shield grounded in various ways. The experiments were conducted in lab standard environment where a considerable amount of electronic equipment was in operation.
The first experiment was conducted with the shield ungrounded. As shown in Figure 7.77, shields left floating are not useful and offer no attenuation to EMI-induced noise, in fact, they act as antennas. Capacitive coupling is unaffected, because the floating shield provides a coupling path to the signal conductors. Most cables exhibit parasitic capacitances between 10-30pF/ft. Likewise, HF magnetically coupled noise is not attenuated because the floating cable shield does not alter either the geometry or the magnetic properties of the cable conductors. LF magnetic noise is not attenuated significantly, because most shield materials absorb very little magnetic energy.

To implement effective EMI/RFI shielding, the shield must be grounded. A grounded shield reduces the value of the impedance of the shield to ground to small values. Implementing this change will reduce the amplitude of the E-Field noise substantially.

Designers often ground both ends of a shield in an attempt to reduce shield impedance and gain further E-Field attenuation. Unfortunately, this approach can create a new set of potential problems. The AC and DC ground potentials are generally different at each end of the shield. Low-frequency ground loop current is created when both ends of a shield are grounded. This low frequency current flows through the large loop area of the shield and couples into the center conductors through the parasitic mutual inductance. If the twisted pairs are precisely balanced, the induced voltage will appear as a common-mode rather than a differential voltage. Unfortunately, the conductors may not be perfectly balanced, the sensor and excitation circuit may not be fully balanced, and the common mode rejection at the receiver may not be sufficient. There will therefore be some differential noise voltage developed between the conductors at the output end, which is amplified and
appears at the final output of the instrumentation amplifier. With the shields of the experimental circuit grounded at both ends, the results are shown in Figure 7.78.

**GROUNDING BOTH ENDS OF A SHIELD PRODUCES LOW FREQUENCY GROUND LOOPS**

![Diagram](image)

_VERTICAL SCALE: 2mV/div
HORIZONTAL SCALE: 10ms/div_

Figure 7.79 illustrates a properly grounded system with good electric field shielding. Notice that the ground loop has been eliminated. The shield has a single point ground, located at the signal conditioning circuitry, and noise coupled into the shield is effectively shunted into the receiver ground and does not appear at the output of the instrumentation amplifier.
Figure 7.80 shows an example of a remotely located, ungrounded, passive sensor (ECG electrodes) which is connected to a high-gain, low power AD620 instrumentation amplifier through a shielded twisted pair cable. Note that the shield is properly grounded at the signal conditioning circuitry. The AD620 gain is $1000 \times$, and the amplifier is operated on $\pm 3V$ supplies. Notice the absence of 60Hz interference in the amplifier output.
Most high impedance sensors generate low-level current or voltage outputs, such as a photodiode responding to incident light. These low-level signals are especially susceptible to EMI, and often are of the same order of magnitude as the parasitic parameters of the cable and input amplifier.

Even properly shielded cables can degrade the signals by introducing parasitic capacitance that limits bandwidth, and leakage currents that limit sensitivity. An example is shown in Figure 7.81, where a high-impedance photodiode is connected to a preamp through a long shielded twisted pair cable. Not only will the cable capacitance limit bandwidth, but cable leakage current limits sensitivity. A pre-amplifier, located close to the high-impedance sensor, is recommended to amplify the signal and to minimize the effect of cable parasitics.
SHIELDS ARE NOT EFFECTIVE WITH HIGH IMPEDANCE REMOTE SENSORS

Figure 7.82 is an example of a high-impedance photodiode detector and pre-amplifier, driving a shielded twisted pair cable. Both the amplifier and the shield are grounded at a remote location. The shield is connected to the cable driver common, G1, ensuring that the signal and the shield at the driving end are both referenced to the same point. The capacitor on the receiving side of the cable shunts high-frequency noise on the shield into ground G2 without introducing a low-frequency ground loop. This popular grounding scheme is known as hybrid grounding.
Figure 7.83 illustrates a balanced active line driver with a hybrid shield ground implementation. When a system’s operation calls for a wide frequency range, the hybrid grounding technique often provides the best choice (Reference 8). The capacitor at the receiving end shunts high-frequency noise on the shield into G2 without introducing a low-frequency ground loop. At the receiver, a common-mode choke can be used to help prevent RF pickup entering the receiver, and subsequent RFI rectification (see References 9 and 10). Care should be taken that the shields are grounded to the chassis entry points to prevent contamination of the signal ground (Reference 11).
To summarize this discussion, shield grounding techniques must take into account the type and the configuration of the sensor as well as the nature of the interference. When a low-impedance passive sensor is used, grounding the shield to the receiving end is the best choice. Active sensor shields should generally be grounded at the source (direct connection to source ground) and at the receiver (connect to receiver ground using a capacitor). This hybrid approach minimizes high-frequency interference and prevents low-frequency ground loops. Shielded twisted conductors offer additional protection against shield noise because the coupled noise occurs as a common-mode, and not a differential signal.

The best shield can be compromised by poor connection techniques. Shields often use “pig-tail” connections to make the connection to ground. A “pig-tail” connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

As shown in Figure 7.84, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through stray capacitance. If the length of the cable is considered electrically long at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the figure, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used.
"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA

ICM = COMMON-MODE CURRENT

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REFERENCES: CABLE SHIELDING


4. AD620 Instrumentation Amplifier, Data Sheet, Analog Devices, Inc.


GENERAL REFERENCES: HARDWARE DESIGN TECHNIQUES


2. **E.S.D. Prevention Manual**
   Available free from Analog Devices, Inc.


   AND

   Free from Analog Devices.

6. International EMI Emission Regulations
   Canada    CSA C108.8-M1983    FDR    VDE 0871/VDE 0875
   Japan     CISPR (VCCI)/PUB 22    USA    FCC-15 Part J

   Free from Analog Devices.


   Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.


PREFACE:
HIGH SPEED DESIGN TECHNIQUES

High speed integrated circuits, both analog, digital, and mixed-signal are used in all types of electronic equipment today. This book examines high speed linear ICs both from the theoretical and practical application point of view.

Figure P.1 shows some of the typical applications for high speed integrated circuits by market segment. Many applications can be filled using standard linear IC products, while others may be better served with specially designed chipsets (see Figure P.2).

All of these high speed linear ICs depend upon a broad base of high speed core competencies shown in Figure P.3. Analog Devices has been a leader in real-world signal processing for over 30 years and has the required expertise in each critical competency area. Regardless of how complex or highly integrated mixed-signal ICs may become, there is no escaping the requirement for these basic building blocks.

An understanding of these building blocks is required for the customer to successfully specify, select, and apply new high speed products at the system level. While a detailed knowledge of the internal circuits is not required, an overall understanding of the operation of the devices is critical to success.

This book is not intended to be a system design manual. Instead, it covers the theory and application of many high speed analog signal processing building blocks such as amplifiers, ADCs, DACs, etc. System applications are presented when they are of broad general interest or illustrate emerging market trends.

The proper application of high speed devices also requires a thorough knowledge of good hardware design techniques, such as simulation, prototyping, layout, decoupling, and grounding. The last section in the book focuses on these issues as well as EMI and RFI design considerations.
## HIGH SPEED PRODUCTS: TYPICAL APPLICATIONS

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### ADI HIGH SPEED INTEGRATED / CHIPSET SOLUTIONS

- Cellular Communications: GSM, DECT, AMPS, PCS, etc. (Handsets and Basestations)
- ADSL/HDSL
- CCD Imaging
- Video Signal Processing (MPEG, etc.)
- Fiber Optic and Disk Drive Data Recovery
- Direct Broadcast Satellite Receivers
- High Speed Modems
- Multimedia Sound and Video Processing
CORE COMPETENCIES: "DC TO LIGHT"

- Amplifiers:
  Op Amps, VCAs, PGAs, Log Amps,
  Sample-and-Hold Amplifiers

- Switches and Multiplexers

- Analog-to-Digital Converters (ADCs)

- Digital-to-Analog Converters (DACs)

- Analog Signal Processing
  Multipliers, RMS-DC Converters, etc.

- RF/IF Signal Processing

- DSP
SECTION 1

SINGLE-SUPPLY AMPLIFIERS

- Rail-to-Rail Input Stages
- Rail-to-Rail Output Stages
- Single-Supply Instrumentation Amplifiers
SECTION 1
SINGLE-SUPPLY AMPLIFIERS

Adolfo Garcia

Over the last several years, single-supply operation has become an increasingly important requirement as systems get smaller, cheaper, and more portable. Portable systems rely on batteries, and total circuit power consumption is an important and often dominant design issue, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of “doing more with less” in their amplifier designs.

SINGLE-SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - Lower Power
  - Battery Operated Portable Equipment
  - Simplifies Power Supply Requirements

- **But Watch Out for:**
  - Signal-swings limited, therefore more sensitive to errors caused by offset voltage, bias current, finite open-loop gain, noise, etc.
  - More likely to have noisy power supply because of sharing with digital circuits
  - DC coupled, multi-stage single-supply circuits can get very tricky!
  - Rail-to-rail op amps needed to maximize signal swings

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1mV are less than a 0.04 LSB error source in a 12-bit, 10V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1mV represents a 0.8LSB error in a 5V FS system, and 1.6LSB error in a 2.5V FS system.

Furthermore, amplifier bias currents, now flowing in larger source resistances to keep current drain from the battery low, can generate offset errors equal to or greater than the amplifier's own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers having open-loop gains in the millions typically operate on dual supplies: for example, the OP07 family types. However, many single-supply/rail-to-rail amplifiers for precision applications
typically have open-loop gains between 25,000 and 30,000 under light loading (>10kohm). Selected devices, like the OPX13 family, do have high open-loop gains (i.e., >1V/µV).

Many trade-offs are possible in the design of a single-supply amplifier: speed versus power, noise versus power, precision versus speed and power, etc. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. System noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0V) is very convenient, as there is equal supply headroom in each direction, and 0V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0V input.

"RAIL-TO-RAIL" AMPLIFIERS

- What exactly is “rail-to-rail”
- Does the input common mode range (for guaranteed CMMR) include: 0V, +Vs, both, or neither?
- Output Voltage Swing (how close to the rails can you get under load?)
- Where is “ground”?
- Complementary bipolar processes make rail-to-rail inputs and outputs feasible (within some fundamental physical limitations)
- Implications for precision single-supply instrumentation amps
Early single-supply “zero-in, zero-out” amplifiers were designed on bipolar processes which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much poorer performance than the NPNs. Fully complementary processes are now required for the new-breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs do not use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose collector-emitter saturation voltage or drain-source channel on-resistance determine output signal swing with the load current.

The characteristics of a single-supply amplifier input stage (common-mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low-voltage applications. Rail-to-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or at the amplifier’s positive supply. Amplifiers having a minimum of 60dB common-mode rejection over the entire input common-mode voltage range from 0V to the positive supply ($V_{POS}$) are good candidates. It is not necessary that amplifiers maintain common-mode rejection for signals beyond the supply voltages: what is required is that they do not self-destruct for momentary overvoltage conditions. Furthermore, amplifiers that have offset voltages less than 1mV and offset voltage drifts less than 2µV/°C are also very good candidates for precision applications. Since input signal dynamic range and SNR are equally if not more important than output dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5µVp-p in the 0.1Hz to 10Hz band.

Since the need for rail-to-rail amplifier output stages is driven by the need to maintain wide dynamic range in low-supply voltage applications, a single-supply/rail-to-rail amplifier should have output voltage swings which are within at least 100mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current, but the voltage swing of a good output stage should maintain its rated swing for loads down to 10kohm. The smaller the $V_{OL}$ and the larger the $V_{OH}$, the better. System parameters, such as “zero-scale” or “full-scale” output voltage, should be determined by an amplifier’s $V_{OL}$ (for zero-scale) and $V_{OH}$ (for full-scale).

Since the majority of single-supply data acquisition systems require at least 12- to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications.

**SINGLE-SUPPLY/RAIL-TO-RAIL OP AMP INPUT STAGES**

With the increasing emphasis on low-voltage, low-power, and single-supply operation, there is some demand for op amps whose input common-mode range includes both supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished
from the many applications where common-mode range close to the supplies or one that includes one of the supplies is necessary, but input rail-rail operation is not.

In many single-supply applications, it is required that the input go to only one of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using either PNP transistors (see OP90 and the OPX93 in Figure 1.3) or N-channel JFETs (see AD820 family in Figure 1.4). P-channel JFETs can be used where inputs must include the positive supply rail (but not the negative rail) as shown in Figure 1.4 for the OP282/OP482.

**Figure 1.3**

In the FET-input stages of Figure 1.4, the possibility exists for phase reversal as input signals approach and exceed the amplifier’s linear input common-mode voltage ranges. As described in Section 7, internal amplifier stages saturate, forcing subsequent stages into cutoff. Depending on the structure of the input stage, phase reversal forces the output voltage to one of the supply rails. For n-channel JFET-input stages, the output voltage goes to the negative output rail during phase reversal. For p-channel JFET-input stages, the output is forced to the positive output rail. New FET-input amplifiers, like the AD820 family of amplifiers, incorporate design improvements that prevent output voltage phase reversal for signals within the rated supply voltage range. Their input stage and second gain stage even offer protection against output voltage phase reversal for input signals 200mV more positive than the positive supply voltage.
As shown in Figure 1.5, true rail-to-rail input stages require two long-tailed pairs, one of NPN bipolar transistors (or N-channel FETs), the other of PNP transistors (or p-channel FETs). These two pairs exhibit different offsets and bias currents, so when the applied input common-mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources (I1 and I2) remain active throughout the entire input common-mode range, amplifier input offset voltage is the average offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the common-mode input voltage range, compared to familiar dual supply precision devices like the OP07 or OP97. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over part of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices.
Many rail-to-rail amplifier input stage designs switch operation from one differential pair to the other differential pair somewhere along the input common-mode voltage range. Devices like the OPX91 family and the OP279 have a common-mode crossover threshold at approximately 1V below the positive supply. In these devices, the PNP differential input stage remains active; as a result, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are all determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common-mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active. As a result, source impedance levels should be balanced when using such devices, as mentioned before, to minimize input bias current offsets and distortion.

An advantage to this type of rail-to-rail input stage design is that input stage transconductance can be made constant throughout the entire input common-mode voltage range, and the amplifier slew symmetrically for all applied signals.

Operational amplifiers, like the OP284/OP484, utilize a rail-to-rail input stage design where both PNP and NPN transistor pairs are active throughout the entire input common-mode voltage range, and there is no common-mode crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages. Amplifier input offset voltage exhibits a smooth transition throughout the entire input common-mode voltage range because of careful laser-trimming of resistors in the input stage. In the same manner, through careful input stage current balancing and input transistor design, amplifier input bias currents also exhibit a smooth transition throughout the entire common-mode input voltage range. The exception occurs at the extremes of the input common-mode range,
where amplifier offset voltages and bias currents increase sharply due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1V of either supply rail.

When both differential pairs are active throughout the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of the square root of 2 for FET input stages. Input stage transconductance determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching VPOS) or the NPN stage (signals approaching GND) are forced into cutoff. The thresholds at which the transconductance changes occur approximately within 1V of either supply rail, and the behavior is similar to that of the input bias currents.

Applications which initially appear to require true rail-rail inputs should be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable. A true rail-to-rail input amplifier should not generally be used if an input range which includes only one rail is satisfactory.

**SINGLE-SUPPLY/RAIL-TO-RAIL OP AMP OUTPUT STAGES**

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 1.6. Naturally, the slew rates were greater for positive-going than for negative-going signals. While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. This asymmetry, which generally results from the use of IC processes with better NPN than PNP transistors, may also result in the ability of the output to approach one supply more closely than the other.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity.
An IC process with relatively well-matched (AC and DC) PNP and NPN transistors allows both the output voltage swing and slew rate to be reasonably well matched. However, an output stage using BJTs cannot swing completely to the rails, but only to within the transistor saturation voltage ($V_{CESAT}$) of the rails (see Figure 1.7). For small amounts of load current (less than 100µA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).

On the other hand, an output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically, 100ohms).
In summary, the following points should be considered when selecting amplifiers for single-supply/rail-to-rail applications:

First, input offset voltage and input bias currents can be a function of the applied input common-mode voltage (for true rail-to-rail input op amps). Circuits using this class of amplifiers should be designed to minimize resulting errors. An inverting amplifier configuration with a false ground reference at the non-inverting input prevents these errors by holding the input common-mode voltage constant. If the inverting amplifier configuration cannot be used, then amplifiers like the OP284/OP484 which do not exhibit any common-mode crossover thresholds should be used.

Second, since input bias currents are not always small and can exhibit different polarities, source impedance levels should be carefully matched to minimize additional input bias current-induced offset voltages and increased distortion. Again, consider using amplifiers that exhibit a smooth input bias current transition throughout the applied input common-mode voltage.

Third, rail-to-rail amplifier output stages exhibit load-dependent gain which affects amplifier open-loop gain, and hence closed-loop gain accuracy. Amplifiers with open-loop gains greater than 30,000 for resistive loads less than 10kohm are good choices in precision applications. For applications not requiring full rail-rail swings, device families like the OPX13 and OPX93 offer DC gains of 0.2V/µV or more.

Lastly, no matter what claims are made, rail-to-rail output voltage swings are functions of the amplifier’s output stage devices and load current. The saturation voltage (VCESAT), saturation resistance (RSAT), and load current all affect the amplifier output voltage swing.
These considerations, as well as those regarding rail-to-rail precision, have implications in many circuits, namely instrumentation amplifiers, which will be covered in the next sections.

**THE TWO OP AMP INSTRUMENTATION AMPLIFIER TOPOLOGY**

There are several circuit topologies for instrumentation amplifier circuits suitable for single-supply applications. The *two op amp* configuration is often used in cost- and space-sensitive applications, where tight matching of input offset voltage, input bias currents, and open-loop gain is important. Also, when compared to other topologies, the two op amp instrumentation amplifier circuit offers the lowest power consumption and low total drift for moderate-gain (G=10) applications. Obviously, it also has the merit of using a single dual op amp IC.

Figure 1.8 shows the topology of a two op amp instrumentation circuit which uses a 5th gain-setting resistor, $R_G$. This additional gain-setting resistor is optional, and should be used in those applications where a fine gain trim is required. Its effect will be included in this analysis.

Circuit resistor values for this topology can be determined from Equations 1.1 through 1.3, where $R_1 = R_4$. To maintain low power consumption in single-supply applications, values for $R$ should be no less than 10kohms:

$$R_1 = R_4 = R \quad \text{Eq. 1.1}$$

$$R_2 = R_3 = \frac{R}{0.9G - 1} \quad \text{Eq. 1.2}$$

$$R_G = \frac{2R}{0.06G} \quad \text{Eq. 1.3}$$

where $G$ equals the desired circuit gain. Note that in those applications where fine gain trimming is not required, Eq. 1.2 reduces to:

$$R_2 = R_3 = \frac{R}{G - 1} \quad \text{Eq. 1.4}$$

A nodal analysis of the topology will illustrate the behavior of the circuit’s nodal voltages and the amplifier output currents as functions of the applied common-mode input voltage ($V_{CM}$), the applied differential (signal) voltage ($V_{IN}$), and the output reference voltage ($V_{REF}$). These expressions are summarized in Equations 1.5 through 1.8, Eq. 1.12, and in Eq. 1.13 for positive, input differential voltages. Due to the structure of the topology, expressions for voltages and currents are similar in form and magnitude for negative, input differential voltages.
From the figure, expressions for the four nodal voltages A, B, C, and $V_{OUT}$ as well as the output stage currents of A1 ($I_{OA1}$) and A2 ($I_{OA2}$) have been developed. Note that the direction of the amplifier output currents, $I_{OA1}$ and $I_{OA2}$, is defined to be into the amplifier’s output stage. For example, if the nodal analysis shows that $I_{OA1}$ and $I_{OA2}$ are positive entities, their direction is into the device; thus, their output stages are sinking current. If the analysis shows that they are negative quantities, their direction is opposite to that shown; therefore, their output stages are sourcing current.

Resistors $R_{P1}$ and $R_{P2}$ at the inputs to the circuit are optional input current limiting resistors used to protect the amplifier input stages against input overvoltage. Although any reasonable value can be used, these resistors should be less than 1kohm to prevent the unwanted effects of additional resistor noise and bias current-generated offset voltages. For protection against a specific level of overvoltage, the interested reader should consult the section on overvoltage effects on integrated circuits, found in Section 7 of this book.

![THE TWO OP AMP INSTRUMENTATION AMPLIFIER TOPOLOGY IN SINGLE-SUPPLY APPLICATIONS](image)

**Figure 1.8**

Using half-circuit concepts and the principle of superposition, the input signal voltage, $V_{IN}$, on the non-inverting input of A1 is set to zero. Since the input signal, $V_{IN+}$, is applied to the non-inverting terminal of A2, an expression for the nodal voltage at the inverting terminal of A1 is given by Eq. 1.5:

$$V_A = V_{CM} \quad \text{Eq. 1.5}$$

An expression for the output voltage of A1 (node B) shows that it is dependent on all three externally applied voltages ($V_{IN}$, $V_{CM}$, and $V_{REF}$), and is illustrated in Eq. 1.6:

$$V_B = (-V_{IN} + \left(\frac{R_2}{R_G}\right) + V_{CM}\left(1 + \frac{R_2}{R_1}\right) - V_{REF}\left(\frac{R_2}{R_1}\right) \quad \text{Eq. 1.6}$$
Since the input signal, $V_{IN+}$, as well as the applied input common-mode voltage, $V_{CM}$, is applied to the non-inverting terminal of A2, then the expression for the voltage at A2’s inverting input (node C) is given by:

$$V_C = V_{CM} + V_{IN+}$$  \hspace{1cm} \text{Eq. 1.7}$$

For the case where $R_1 = R_4$ and $R_2 = R_3$, combining the results in Eq. 1.5, 1.6, and 1.7 yields the familiar expression for the circuit’s output voltage:

$$V_{OUT} = (V_{IN+} + \left(1 + \frac{R_4}{R_3} + \frac{2R_4}{R_G}\right) + V_{REF}$$  \hspace{1cm} \text{Eq. 1.8}$$

At this point, it is worth noting the behavior of the circuit’s nodal voltages based on the applied external voltages. From Eq. 1.5 and Eq. 1.7, the common-mode component of the current through $R_G$ is equal to zero, whereas the full differential input voltage appears across it. Furthermore, Eq. 1.6 has shown that A1 amplifies the applied common-mode input voltage by a factor of $(1 + R_2/R_1)$. In low-gain applications, the ratio of $R_2$ to $R_G$ can be as small as 1:1 (for circuit gains greater than or equal to 2). Therefore, Equation 1.6 sets the upper bound on the input common-mode voltage in low-gain applications. If the output of A1 is allowed to saturate at high input common-mode voltages, then it will not have enough “headroom” to amplify the input signal, as shown in Eq. 1.6. Therefore, in order for A1 to amplify accurately input signal voltages for any circuit gain $> 1$ (circuit gains equal to 1 are not permitted in this topology) requires that an upper bound on the total applied input voltage (common-mode plus differential-mode voltages) be determined to prevent amplifier output voltage saturation. This upper bound can be determined by the desired circuit gain, $G$, and the amplifier’s minimum output high voltage:

$$V_{IN(Total)} < V_{OH(MIN)} \left(\frac{0.9G-1}{0.9G}\right) - V_{IN+}$$  \hspace{1cm} \text{Eq. 1.9}$$

In a similar fashion, a lower bound on the total applied input voltage is also determined by circuit gain and the amplifier’s maximum output low voltage:

$$V_{IN(Total)} > V_{OL(MAX)} \left(\frac{0.9G-1}{0.9G}\right) + V_{IN+}$$  \hspace{1cm} \text{Eq. 1.10}$$

For example, if a rail-to-rail operational amplifier exhibited a $V_{OL(MAX)}$ equal to 10mV and a $V_{OH(MIN)}$ equal to 4.95V, and if the application required a circuit gain of 10 to produce a 1V full-scale output, then the total input voltage range would be bounded by:

$$0.109 \text{ V} < V_{IN(Total)} < 4.3 \text{ V}$$
Therefore, the range over which the circuit will handle input voltages without amplifier output voltage saturation is given by:

\[ V_{OL(MAX)} \left( \frac{0.9G-1}{0.9G} \right) + V_{IN}^+ < V_{IN(TOTAL)} < V_{OH(MIN)} \left( \frac{0.9G-1}{0.9G} \right) - V_{IN}^+ \]

Eq. 1.11

In low-gain instrumentation circuits, the usable input voltage range is limited and asymmetric about the supply mid-point voltage. To complete the nodal analysis of the two op amp instrumentation circuit, expressions for operational amplifier output stage currents are shown in Equations 1.12 and 1.13:

\[
I_{OA1} = \left( V_{IN}^+ \right) \left( \frac{2}{R_G} + \frac{1}{R_3} \right) + \left( V_{REF} - V_{CM} \right) \left( \frac{2}{R_1} \right)
\]

Eq. 1.12

\[
I_{OA2} = \left( -V_{IN}^+ \right) \left( \frac{2}{R_G} + \frac{1}{R_3} \right) + \left( V_{CM} - V_{REF} \right) \left( \frac{1}{R_4} \right)
\]

Eq. 1.13

Equation 1.12 illustrates that A1's output stage must be able to sink current as a function of the applied differential input voltage and the output reference voltage. On the other hand, A1's output stage is required to source current over the entire input voltage range. In the single-supply case where the circuit is required to sense small differential signals near ground, Eq. 1.6 and Eq. 1.12 both illustrate that A1's output stage is required to sink current while trying to maintain a more negative output voltage than its own negative supply. A1 is thus forced into saturation.

As shown in Eq. 1.13, A2's output stage sources current for positive differential input voltages with no differential or common-mode voltage constraints placed upon its output by Eq. 1.8. Note, however, that as a function of the applied common-mode voltage, A2 is required to sink current. Unfortunately, in the absence of an input signal, Eq. 1.13 shows that A2's output stage may be forced into saturation, trying to sink current while maintaining its output voltage at \( V_{OL} \).

To circumvent the circuit topological and amplifier output voltage limitations, a reference voltage should be used to bias the output of the circuit (A2's output) in the middle of its output voltage swing, and not at exactly one-half the supply voltage:

\[ V_{REF} = \frac{V_{OH(MIN)} + V_{OL(MAX)}}{2} \]

Eq. 1.14

The output reference voltage allows the output stages of A1 and A2 to sink or source current without any output voltage constraints. So long as Eq. 1.11 is used to define to total input voltage range, then amplifier behavior for differential- and common-mode operation is linear. To maximize output signal dynamic range and output SNR, the gain of the instrumentation amplifier circuit should be set according to Eq. 1.15:
Circuit Ga in \( = \frac{V_{OH(MIN)} - V_{OL(MAX)}}{2 \cdot V_{IN(MAX)}} \)  

Eq. 1.15

Under these operating conditions, the differential output voltage of the instrumentation amplifier circuit is now measured relative to \( V_{REF} \) and not to GND. Thus, negative full-scale input signals produce output voltages near A2’s \( V_{OL} \), and positive full-scale signals produce output voltages near A2’s \( V_{OH} \). Therefore, the circuit’s input common-mode range and output dynamic range are optimized in terms of the desired circuit gain and amplifier output voltage characteristics.

For minimal impact of amplifier output load currents on \( V_{OH} \) and \( V_{OL} \), circuit resistor values should be greater than 10kohm in most single-supply applications. Thus, Equations 1.11, 1.14, and 1.15 can all be used to design accurate and repeatable two op amp instrumentation amplifier circuits with single-supply/rail-to-rail operational amplifiers.

One fundamental limitation of the two operational amplifier instrumentation circuit is that since the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths), there will be generally poor AC common-mode rejection without the use of an AC CMR trim capacitor. For optimal AC CMR performance, a trimming capacitor should be connected between the inverting terminal of A1 to ground.

**A TWO OP AMP, FET-INPUT INSTRUMENTATION AMPLIFIER**

Figure 1.9 illustrates a two op amp instrumentation amplifier using the AD822, a dual JFET-input, rail-to-rail output operational amplifier. The output offset voltage is set by \( V_{REF} \).
Dual operational amplifiers, like the AD822, make these types of instrumentation amplifiers both cost- and power-efficient. In fact, when operating on a single, +3 V supply, total circuit power consumption is less than 3.5mW. The AD822’s 2pA bias currents minimize offset errors caused by unbalanced source impedances.

Circuit performance is enhanced dramatically by the use of a matched resistor network. A thin-film resistor array sets the circuit gain to either 10 or 100 through a DPDT (double-pole, double-throw) switch. The array’s resistors are laser-trimmed for a ratio match of 0.01%, and exhibit a maximum differential temperature coefficient of 5ppm/°C. Note that in this application circuit, the fifth gain-setting resistor is not used. The use of this gain trim resistor would introduce serious gain and linearity errors due to the resistance of the double-pole, double-throw switches.

A performance summary and transient response of this instrumentation amplifier is shown in Figure 1.10. Note that the small-signal bandwidth of the circuit is independent of supply voltage, and that the rail-to-rail output pulse response is well-behaved. For greater bandwidth at the expense of higher supply current, the functionally similar AD823 can also be used.
The Three Op Amp Instrumentation Amplifier Topology

For the highest precision and performance, the three op amp instrumentation amplifier topology is optimum for bridge and other offset transducer applications where high accuracy and low nonlinearity are required. This is at the expense of additional power consumption over the two op amp instrumentation circuit (3 amplifiers versus 2 amplifiers). Furthermore, like the two op amp configuration, the input amplifiers can use one dual op amp for tight matching of input offset voltage matching, input bias current, and open-loop gain. Or, a single quad operational amplifier can be used for the whole circuit, including a reference voltage buffer, if required.

Single-supply/rail-to-rail amplifiers can be used in this topology, like that shown for two op amp designs, if the output characteristics of the single-supply/rail-to-rail amplifiers are understood. As shown in Figure 1.11, a generalized, comprehensive analysis of the structure will illustrate the behavior of the nodal voltages and amplifier output currents as functions of the applied common-mode input voltage ($V_{CM}$), the applied differential (signal) voltage ($V_{IN}$), and the output reference voltage ($V_{REF}$). As shown in Eq. 1.16 through 1.27, the nodal analysis was carried out for positive-input differential voltages; because of the symmetry in the circuit, the expressions for the nodal voltages and amplifier output currents carried out for negative-input differential voltages are identical.
Using half-circuit concepts and the principle of superposition, the signal voltage applied to the non-inverting terminal of A1 is set to zero. Since the input signal is applied to the non-inverting terminal of A2, then an expression for the output voltage of amplifier A1 (node A) for positive, differential input signals is given by Eq. 1.16:

$$V_A = (V_{IN} + \left( \frac{R_1}{R_G} \right) + V_{CM}$$  \hspace{1cm} Eq. 1.16

Since the voltage at the inverting input of A1 must equal the voltage at its non-inverting terminal, then an expression for the voltage at amplifier A1’s inverting terminal (node B) is given by Eq. 1.17:

$$V_B = V_{CM}$$  \hspace{1cm} Eq. 1.17

In a similar manner, the voltage at A2’s inverting terminal must equal the voltage on A2’s non-inverting terminal:

$$V_C = V_{IN} + + V_{CM}$$  \hspace{1cm} Eq. 1.18

The expression for the output voltage of A2 (node D) shows that it is dependent upon both the input signal and the applied input common-mode voltage:

$$V_D = (V_{IN} + \left( 1 + \frac{R_2}{R_G} \right) + V_{CM}$$  \hspace{1cm} Eq. 1.19

At this point, it is worth noting the behavior of the nodal voltages of the input amplifiers as functions of the applied differential input voltage and the input common-mode voltage. From Eqs. 1.17 and 1.18, the common-mode component of
the current through the gain setting resistor, $R_G$, is zero – the input stages simply buffer the applied input common-mode voltage. In other words, the input stage common-mode gain is unity.

On the other hand, the full differential input voltage appears across $R_G$. In fact, Eq. 1.16 shows that $A_1$ multiplies and inverts the input differential voltage by a factor of $(-R_1/R_G)$, while Eq. 1.19 shows that $A_2$ multiplies the input voltage by a factor of $(1 + R_1/R_G)$. For the case where the output subtractor stage is configured for a gain of 1, all the differential gain is set in the input stage. Therefore, the ratio of $R_1$ to $R_G$ (or $R_2$ to $R_G$) could be as small as 1:1 or as large as 5000:1. Therefore, to avoid input amplifier output voltage saturation requires an upper and a lower bound be placed on the total input voltage (defined to be common-mode plus differential-mode voltages). These bounds are set by the gain of the instrumentation amplifier and the output high and low voltage limits of the amplifier. The lower bound on the total applied input voltage is given by Eq. 1.20:

$$V_{IN(TOTAL)} > V_{OL(MAX)} + \left(\frac{G-1}{2}\right)V_{IN+}$$  \hspace{1cm} \text{Eq. 1.20}

An upper bound on the total input voltage can be determined in a similar fashion and is also dependent on the circuit gain and the amplifier’s minimum output high voltage:

$$V_{IN(TOTAL)} < V_{OH(MIN)} - \left(\frac{G+1}{2}\right)V_{IN+}$$  \hspace{1cm} \text{Eq. 1.21}

For example, if a rail-to-rail operational amplifier exhibited a $V_{OL(MAX)}$ equal to 10mV and a $V_{OH(MIN)}$ equal to 4.95V, and if the application required a circuit gain of 10 for a 1V full-scale output, then the total input voltage range would be bounded by:

$$0.46 \, V < V_{IN(TOTAL)} < 4.4 \, V$$

Therefore, for the three op amp instrumentation circuit, the total applied input voltage range expressed in terms of circuit gain and amplifier output voltage limits is given by:

$$V_{OL(MAX)} + \left(\frac{G-1}{2}\right)V_{IN+} < V_{IN(TOTAL)} < V_{OH(MIN)} - \left(\frac{G+1}{2}\right)V_{IN+}$$  \hspace{1cm} \text{Eq. 1.22}
Since the non-inverting input of the subtractor amplifier A3 determines the voltage on its inverting terminal, an expression for the voltages at Nodes E and F is given by Eq. 1.23:

\[
V_E = V_F = (V_{IN} + \frac{R_6}{R_4 + R_6}(1 + \frac{R_2}{R_G}) + V_{CM}\frac{R_6}{R_4 + R_6}) + V_{REF}\frac{R_4}{R_4 + R_6}
\]

Eq. 1.23

For the case where R3, R4, R5, and R6 are all equal to R (typically the case for instrumentation amplifier gains greater than or equal to 1), then these nodal voltages will set up at one-half the applied output voltage reference (V_{REF}) and at one-half the applied input common-mode voltage (V_{CM}). Furthermore, the component due to the amplified differential input signal is also attenuated by a factor of two. Finally, Eq. 1.24 shows an expression for the circuit’s output voltage in its familiar form for R4 = R3 and R6 = R5:

\[
V_{OUT} = (V_{IN} + \frac{R_5}{R_3}(1 + \frac{2R_1}{R_G}) + V_{REF}
\]

Eq. 1.24

From Eq. 1.24, the circuit output voltage is only a function of the amplified input differential voltage and the output reference voltage. Provided that R4 = R3 and R6 = R5, the component of the output voltage due to the applied input common-mode voltage is completely suppressed. The only remaining error voltage is that due to the finite CMR of A3 and the ratio match of R3 to R5 and R4 to R6. Also, in the absence of either an input signal or an output reference voltage, A3’s output voltage is equal to zero; in a single-supply application where rail-to-rail output amplifiers are used, it is equal to V_{OL}.

To complete the analysis of this instrumentation circuit, expressions for operational amplifier output stage currents have been developed and are shown in Eqs. 1.25 through 1.27:

\[
I_{OA1} = \left(\frac{V_{IN}}{R_3}\right)\left(\frac{R_1}{R_G}\right)(1 + \frac{R_3}{R_1}) + \left(1 + \frac{R_2}{R_G}\right)\frac{R_4}{R_4 + R_6} + \frac{V_{REF} - V_{CM}}{R_3}\frac{R_4}{R_4 + R_6}
\]

Eq. 1.25

\[
I_{OA2} = (-V_{IN} +)\left[\left(1 + \frac{R_2}{R_G}\right)\frac{1}{R_2} + \frac{1}{R_4} - \frac{1}{R_4}\frac{R_6}{R_4 + R_6}\right] - \left(\frac{1}{R_2}\right) + \frac{V_{REF} - V_{CM}}{R_4 + R_6}
\]

Eq. 1.26
Recall in the analysis of the two-amplifier instrumentation circuit that amplifier output stage currents were defined to be positive, if current flow is into the device, the amplifier is sinking current. Conversely, if the nodal analysis shows that output currents are negative quantities, then current flow is out of the amplifier, and the amplifier is sourcing current.

Equation 1.25 illustrates that A1's output stage must be able to sink current as a function of the applied differential input voltage and the output reference voltage. On the other hand, A1's output stage is required to source current throughout the applied common-mode voltage. In the single-supply case where the circuit is required to sense small differential signals near ground, Eq. 1.16 and Eq. 1.25 both illustrate that A1's output stage is required to sink current while trying to maintain a more negative output voltage than its own negative supply. A1 cannot sustain this operating point, and thus is forced into output saturation.

As shown in Eq. 1.26, A2's output stage sources current for positive input signal voltages with no differential nor common-mode voltage constraints placed upon its output by Eq. 1.19. A3's output stage is also required to source current around its feedback resistor as a function of the positive input differential voltage. Note, however, that as a function of the applied common-mode voltage, it is required to sink current. Unfortunately Eq. 1.24 showed that in the absence of an input signal, A3's output stage can be forced into saturation, trying to sink current while maintaining its output voltage at A3's \( \text{V}_{OL} \).

To circumvent circuit topological and amplifier output voltage limitations, the results shown in Eq. 1.14 and Eq. 1.15 for the two op amp instrumentation circuit apply equally well here. The output reference voltage is chosen in the middle of A1 and A2's output voltage swing:

\[
\text{V}_{REF} = \frac{\text{V}_{OH(MIN)} + \text{V}_{OL(MAX)}}{2}
\]

Eq. 1.14

Similarly, output signal dynamic range and output SNR are maximized if the gain of the instrumentation circuit is set according to Eq. 1.15:

\[
\text{Circuit Gain} = \frac{\text{V}_{OH(MIN)} - \text{V}_{OL(MAX)}}{2 \cdot \text{Vin(MAX)}}
\]

Eq. 1.15

Under these operating conditions, the differential output voltage of the instrumentation amplifier circuit is now measured relative to \( \text{V}_{REF} \) and not to GND. Thus, negative full-scale input signals yield output voltages near A3's \( \text{V}_{OL} \), and positive full-scale signals produce output voltages near A3's \( \text{V}_{OH} \). Thus, circuit input common-mode range and output dynamic range are optimized in terms of the desired circuit gain and amplifier output voltage characteristics.
For minimal impact on $V_{OH}$ and $V_{OL}$ due to amplifier output load currents, circuit resistor values should be greater than 10kohm in single-supply applications. Thus, Equations 1.22, 1.14, and 1.15 can all be used to design accurate and repeatable three op amp instrumentation amplifier circuits with single-supply/rail-to-rail operational amplifiers.

**A COMPOSITE, SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER [3]**

As it has been shown throughout this chapter, operation of high performance linear circuits from a single, low-voltage supply (5V or less) is a common requirement. While there are many precision single supply operational amplifiers (some rail-rail), such as the OP213, the OP291, and the OP284, and some good single-supply instrumentation amplifiers, such as the AMP04 and the AD626 (both covered later), the highest performance instrumentation amplifiers are still specified for dual-supply operation.

One way to achieve both high precision and single-supply operation takes advantage of the fact that several popular transducers (e.g. strain gauges) provide an output signal centered around the (approximate) mid-point of the supply voltage (or the reference voltage), where the inputs of the signal conditioning amplifier need not operate near “ground” or the positive supply voltage.

Under these conditions, a dual-supply instrumentation amplifier referenced to the supply mid-point followed by a “rail-to-rail” operational amplifier gain stage provides very high DC precision. Figure 1.12 illustrates one such high-performance instrumentation amplifier operating on a single, +5V supply. This circuit uses an AD620 low-cost precision instrumentation amplifier for the input stage, and an AD822 JFET-input dual rail-to-rail output operational amplifier for the output stage.

![A Precision Single-Supply Instrumentation Amplifier With Rail-to-Rail Output](Figure 1.12)
In this circuit, R1 and R2 form a voltage divider which splits the supply voltage in half to +2.5V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of an AD822 which buffers it and provides a low-impedance source needed to drive the AD620’s output reference port. The AD620’s REFERENCE input has a 10kohm input resistance and an input signal current of up to 200µA. The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output ±2.5V, “rail-to-rail,” with only ±0.83V required of the AD620. This output voltage level of the AD620 is well within the AD620’s capability, thus ensuring high linearity for the “dual-supply” front end. Note that the final output voltage must be measured with respect to the +2.5V reference, and not to GND.

The general gain expression for this composite instrumentation amplifier is the product of the AD620 and the inverting amplifier gains:

\[
\text{GAIN} = \left(\frac{49.4k\Omega}{R_G} + 1\right) \left(\frac{R_F}{R_I}\right) \quad \text{Eq. 1.28}
\]

For this example, an overall gain of 10 is realized with \(R_G = 21.5k\Omega\) (closest standard value). The table (Figure 1.13) summarizes various \(R_G\)/gain values.

In this application, the total input voltage applied to the inputs of the AD620 can be up to +3.5V with no loss in precision. For example, at an overall circuit gain of 10, the common-mode input voltage range spans 2.25V to 3.25V, allowing room for the ±0.25V full-scale differential input voltage required to drive the output ±2.5V about \(V_{\text{REF}}\).

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the buffer’s feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100kHz for gain configurations up to 300. Figure 1.13 summarizes the performance of this composite instrumentation amplifier. To reduce the effects of unwanted noise pickup, a capacitor is recommended across A2’s feedback resistance to limit the circuit bandwidth to the frequencies of interest. Also, to prevent the effects of input-stage rectification, an optional 1kHz filter is recommended at the inputs of the AD620.
PERFORMANCE SUMMARY OF THE +5V SINGLE-SUPPLY 
AD620/AD822 COMPOSITE INSTRUMENTATION AMP 
WITH RAIL-TO-RAIL OUTPUTS

<table>
<thead>
<tr>
<th>CIRCUIT</th>
<th>R_G</th>
<th>Vos, RTI</th>
<th>TCVos, RTI</th>
<th>Nonlinearity*</th>
<th>Bandwidth**</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>21.5k</td>
<td>1000</td>
<td>4.5</td>
<td>&lt;0.005%</td>
<td>600</td>
</tr>
<tr>
<td>30</td>
<td>5.49k</td>
<td>430</td>
<td>1.5</td>
<td>&lt;0.005%</td>
<td>600</td>
</tr>
<tr>
<td>100</td>
<td>1.53k</td>
<td>215</td>
<td>1.4</td>
<td>&lt;0.005%</td>
<td>300</td>
</tr>
<tr>
<td>300</td>
<td>499</td>
<td>150</td>
<td>1.1</td>
<td>&lt;0.005%</td>
<td>120</td>
</tr>
<tr>
<td>1000</td>
<td>149</td>
<td>150</td>
<td>1.0</td>
<td>&lt;0.005%</td>
<td>30</td>
</tr>
</tbody>
</table>

*Nonlinearity measured over the output voltage range: 0.1V < VOUT < 4.90V
**Bandwidth measured with no input filter and no 10Hz noise filter

- Input bias current (2mA, max) must have DC return path to power supply
- Total V_IN (CM + DM) = V_IN,CM + \frac{V_IN,DM}{2}

Figure 1.13

LOW-SIDE AND HIGH-SIDE SIGNAL CONDITIONING

As previous discussions have shown, single-supply and rail-to-rail operational amplifiers in two and three op amp instrumentation amplifier circuits impose certain limits on the usable input common-mode and output voltage ranges of the circuit. There are, however, many single-supply applications where low- and high-side signal conditioning is required. For these applications, novel circuit design techniques allow sensing of very small differential signals at GND or at VPOS. Two such devices, the AMP04 and AD626, have been designed specifically for these applications.

As illustrated in Figure 1.14, the AMP04, a single-supply instrumentation amplifier, uses a inverting-mode output gain architecture, where an external resistor, R_G (connected between the AMP04’s Pins 1 and 8), is used as the input resistor to A4, and an internal 100kohm thin-film resistor, R1, serves as the output amplifier’s feedback resistance. Unity-gain input buffers A1 and A2 both serve two functions: they present a high impedance to the source, and provide a DC level shift to the applied common-mode input voltage of one V_BE for amplifiers A3 and A4. As a result, their output stages can operate very close the negative supply without saturating.

The input buffers are designed with PNP transistors that allow the applied common-mode voltage range to extend to 0V. In fact, the usable input common-mode voltage range of the AMP04 actually extends 0.25V below the negative supply (although not guaranteed, applied input voltages to any integrated circuit should always remain within its total supply voltage range). On the other hand, since the input buffers are PNP stages, the input common-mode voltage range does not include the AMP04’s positive supply voltage. When the inputs are driven within 1V of the positive rail,
the PNP input transistors are forced into cutoff; and, as a result, input offset voltages and bias currents increase, and CMR degrades.

**SINGLE SUPPLY INSTRUMENTATION AMP HANDLES ZERO-VOLTS INPUT AND ZERO-VOLTS OUTPUT (AMP04)**

A pulsed-bridge transducer-driver/amplifier illustrates the utility of this low-power, single-supply instrumentation amplifier circuit as shown in Figure 1.15. Commonly available 350ohm strain-gauge bridges are difficult to apply in low-voltage, low-power systems for a number of reasons, including the requirements for high bridge drive currents and high sensitivity. For low-speed measurements, power limitations can be overcome by operating the bridge in a pulsed-power mode, reading the amplified output on a low-speed, low-duty-cycle basis.
A LOW POWER, PULSED LOAD CELL BRIDGE AMPLIFIER

In this circuit, an externally generated 800µs TTL/CMOS pulse is applied to the SHUTDOWN input to the REF195, a +5V precision voltage reference. The REF195’s shutdown feature is used to switch between a normal +5V DC output if left open (or at logic HIGH), and a low-power-down standby state (5µA maximum current drain) with the shutdown pin held low. The switched 5V output from the REF195 drives the bridge and supplies power to the AMP04. The AMP04 is programmed for a gain of 20 by the 4.99kohm resistor, which should be a stable film type (TCR = 50ppm/°C or better) in close physical proximity to the amplifier. Dynamic performance of the circuit is excellent, because the AMP04’s output settles to within 0.5mV of its final value in about 230µs (not shown).

This approach allows fast measurement speed with a minimum standby power. Generally speaking, with all active circuitry essentially being switched by the measurement pulse, the average current drain of this circuit is determined by its duty cycle. On-state current drain is about 15mA from the 6V battery during the measurement interval (90mW peak power). Therefore, an 800µs measurement strobe once per second will dissipate an average of 72µW, to which is added the 30µW standby power of the REF195. In any event, overall operation is enhanced by the REF195’s low-dropout regulation characteristics. The REF195 can operate with supply voltages as low as +5.4 V and still maintain +5V output operation.

If low-frequency filtering is desired, an optional capacitor can be connected between pins 6 and 8 of the AMP04. However, a much longer strobe pulse must be used so that the filter can settle to the circuit’s required accuracy. For example, if a 0.1µF capacitor is used for noise filtering, then the R-C time constant formed with the AMP04’s internal 100kohm resistor is 10ms. Therefore, for a 10-bit settling criterion, 6.9 time constants, or 70ms, should be allowed. Obviously, this will place greater demands upon system power, so trade-offs may be necessary in the amount of filtering used.
Of course, the amplified bridge output appears only during the measurement interval, and is valid after 220µs unless filtering is used. During this time, a sampled-input ADC (analog-to-digital converter) reads \( V_{\text{OUT}} \), eliminating the need for a dedicated sample-and-hold circuit to retain the output voltage. If 10-bit measurements are sufficient, the 5V bridge drive can also be assumed to be constant (for 10-bit accuracy), because the REF195 exhibits a ±1mV (±0.02 %) output voltage tolerance. For more accurate measurements, a ratiometric reading of the bridge status can be obtained by reading the bridge drive (\( V_{\text{REF}} \)) as well as \( V_{\text{OUT}} \).

On the other hand, single-supply instrumentation amplifiers, like the AD626, shown in Figure 1.16, exhibit an input stage architecture that allows the sensing of small differential input signals, not only at its positive supply, but beyond it as well. The AD626 is a differential amplifier consisting of a precision balanced attenuator, a very low-drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages, without the use of any other external active or passive components.

**AD626 SCHEMATIC ILLUSTRATES INPUT PROTECTION AND SCALING RESISTORS AND ALLOWS INPUT COMMON MODE VOLTAGE UP TO 6 \times (V_s - 1V)**

![AD626 Schematic](image)

Figure 1.16

The simplified equivalent circuit in Figure 1.16 illustrates the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to the dual resistive attenuators R1 through R4, whose purpose is to reduce the peak common-mode voltage at the inputs of A1. This allows the applied differential voltage to be accurately amplified in the presence of large common-mode voltages six times greater than that which can be tolerated by the actual input to A1. As a result, input common-mode rejection extends to 6\( \times \)\((V_s - 1V)\). The overall common-mode error is minimized by precise laser trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio (CMRR) of at least 10,000:1 (80dB).
To minimize the effect of spurious RF signals at the inputs due to rectification at the inputs to A1, small filter capacitors C1 and C2, internal to the AD626, limit the input bandwidth to 1MHz.

The output of A1 is connected to the input of A2 via a 100kohm resistor (R12) to allow the low-pass filtering to the signals of interest. To use this feature, a capacitor is connected between Pin 4 and the circuit’s common. Equation 1.29 can be used to determine the value of the capacitor, based on the corner frequency of this low-pass filter:

$$C_{LP} = \frac{1}{2\pi \cdot (100 \text{ k}\Omega) \cdot f_{LP}} \quad \text{Eq. 1.29}$$

where $f_{LP}$ = the desired corner frequency of the low-pass filter, in Hz.

The 200kohm input impedance of the AD626 requires that the source resistance driving this amplifier should be less than 1kohm to minimize gain error. Also, any mismatch between the total source resistance of either input will affect gain accuracy and common-mode rejection. For example, when operating at a gain of 10, an 80ohm mismatch in the source resistance between the inputs will degrade circuit CMR to 68dB.

Output amplifier, A2, operates at a gain of 2 or 20, thus setting the overall, precalibrated gain of the AD626 (with no external components) at 10 or 100. The gain is set by the feedback network around amplifier A2.

The output of A2 uses an internal 10kohm resistor to $-V_S$ to “pull down” its output. In single-supply applications where $-V_S$ equals GND, A2’s output can drive a 10kohm ground-referenced load to at least +4.7V. The minimum nominal “zero” output voltage of the AD626 is 30mV.

If pin 7 is left unconnected, the gain of the AD626 is 10. By connecting pin 7 to GND, the AD626’s gain can be set to 100. To adjust the gain of the AD626 for gains between 10 and 100, a variable resistance network can be used between pin 7 and GND. This variable resistance network includes a fixed resistor with a rheostat-connected potentiometer in series. The interested reader should consult the AD626 data sheet for complete details for adjusting the gain of the AD626. For these applications, a $\pm 20\%$ adjustment range in the gain is required. This is due to the on-chip resistors absolute tolerance of 20% (these resistors, however, are ratio-matched to within 0.1%).

An example of the AD626 high-side sensing capabilities, Figure 1.17 illustrates a typical current sensor interface amplifier. The signal current is sensed across the current shunt, $R_S$. For reasons mentioned earlier, the value of the current shunt should be less than 1ohm and should be selected so that the average differential voltage across this resistor is typically 100mV. To generate a full-scale output voltage of +4V, the AD626 is configured in a gain of 40. To accommodate the tolerance in the current shunt, the variable gain-setting resistor network shown in
the circuit has an adjustment range of ±20%. Note that sufficient headroom exists in the gain trim to allow at least a 10% overrange (+4.4V).

**AD626 HIGH-SIDE CURRENT MONITOR INTERFACE**

![DIAGRAM]

**Figure 1.17**

**INSTRUMENTATION AMPLIFIER INPUT-STAGE RECTIFICATION**

A well-known phenomenon in analog integrated circuits is RF rectification, particularly in instrumentation amplifiers and operational amplifiers. While amplifying very small signals, these devices can rectify unwanted high-frequency, out-of-band signals. The results are DC errors at the output in addition to the wanted sensor signal. Unwanted out-of-band signals enter sensitive circuits through the circuit’s conductors which provide a direct path for interference to couple into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling. Regardless of the type of interference, the unwanted signal is a voltage which appears in series with the inputs.

All instrumentation and operational amplifier input stages are either emitter-coupled (BJT) or source-coupled (FET) differential pairs with resistive or current-source loading. Depending on the quiescent current level in the devices and the frequency of the interference, these differential pairs can behave as high-frequency detectors. As it has been shown in [1], this detection process produces spectral components at the harmonics of the interference as well at DC. It is the DC component that shifts internal bias levels of the input stages causing errors, which can lead to system inaccuracies. For a complete treatment of this issue, including analytical and empirical results, the interested reader should consult Reference [1].

Since it is required to prevent unwanted signals and noise from entering the input stages, input filtering techniques are used for these types of devices. As illustrated in Reference [1], this technique uses an equivalent approach suggested for operational amplifiers. As shown in Figure 1.18, low-pass filters are used in series...
with the differential inputs to prevent unwanted noise from reaching the inputs. Here, capacitors, $C_{X1}$, $C_{X2}$, and $C_{X3}$, connected across the inputs of the instrumentation amplifier, form common-mode ($C_{X1}$ and $C_{X2}$) and differential-mode ($C_{X3}$) low-pass filters with the two resistors, $R_X$. Time constants $R_X-C_{X1}$ and $R_X-C_{X2}$ should be well-matched (1% or better), because imbalances in these impedances can generate a differential error voltage which will be amplified.

On the other hand, an additional benefit of using a differentially-connected capacitor is that it can reduce common-mode capacitive imbalance. This differential connection helps to preserve high-frequency AC common-mode rejection. Since series resistors are required to form the low-pass filter, errors due to poor layout (CMR imbalance), component tolerance of $R_X$ (input bias current-induced offset voltage) and resistor thermal noise must be considered in the design process. In applications where the sensor is an RTD or a resistive strain gauge, $R_X$ can be omitted, provided the sensor is close to the amplifier.

![Diagram](external_common-mode_and_differential-mode_input_filters_prevent_rfi_rectification_in_instrumentation_amplifier_circuits.png)

**Figure 1.18**
REFERENCES


SECTION 2
HIGH SPEED OP AMPS

- Driving Capacitive Loads
- Cable Driving
- Single-Supply Considerations
- Application Circuits
SECTION 2

HIGH SPEED OP AMPS

Walt Jung and Walt Kester

Modern system design increasingly makes use of high speed ICs as circuit building blocks. With bandwidths going up and up, demands are placed on the designer for faster and more power efficient circuits. The default high speed amplifier has changed over the years, with high speed complementary bipolar (CB) process ICs such as the AD846 and AD847 in use just about ten years at this writing. During this time, the general utility/availability of these and other ICs have raised the “high speed” common performance denominator to 50MHz. The most recent extended frequency complementary bipolar (XFCB) process high speed devices such as the AD8001/AD8002, the AD9631/9632 and the AD8036/AD8037 now extend the operating range into the UHF region.

Of course, a traditional performance barrier has been speed, or perhaps more accurately, painless speed. While fast IC amplifiers have been around for some time, until more recently they simply haven’t been the easiest to use. As an example, devices with substantial speed increases over 741/301A era types, namely the 318-family, did so at the expense of relatively poor settling and capacitive loading characteristics. Modern CB process parts like the AD84X series provide far greater speed, faster settling, and do so at low user cost. Still, the application of high performance fast amplifiers is never entirely a cookbook process, so designers still need to be wary of many inter-related key issues. This includes not just the amplifier selection, but also control of parasitics and other potentially performance-limiting details in the surrounding circuit.

It is worth underscoring that reasons for the “speed revolution” lie not just in affordability of the new high speed ICs, but is also rooted in their ease of use. Compared to earlier high speed ICs, CB process devices are generally more stable with capacitive loads (with higher phase margins in general), have lower DC errors, consume less power for a given speed, and are all around more “user friendly”. Taking this a step further, XFCB family devices, which extend the utility of the op amp to literally hundreds of MHz, are understandably less straightforward in terms of their application (as is any amplifier operating over such a range). Thus, getting the most from these modern devices definitely stresses the “total environment” aspects of design.

Another major ease of use feature found in today’s linear ICs is a much wider range of supply voltage characterization. While the older ±15V standard is still much in use, there is a trend towards including more performance data at popular lower voltages, such as ±5V, or +5V only, single supply operation. The most recent devices using the lower voltage XFCB process use supply voltages of either ±5V, or simply +5V only. The trend towards lower supply voltages is unmistakable, with a goal of squeezing the highest performance from a given voltage/power circuit environment. These “ease of use” design aspects with current ICs are illustrated in this chapter,
along with parasitic issues, optimizing performance over supply ranges, and low
distortion stages in a variety of applications.

**DRIVING CAPACITIVE LOADS**

From system and signal fidelity points of view, transmission line coupling between
stages is best, and is described in some detail in the next section. However, complete
transmission line system design may not always be possible or practical. In addition,
various other parasitic issues need careful consideration in high performance
designs. One such problem parasitic is amplifier load capacitance, which potentially
comes into play for all wide bandwidth situations which do not use transmission line
signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap
loading) effects should *always* be considered. This is because PC board capacitance
can build up quickly, especially for wide and long signal runs over ground planes
insulated by thin, higher K dielectric. For example, a 0.025” PC trace using a G-10
dielectric of 0.03” over a ground plane will run about 22pF/foot (Reference 1). Even
relatively small load capacitance (i.e., <100 pF) can be troublesome, since while not
causing outright oscillation, it can still stretch amplifier settling time to greater
than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply
detrimental, they are actually an anathema to high quality signals. However, before-
the-fact designer knowledge still allows high circuit performance, by employing
various tricks of the trade to combat the capacitive loading. If it is not driven via a
transmission line, remote signal circuitry should be checked for capacitive loading
very carefully, and characterized as best possible. Drivers which face poorly defined
load capacitance should be bullet-proofed accordingly with an appropriate design
technique from the options list below.

Short of a true matched transmission line system, a number of ways exist to drive a
load which is capacitive in nature while maintaining amplifier stability.

*Custom capacitive load (cap load) compensation, includes two possible options,
  namely a); overcompensation, and b); an intentionally forced-high loop noise gain
  allowing crossover in a stable region. Both of these steps can be effective in special
  situations, as they reduce the amplifier’s effective closed loop bandwidth, so as to
  restore stability in the presence of cap loading.*

*Overcompensation* of the amplifier, when possible, reduces amplifier bandwidth so
that the additional load capacitance no longer represents a danger to phase margin.
As a practical matter however, amplifier compensation nodes to allow this are
available on few high speed amplifiers. One such useful example is the AD829,
compensated by a single capacitor at pin 5. In general, almost any amplifier using
external compensation can always be over compensated to reduce bandwidth. This
will restore stability against cap loads, by lowering the amplifier’s unity gain
frequency.
CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY

Forcing a high noise gain, is shown in Figure 2.1, where the capacitively loaded amplifier with a noise gain of unity at the left is seen to be unstable, due to a 1/β - open loop rolloff intersection on the Bode diagram in an unstable −12dB/octave region. For such a case, quite often stability can be restored by introducing a higher noise gain to the stage, so that the intersection then occurs in a stable −6dB/octave region, as depicted at the diagram right Bode plot.

RAISING NOISE GAIN (DC OR AC) FOR FOLLOWER OR INVERTER STABILITY

To enable a higher noise gain (which does not necessarily need to be the same as the stage’s signal gain), use is made of resistive or RC pads at the amplifier input, as in Figure 2.2. This trick is more broad in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally allows use with any amplifier setup, even voltage followers. The technique adds an extra resistor Rp, which works against Rf to force the noise gain of the stage to a level appreciably higher than the signal gain (which is unity in both cases here). Assuming that CL is a value which produces a parasitic pole near the amplifier’s natural crossover, this loading combination would likely lead to oscillation due to the
excessive phase lag. However with RD connected, the higher amplifier noise gain produces a new 1/ß - open loop rolloff intersection, about a decade lower in frequency. This is set low enough that the extra phase lag from CL is no longer a problem, and amplifier stability is restored.

A drawback to this trick is that the DC offset and input noise of the amplifier are raised by the value of the noise gain, when the optional CD is not present. But, when CD is used in series with RD, the offset voltage of the amplifier is not raised, and the gained-up AC noise components are confined to a frequency region above 1/(2π•RD•CD). A further caution is that the technique can be somewhat tricky when separating these operating DC and AC regions, and should be applied carefully with regard to settling time (Reference 2). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

“Passive” cap load compensation, shown in Figure 2.3, is the most simple (and most popular) isolation technique available. It uses a simple “out-of-the-loop” series resistor RX to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR AD811 CURRENT FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 13.5 MHz)

As noted, this technique can be applied to virtually any amplifier, which is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor, RX. This resistor’s minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.
Drawbacks of this approach are the loss of bandwidth as $R_X$ works against $C_L$, the loss of voltage swing, a possible lower slew rate limit due to $I_{MAX}$ and $C_L$, and a gain error due to the $R_X$-$R_L$ division. The gain error can be optionally compensated with $R_{IN}$, which is ratioed to $R_F$ as $R_L$ is to $R_X$. In this example, a ±100mA output from the op amp into $C_L$ can slew $V_{OUT}$ at a rate of 100V/µs, far below the intrinsic AD811 slew rate of 2500V/µs. Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier is not otherwise protected, then an $R_X$ resistor of 50-100ohms should be used with virtually any amplifier facing capacitive loading. Although a non-inverting amplifier is shown, the technique is equally applicable to inverter stages.

With very speed high amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type problem. In such cases the amplifier must be stable driving the capacitance, but it must also preserve its best bandwidth and settling time characteristics. To address this type of cap load case performance, $R_S$ and $C_L$ data for a specified settling time is most appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance, which in combination with $C_L$ causes peaking or even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device $f_t$, the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

In general, a small damping resistor ($R_S$) placed in series with $C_L$ will help restore the desired response (see Figure 2.4). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simply stability or an acceptable amount of peaking has been used, but a more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of $R_S$ - $C_L$ curves exists, such as those of Figure 2.4. These data will aid in selecting $R_S$ for a given application.
The basic shape of this curve can be easily explained. When \( C_L \) is very small, no resistor is necessary. When \( C_L \) increases to some threshold value an \( R_S \) becomes necessary. Since the frequency at which the damping is required is related to the \( R_S \cdot C_L \) time constant, the \( R_S \) needed will initially increase rapidly from zero, and then will decrease as \( C_L \) is increased further. A relatively strict requirement, such as for 0.1%, settling will generally require a larger \( R_S \) for a given \( C_L \), giving a curve falling higher (in terms of \( R_S \)) than that for a less stringent requirement, such as 20% overshoot. For the common gain condition of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed loop gains lessen the problem dramatically, and will require less \( R_S \) for the same performance. The third (lower-most) curve illustrates this, demonstrating a closed loop gain of 10 \( R_S \) requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 2.2.

The recommended values for \( R_S \) will optimize response, but it is important to note that generally \( C_L \) will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large \( R_S \cdot C_L \) time constant will dominate the response. In any given application, the value for \( R_S \) should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

Active or "in-the-loop" cap load compensation can also be used as shown in Figure 2.5, and this scheme modifies the passive configuration to provide feedback correction for the DC & low frequency gain error associated with \( R_X \). In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers don’t allow the integrating connection of \( C_F \).
ACTIVE “IN-LOOP” CAPACITIVE LOAD COMPENSATION CORRECTS FOR DC AND LF GAIN ERRORS

![Circuit Diagram]

Figure 2.5

This circuit returns the DC feedback from the output side of isolation resistor Rx, thus correcting for errors. AC feedback is returned via CF, which bypasses Rx/Rf at high frequencies. With an appropriate value of CF (which varies with CL for fixed resistances) this stage can be adjusted for a well damped transient response (Reference 2,3). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the DC errors can be very low. A drawback is the need to tune CF to CL as even if this is done well initially, any change to CL will alter the response away from flat. The circuit as shown is useful for voltage feedback amplifiers only, because capacitor CF provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of RIN.

Internal cap load compensation involves the use of an amplifier which internally has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.
The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 2.6, a simplified diagram of an amplifier with internal cap load compensation, shows how it works. The cap load compensation is the $C_F$ -resistor network shown around the unity gain output stage of the amplifier - note that the dotted connection of this network underscores the fact that it only makes its presence felt for certain load conditions.

Under normal (non-capacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the $C_F$ network then sees a relatively small voltage drop, and has little or no effect on the amplifier’s high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the $C_F$ network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner which is adaptive to the external capacitance, $C_L$.

As a point of reference, note that it requires 6.3mA peak to support a 2Vp-p swing across a 100pF load at 10MHz.

Since this mechanism is resident in the amplifier output stage and it affects the overall compensation characteristics dynamically, it acts independent of the specific
feedback hookup, as well as size of the external cap loading. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make it work (other than selecting an IC which employs it). Some amplifiers using internal cap load compensation are the AD847 and the AD817, and their dual equivalents, AD827 and AD826.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the C_p network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits for lower-level outputs.

**RESPONSE OF INTERNAL CAP LOAD COMPENSATED AMPLIFIER VARIES WITH SIGNAL LEVEL**

The dynamic nature of this internal cap load compensation is illustrated in Figure 2.7, which shows an AD817 unity gain inverter being exercised at both high and low output levels, with common conditions of \( V_s = \pm 15V \), \( R_L = 1\, \text{k}\Omega \), \( C_L = 1\, \text{nF} \), and using \( 1\, \text{k}\Omega \) input/feedback resistors. In both photos the input signal is on the top trace and the output signal is on the bottom trace, and the time scale is fixed. In the 10\,\text{Vp-p} output (A) photo at the left, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. This indicates that for this high level case, the bandwidth reduction due to \( C_L \) is most effective. However, in the (B) photo at the right, the 200\,\text{mVp-p} output shows greater overshoot and ringing, for the lower level signal. The point is made that, to some degree at least, the relative cap load immunity of this type of internally cap load compensated amplifier is signal dependent.

![Figure 2.7](image_url)
Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion and load drive ability, and these factors influence amplifier performance in video applications. Though the network's presence does not by any means make devices like the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase which are achievable with otherwise comparable amplifiers (for example, the AD818).

While the individual techniques for countering cap loading outlined above have various specific tradeoffs as noted, all of the techniques have a serious common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, then a matched transmission line system is the solution, and is discussed in more detail later in the chapter. As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem- just pick the right amplifier and forget about it. And indeed, that would seem the “panacea” solution for all cap load situations - if you use the “right” amplifier you never need to think about cap loading again. Could there be more to it?

Yes! The “gotcha” of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, without the CFP-resistor network. Like the old saying about no free lunches, if you care about attaining top-notch levels of high frequency AC performance, you should give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier could be a good choice. Such amplifiers are certainly easier to use, and relatively forgiving about loading issues. Some applications of this chapter illustrate the distortion point specifically, quoting performance in a driver circuit with/without the use of an internal cap load compensated amplifiers.

With increased gain bandwidths of greater than or equal to 100MHz available in today’s ICs, layout, grounding and the control of parasitics become much, much more important. In fact, with the fastest available ICs such as the XFCB types, these issues simply cannot be ignored, they are critical and must be addressed for stable performance. All high frequency designs can profit from the use of low parasitic construction techniques, such as described in Chapter 9. In the circuit discussions which follow, similar methods should be used for best results, and in the very high frequency circuits (greater than 100MHz) it is mandatory. Some common pitfalls are covered before getting into specific circuit examples.

As with all wide bandwidth components, good PC board layout is critical to obtain the best dynamic performance with these high speed amplifiers. The ground plane in the area of the op amp and its associated components should cover as much of the component side of the board as possible (or first interior ground layer of a multilayer board).
The ground plane should be removed in the area of the amplifier inputs and the feedback and gain set resistors to minimize stray capacitance at the input. Each power supply trace should be decoupled close to the package with a minimum of 0.1µF ceramic (preferably surface mount), plus a 6.8µF or larger tantalum capacitor within 0.5”, as a charge storage reservoir when delivering high peak currents (line drivers, for example). Optionally, larger value conventional electrolytic can be used in place of the tantalum types, if they have a low ESR.

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors (buffed metal film rather than laser-trimmed spiral-wound) and/or carbon resistors.

Microstrip techniques should be used for all input and output lead lengths in excess of one inch (Reference 1). Sockets should be avoided if at all possible because of their parasitic capacitance and inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray capacitance and inductance than molded socket assemblies.

The effects of inadequate decoupling on harmonic distortion performance are dramatically illustrated in Figure 2.8. The left photo shows the spectral output of the AD9631 op amp driving a 100ohm load with proper decoupling (output signal is 20MHz, 2V p-p). Notice that the second harmonic distortion at 40MHz is approximately –70dBc. If the decoupling is removed, the distortion is increased, as shown in the right photo of the same figure. Figure 2.8 (right-hand photo) also shows stray RF pickup in the wiring connecting the power supply to the op amp test fixture. Unlike lower frequency amplifiers, the power supply rejection ratio of many high frequency amplifiers is generally fairly poor at high frequencies. For example, at 20MHz, the power supply rejection ratio of the AD9631 is less than 25dB. This is the primary reason for the degradation in performance with inadequate decoupling. The change in output signal produces a corresponding signal-dependent load current change. The corresponding change in power supply voltage due to inadequate decoupling produces a signal-dependent error in the output which manifests itself as an increase in distortion.
Inadequate decoupling can also severely affect the pulse response of high speed amplifiers such as the AD9631. Figure 2.9 shows normal operation and the effects of removing all decoupling capacitors on the AD9631 in its evaluation board. Notice the severe ringing on the pulse response for the poorly decoupled condition, in the right photo. A Tektronix 644A, 500MHz digitizing oscilloscope was used to make the measurement (as well as the pulse responses in Figure 2.10, 2.14, 2.15, 2.16, and 2.17).

The effects of stray parasitic capacitance on the inverting input of such high speed op amps as the AD8001 is shown in Figure 2.10. In this example, 10pF was connected to the inverting input, and the overshoot and ringing increased significantly. (The AD8001 was configured in the inverting mode with a gain of −1, and the feedback and feedforward resistors were equal to 649ohms). In some cases,
low-amplitude oscillation may occur at frequencies of several hundred megahertz when there is significant stray capacitance on the inverting input. Unfortunately, you may never actually observe it unless you have a scope or spectrum analyzer which has sufficient bandwidth. Unwanted oscillations at RF frequencies will probably be rectified and averaged by devices to which the oscillating signal is applied. This is referred to as RF rectification and will create small unexplained dc offsets which may even be a function of moving your hand over the PC board. It is absolutely essential when building circuits using high frequency components to have high bandwidth test equipment and use it to check for oscillation at frequencies well beyond the signals of interest.

**EFFECT OF 10pF STRAY INVERTING INPUT CAPACITANCE ON PULSE RESPONSE OF AD8001 OP AMP**

![Figure 2.10](image)

Many of these problems occur in the prototype phase due to a disregard for high frequency layout and decoupling techniques. The solutions to them lie in rigorous attention to such details as above, and those described in Chapter 9.

**CABLE DRIVING**

For a number of good reasons, wide bandwidth amplifier systems traditionally use transmission line interconnections, such as that shown in the basic diagram of Figure 2.11. This system uses a drive amplifier A, matched in terms of output impedance by the 75ohm source termination $R_T$ to the transmission line connecting stages A and B. In this particular case the line is a 75ohm coax, but in general it is a wideband line matched at both ends, and can alternately be of twisted pair or stripline construction. It is followed immediately by the differential receiver circuit, B, which terminates the line with a load $R_{TERM}$, equal to its 75ohm impedance. The receiver stage recovers a noise-free 1V signal which is referenced to system ground B.
When properly implemented (i.e., the line is source and load terminated in its characteristic impedance), this system presents resistive-only loading to drive amplifier A. This factor makes it near ideal from the mutual viewpoints of amplifier stability, distortion and frequency response, as well as minimizing line reflections and associated time domain aberrations. There is an intrinsic 2/1 (6dB) signal loss associated with the line’s source and load terminations, but this is easily made up by a 2x driver stage gain.

It is very important to understand that the capacitive-load compensation techniques described above are hardly the perfect solution to the line-driving problem. The most foolproof way to drive a long line (which could otherwise present a substantial capacitive load) is to use a transmission line, a standard for signal distribution in video and RF systems for years. Figure 2.12 summarizes several important cable characteristics.

**CABLE CAPACITANCE**

- **All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not controlled)**
- **The Characteristic Impedance is Equal to \( \sqrt{L/C} \), where L and C are the Distributed Inductance and Capacitance**
- **Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance**
- **Unterminated Transmission Lines Behave Approximately as Lumped Capacitance at Frequencies \(<< 1/t_p\), where \( t_p \) = Propagation Delay of Cable**

A transmission line correctly terminated with pure resistance (no reactive component) does not look capacitive. It has a controlled distributed capacitance per foot (C) and a controlled distributed inductance per foot (L). The characteristic impedance of the line is given by the equation \( Z_0 = \sqrt{L/C} \). Coaxial cable is the
most popular form of single-ended transmission line and comes in characteristic impedances of 50ohms, 75ohms, and 93ohms.

Because of skin effect, it exhibits a loss which is a function of frequency as shown in Figure 2.13 for several popular coaxial cables (Reference 5). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (Reference 5).

**COAXIAL CABLE ATTENUATION VERSUS FREQUENCY**

![Graph showing coaxial cable attenuation versus frequency.](image)

*Figure 2.13*

It is useful to examine what happens for conditions of proper and improper cable source/load terminations. To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 2.14. The AD8001 drives 5 feet of 50ohm coaxial cable which is load-end terminated in the characteristic impedance of 50ohms. No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

The output of the cable was measured by connecting it directly to the 50ohm input of a 500MHz Tektronix 644A digitizing oscilloscope. The 50ohm resistor termination is actually the input of the scope. The 50ohm load is not a perfect termination (the scope input capacitance is about 10pF), so some of the pulse is reflected out of phase back to the source. When the reflection reaches the op amp output, it sees the closed-loop output impedance of the op amp which, at 100MHz, is approximately 100ohms. Thus, it is reflected back to the load with no phase reversal, accounting for the negative-going "blip" which occurs approximately 16ns after the leading edge. This is equal to the round-trip delay of the cable (2•5ft•1.6 ns/ft=16ns). In the frequency domain (not shown), the cable mismatch will cause a loss of bandwidth flatness at the load.
Figure 2.14

Figure 2.15 shows a second case, the results of driving the same coaxial cable, but now used with both a 50ohm source-end as well as a 50ohm load-end termination. This case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier’s source termination resistor. The disadvantage is that there is a 2x gain reduction, because of the voltage division between the equal value source/load terminations. However, a major positive attribute of this configuration, with matched source and load terminations in conjunction with a low-loss cable, is that the best bandwidth flatness is ensured, especially at lower operating frequencies. In addition, the amplifier is operated under near optimum loading conditions, i.e., a resistive load.
Source-end (only) terminations can also be used as shown in Figure 2.16, where the op amp is source terminated by the 50ohm resistor which drives the cable. The scope is set for 1Mohm input impedance, representing an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100ohm load (the 50ohm source resistor in series with the 50ohm coax impedance). When the pulse reaches the load, a large portion is reflected in phase because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50ohm source resistance in series with the op amp closed loop output impedance (approximately 100ohms at the frequency represented by the 2ns risetime pulse edge). The reflected portion remains in phase, and appears at the scope input as the positive-going "blip" approximately 16ns after the leading edge.

PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE-TERMINATED 50Ω COAXIAL CABLE

From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100MHz. (Using the rule-of-thumb that bandwidth = 0.35/risetime). At video frequencies, either load-only, or source-only terminations may give acceptable results, but the data sheet should always be consulted to determine the op amp’s closed-loop output impedance at the maximum frequency of interest. A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy.

Now, for a truly worst case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 150pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 2.17 shows the output of the AD8001 driving a lumped 160pF
capacitance (including the scope input capacitance of 10pF). Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.

**PULSE RESPONSE OF AD8001 DRIVING 160pF || 50Ω LOAD**

![Pulse Response Diagram](image)

**Figure 2.17**

**Line Drivers**

The single-ended line driver function complements the receiver at the transmission end (below). This type driver is usually non-inverting, and accepts a signal from a high impedance board level source, scales it, and buffers it to drive a source matched coaxial transmission line of 50-100ohms. Typically, the driver has a gain of 2 times, which complements the 2/1 attenuation of system source/load terminations. A gain-of-two stage seems simple on the surface, but actually many factors become involved in optimizing device and power supply selection to meet overall system performance criteria. Among these are bandwidth/distortion levels versus load impedance, supply voltage/power consumption, and device type.

Fortunately, modern ICs have become more complete in their specifications, as well as more flexible in terms of supply voltage, so there is much from which to choose. For high performance in such demanding applications as wideband video, designers need a fully specified circuit environment, so that the best choice can be easy. For NTSC video systems, distortion is usually rated in terms of differential gain and differential phase, expressed as change in percentage for gain and change in degrees for phase, driving a rated load at the 3.58MHz subcarrier frequency. While traditional 3dB bandwidth is important, a more stringent specification of 0.1dB bandwidth is also often used.
An excellent single-ended, high performance line driver meeting these guidelines is shown in Figure 2.18. Although this circuit uses inexpensive amplifiers, an AD818 (or 1/2 an AD828), it is still has excellent performance. Stage gain is set at 2 times by the equal R1- R2 values, which are also relatively low (500-1kohms), to minimize the feedback time constant. This voltage feedback op amp has maximum effective bandwidth when operated at G=2, and has been optimized for this specific application, thus it is able to achieve a 50MHz 0.1dB bandwidth. For highest linearity, it does not use internal capacitive load compensation. This factor, plus a high current (50mA) output stage provides the gain linearity required for high performance video, and line driving applications.

The NTSC video differential gain/phase performance of this circuit is quite good with the 150ohm loading presented by the 75ohm source termination RT plus the 75ohm load, RL, and is typically on the order of 0.01%/0.05° for a 2Vp-p VOUT video swing while operating at ±15V. These figures do degrade for operation at V_s= ±5V, but can be maintained for supplies of ±10V or more. Thus to minimize distortion, supplies of ±10V to ±15V should be used. Other video grade op amps can also be used for U1, but illustrate the potential for distortion tradeoffs. For example, the AD817 (a similar op amp with internal cap load compensation, see above) achieves NTSC video distortion figures of 0.04%/0.08° at V_s=±15V for the same 150ohm loading.

Supply bypassing for line drivers such as this should include both local low inductance caps C1- C3, as well as larger value electrolytics, for a charge reservoir to buffer heavy load currents. Tantalum types can be used for C2 - C4, and tend to have both lower ESR and small physical size (both desirable), but the 100µF aluminum types shown can also be used. Quiescent current of this circuit is 7mA, which equates to power dissipations of 210 and 70mW for V_s=±15V and ±5V, respectively.
Figure 2.19 shows another high-performance video line driver using the AD810 current feedback amplifier. This circuit is also inexpensive and has higher slew rate and higher output current. The AD810 has a 3dB bandwidth of 65MHz, and a 0.1dB bandwidth of 20MHz, while the quiescent current is only 8mA.

A unique feature of the AD810 is its power-down mode. The DISABLE pin is active-low to shut the device down to a standby current drain of 2mA, with 60dB input isolation at 10MHz. This permits on/off control of a single amplifier, or "wire or-ing" the outputs of a number of devices to achieve a multiplexing function. Note: If the AD810’s disabling function is not required, then the DISABLE pin can float, and it operates conventionally.

Note that when the AD810 is used on different power supplies, the optimum R_F will change (see table... this also will be true for other current feedback amplifiers). Other current feedback amplifiers suitable for this driver function are the single AD811, the dual AD812, and the triple AD813 (with the AD813 also featuring a DISABLE function).
Figure 2.20 illustrates a very high performance video line driver, which has optional
distribution amplifier features. This circuit uses the AD8001 current feedback
amplifier as a gain-of-2 dual 75ohm line driver, generally similar to the above. Some
key performance differences which set this circuit apart lie in the fact that the op
amp employs a complementary UHF process. It is capable of extremely wideband
response, due to the NPN/PNP $f_t$ of 3-5GHz. This allows higher frequency response
at a lower power dissipation than the 500-600MHz $f_t$ complementary process parts,
such as the AD818 or AD810 above. The extended frequency response and lower
power helps achieve low distortion at higher frequencies, while operating at a much
lower quiescent power on supply voltages up to 12V.

Because the higher frequency response per mW of power, a higher output drive is
possible. Here, this leads to a performance difference in that this circuit also doubles
as a distribution amplifier, that is it can drive two 75ohm output lines if desired.
Operated from $\pm 5$V supplies as shown, the circuit has 3dB bandwidth of 440MHz.
Video distortion for differential gain/phase is 0.01%/0.025° with one line driven ($R_L$
= 150ohms). Driving two lines ($R_L = 75$ohms), the differential gain errors are
essentially the same, while the differential phase errors rise to about 0.07°. The
0.1dB bandwidth of this circuit is 110MHz, and the quiescent power is 50mW with
the $\pm 5$V supplies. Supply bypassing should follow the same guidelines as the
previous drivers, and the general physical layout should follow the RF construction
techniques described above and in Chapter 9.

**SINGLE-SUPPLY CONSIDERATIONS**

The term *single-supply* has various implications, some of which are often further
confused by marketing hype, etc. As mentioned above, there is a distinct trend
toward systems which run on lower supply voltages. For high speed designs where
2Vp-p swings are often the norm, $\pm 5$V power supplies have become standard. There
are many obvious reasons for lower power dissipation, such as the ability to run without fans, reliability issues, etc. There are, therefore, many applications for single-supply ADCs other than in systems which have only one supply voltage. In many instances, the lower power drain of a single-supply ADC can be the reason for its selection, rather than the fact that it requires just one supply.

Then, there are also systems which truly operate on a single power supply. In such cases, it can often be difficult to maintain DC coupling from a source all the way to the ADC. In fact, AC coupling is quite often used in single-supply systems, with a DC restoration circuit preceding the ADC. This is necessary to prevent the loss of dynamic range which could otherwise occur, because of a need to provide maximum headroom to an AC coupled signal of arbitrary duty cycle. In the AC-coupled portions of such systems, a “false ground” is often created, usually centered between the rails.

This introduces the question of an optimum input voltage range for a single-supply ADC. At first it would seem that a zero-volt referenced input might be desirable. But in fact, this places severe constraints on the ADC driving amplifier in DC coupled systems, as it must maintain full linearity at or near 0V out. In actuality, there is no such thing as a true rail-rail output amplifier, since all output stage types will have finite saturation voltage(s) to the +Vs rail or ground. Bipolar stages come the closest, and can go as low as an NPN VCESAT of ground (or, a complementary PNP can go within a VCESAT of the + rail). The exact saturation voltage is current dependent, and while it may be only a few mV at light currents, it can be several hundred mV for higher load currents. The traditional CMOS rail-rail output stage looks like a resistor to ground for zero-volt outputs (or to the + rail, for + outputs), so substantial load currents create proportionally higher voltage drops across these resistors, thereby limiting the output swing.

A more optimum ADC input range is thus one which includes neither ground nor the positive supply, and a range centered around V$/frac{1}{2}$/2 is usually optimum. For example, an input range of 2Vp-p around +2.5V is bounded by +1.5V and +3.5V. A complementary common-emitter type single-supply output stage is quite capable of handling this range.

For design and process reasons however, the ADC input common-mode range may be offset from the ideal V$/frac{1}{2}$/2 voltage midpoint. Single-supply op amps dynamic specifications such as distortion, settling time, slew rate, bandwidth, etc. are typically stated for a V$/frac{1}{2}$/2 output bias condition. Distortion and other dynamics can degrade if the signal is offset substantially in either direction from this nominal range.

The output voltage range of an op amp is most often given for DC or low frequency output signals. Distortion may increase as the signal approaches either high or low saturation voltage limits. For instance, a +5V op amp can have a distortion specification of –60dBc for a 3Vp-p output signal. If not stated otherwise, the implication is that the signal is centered around +2.5V (or V$/frac{1}{2}$/2), i.e., the sinewave is bounded by +1V and +4V. If the signal is offset from +2.5, distortion may very well increase.
Low distortion op amp designs typically use a complementary emitter follower output stage. This limits their output swing to slightly greater than 1 diode drop of the rails, in general more like 1V of the rails. In order to maintain low distortion at high frequencies, even more headroom may be required, reducing the available peak-to-peak swing.

The complementary common-emitter output stage allows the output to approach within $V_{CESAT}$ of the rails. However, it does have a higher open-loop output impedance than that of the follower type of stage, and is more likely to distort when driving such non-linear loads as flash converters. When driving constant impedance loads, distortion performance can be equal to or better that the follower type of stage, but such a generalization obviously has its limitations.

The input voltage range of a single-supply op amp may also be restricted. The ability to handle zero-volt input signals can be realized by either a PNP bipolar transistor or N-channel JFET differential input stage. Including both supply rails is rarely required for high frequency signal processing. Of course, the positive rail can be included, if the op amp design uses NPN bipolars, or P-channel JFETs. For true rail-rail input capability, two amplifier input stages must operate in parallel, and the necessary bias crossover point between these stages can result in distortion and reduced CMRR. This type of input stage serves DC and lower frequency amplifiers best.

In many cases, an amplifier may be AC-specified for low voltage single-supply operation, but neither its input nor its output can actually swing very close to the rails. Such devices must use applications designed so that both the input and output common-mode restrictions are not violated. This generally involves offsetting the inputs using some sort of a false ground reference scheme.

To summarize, there are many tradeoffs involved in single-supply high speed designs. In many cases using devices specified for operation on +5V, but without true rail inclusive input/output operation, can give best available performance. As more high speed devices which are truly single-supply become available, they can be added to the designer’s bag of tricks.

**Direct Coupling Requires Careful Design and Controlled Levels**

A design which operates on a single +5V supply with DC coupling is illustrated in Figure 2.21. This type of circuit is useful when the input signal maximum amplitude is known, and a specified output bias level is required to interface to the next stage (such as the ADC input range mentioned).
Here the source voltage is a ±2V 75ohm source, which is DC coupled and terminated by $R_T$. An AD812 amplifier is used, which has an input CM range of +1V to +4V (when operating on +5V), and a minimum output swing of 3Vp-p into 1kohm on 5V. It can easily swing the required 2Vp-p at the output, so there is some latitude for biasing it around an output level of $V_s/2$. For unity signal gain, equal value feedback and input resistors are used. The $R_F$ and $R_IN$ values chosen are a slight compromise to maximum bandwidth (the optimum value is 715ohms), but the input line is terminated properly at 75ohms (the parallel equivalent value of $R_T$ and $R_IN$).

The resulting resistor values provide a gain of about 1.95 to the DC voltage applied to pin 3, $V_{BIAS}$. A voltage of 1.235V from a stable reference source such the AD589 will fix the static output DC level at 1.95•1.235V, or 2.41V. Because of the inverting mode signal operation, pin 2 of the op amp does not change appreciably with signal, therefore this node effectively operates at a fixed DC level, equal to $V_{BIAS}$. As long as this bias voltage is well above the amplifier’s minimum CM range of +1V, there should be no problem. The RC network at pin 3 provides a noise filter for the diode. If a more precise output DC level is required from this stage, then $V_{BIAS}$ can be adjusted to provide it without change to the stage’s signal gain.

**Single-Supply Line Drivers**

By choosing a high frequency op amp which is specified for operation on low voltage supplies, single-ended line drivers can also be adapted for single 5V supply operation. An example is the 5V supply line driver circuit of Figure 2.22, which also illustrates AC coupling in single-supply design.
Speaking generally, this circuit can use a number of op amps, both voltage and current feedback types. The output of the AD812 and AD813 devices can swing to within about 1V of either rail, allowing 3Vp-p outputs to be delivered into 150ohm loads on 5V. While bandwidth of these current feedback amplifiers does reduces with low voltage operation, they are still capable of a small signal 0.1dB bandwidth on the order of 10MHz, and good differential gain/phase performance, about 0.07%/0.06°, quite good for a simple circuit. The AD817 and AD818 are not as clean in performance, and not necessarily recommended for 5V line drivers, but are included as examples of more general purpose voltage feedback types operable on 5V. For optimizing the bias and bandwidth of any of these amplifiers, use the resistor values from the table.

As would be expected, headroom is critical on such low supplies, so if nothing else, biasing should be optimized for the voltage in use, via the R5 value as noted. R3 and R4 are equal values, AC bypassed for minimum noise coupling from the supply line. All input and output coupling capacitors are large in value, and are so chosen for a minimum of low frequency phase shift, for composite video uses. They can be reduced for applications with higher low frequency cutoffs. C_OUT is potentially a problem in the large value shown, as large electrolytics can be inductive. C5, a non-critical optional low inductance shunt, can minimize this problem.

Obviously, the stage cannot be driven beyond 3Vp-p at V_OUT without distortion, so operating levels need to maintained conservatively below this. The next section discusses AC coupling issues and headroom in more detail.

The AC coupling of arbitrary waveforms can actually introduce problems which don’t exist at all in DC coupled or DC restored systems. These problems have to do with
the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are AC coupled.

In an amplifier circuit such as that of Figure 2.22, the output bias point will be equal to the DC bias as applied to the op amp’s (+) input. For a symmetric (50% duty cycle) waveform of a 2Vp-p output level, the output signal will swing symmetrically about the bias point, or nominally 2.5V ±1V. If however the pulsed waveform is of a very high (or low) duty cycle, the AC averaging effect of CIN and R4 || R5 will shift the effective peak level either high or low, dependent upon the duty cycle. This phenomenon has the net effect of reducing the working headroom of the amplifier, and is illustrated in Figure 2.23.

Figure 2.23

In Figure 2.23 (A), an example of a 50% duty cycle square wave of about 2Vp-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5V supply amplifier. This amplifier, for example, (an AD817 biased similarly to Figure 2.22) can only swing to the limited DC levels as marked, about 1V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes while maintaining the same peak-to-peak input level. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

Since standard video waveforms do vary in duty cycle as the scene changes, the point is made that low distortion operation on AC coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3Vp-p output swing available before clipping, and it must cleanly reproduce an arbitrary waveform, then the maximum allowable amplitude is less than 1/2 of this 3Vp-p swing, that is <1.5Vp-p. An example of violating this criteria is contained the 2Vp-p waveform of Figure 2.23, which is clipping for both the high and low duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an
even more conservative criteria for lowest distortion operation such as composite NTSC video amplifiers.

Of course, amplifiers designed with rail-rail outputs and low distortion in mind address these problems most directly. One such device is the AD8041, an XFCB single-supply op amp designed for video applications, and summarized briefly by Figure 2.24. As these data show, this part is designed to provide low NTSC video distortion while driving a single 75ohm source terminated load (in a circuit such as Figure 2.22).

**RAIL-RAIL OUTPUT VIDEO OP AMPS ALLOW LOW DISTORTION OUTPUT AND GREATEST FLEXIBILITY**

Typical specifications for AD8041 op amp @ $V_s = +5V$, $T_A = 25^\circ C$

- Common Mode Range: -0.2V to +4V
- Offset Voltage: 2mV
- Bias Current: 1.2μA
- Bandwidth: 80MHz
- Slew Rate: 160V/μs
- Differential Gain/Phase: 0.03%/ 0.03°
- ($V_{out} = 2Vp-p$, $R_L=150\Omega$)
- Output Current: 50mA (0.5V from rails)
- Quiescent Current: 5mA
- Disable Feature Allows Multiplexing

Figure 2.24

**APPLICATION CIRCUITS**

A common video circuit requirement is the multiplexer, a stage which selects one of “N” video inputs, and transmits a buffered version of the selected signal to an output transmission line. Video amplifiers which can operate internally in a switched mode, such as the AD810 and AD813, allow this operation to be performed directly in the video signal path with no additional hardware. This feature is activated with the use of the device’s *disable* pin, which when pulled low, disables the amplifier and drops power to a low state. The AD810 is a single channel current feedback amplifier with this disable feature, while the AD813 offers similar functionality, in a 14 pin, three channel format. The high performance of the AD813 on low voltages allows it to achieve high performance on ±5V supplies, and to be directly interfaced with standard 5V logic drivers.

**2:1 Video Multiplexer**

The outputs of two AD810s can be wired together to form a 2:1 multiplexer without degrading the flatness of the gain response. Figure 2.25 shows a recommended configuration, which results in a 0.1dB bandwidth of 20MHz and OFF channel isolation of 77dB at 10MHz on ±5V supplies. The time to switch between channels is about 750ns when the disable pins are driven by open drain output logic. With the use of the recommended 74HC04 as shown, the switching time is about 180ns. The switching time is only slightly affected by the signal level.
A 2:1 VIDEO MULTIPLEXER USING AD810s HAS -0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 180ns

Figure 2.25

3:1 Video Multiplexer

A 3:1 video multiplexer circuit using the triple AD813 is shown in Figure 2.26, and features relative simplicity and high performance while operating from ±5V power supplies. The 3 standard 1Vp-p video input signals \( V_{IN1} - V_{IN3} \) drive the 3 channels of the AD813, one of which is ON at a given moment. If say channel 1 is selected, amplifier section 1 is enabled, by virtue of a logic HIGH signal on the SELECT1 line driving the ENABLE input of the first amplifier. The remaining two amplifier channels appear as open circuits looking back into them, but their feedback networks do appear as a load to the active channel. Control logic decoding is provided by U2, a 74HC238 1 of 8 logic decoder. The control lines A0 and A1 are decoded as per the truth table, which provides selection between the 3 input signals and OFF, as noted.
3:1 VIDEO MULTIPLEXER USING AD813 TRIPLE OP AMP

Some design subtleties of the circuit come about because of necessity to account for several design criteria. One is the 590ohm value of feedback resistor R1, to provide optimum response to the AD813 current feedback amplifier; another is the parasitic loading of the two unused gain resistor networks; a third is the source termination of the line, 75ohms in this case. While any given channel is ON, it drives not only load resistor RL, but also the net dummy resistance RX/2, where RX is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity plus and effective 75ohm source impedance, this sets the resistance values of R1 + R2 + R3 as shown.
SWITCHING CHARACTERISTICS OF 3:1 VIDEO MULTIPLEXER

Performance of the circuit is excellent, with 0.1dB bandwidth of 20MHz, and an OFF state isolation of 60dB at 10MHz. Switching time is about 180ns, and is shown in Figure 2.27 switching between two different inputs (top trace) with the control input also shown (bottom trace).

Figure 2.27

Video Programmable Gain Amplifier

Closely related to the 3:1 multiplexer of Figure 2.26 is a programmable gain video amplifier, or PGA, as shown in Figure 2.28. With a similarly configured 2 line digital control input, this circuit can be set up to provide 3 different gain settings. This makes it a useful tool in various systems which can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, etc. The gains can be binary related as here, or they can be arbitrary. An extremely useful feature of the AD813 current feedback amplifier to this application is the fact that the bandwidth does not reduce in inverse proportion, as gain is increased. Instead, it stays relatively constant as gain is raised. Thus more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product amplifier type.
GAIN OF 1, 2, 4 PROGRAMMABLE GAIN VIDEO AMPLIFIER

Figure 2.28

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can varied by adjustment of the R2/R3 or R4/R5 ratios. For the gain range and values shown, the PGA will be able to maintain a 3dB bandwidth of about 50MHz or more for loading as shown (a high impedance load of 1kohm or more is assumed). Fine tuning of the bandwidth for a given gain setting can be accomplished by tweaking the absolute values of the feedback resistors (most applicable at higher gains).

Differential Drivers

Many applications require gain/phase matched complementary or differential signals. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of 2nd harmonic distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as UTP-5. While various topologies can be employed to derive differential drive signals, many circuit details as well as the topologies themselves are important as to how accurate two outputs can be maintained.

Inverter-Follower Differential Driver

The circuit of Figure 2.29 is useful as a high speed differential driver for driving high speed 10-12 bit ADCs, differential video lines, and other balanced loads at levels of 1-4Vrms. As shown it operates from ±5V supplies, but it can also be adapted to supplies in the range of ±5 to ±15V. When operated directly from ±5V as here, it
minimizes potential for destructive ADC overdrive when higher supply voltage buffers drive a ±5V powered ADC, in addition to minimizing driver power.

**DIFFERENTIAL DRIVER USING INVERTER/FOLLOWER**

In many of these differential drivers the performance criteria is high. In addition to low output distortion, the two signals should maintain gain/phase flatness. In this driver, two sections of an AD812 dual current feedback amplifier are used for the channel A & B buffers, U1A & U1B. This measure can provide inherently better open-loop bandwidth matching than will the use of two individual same part number singles (where bandwidth varies between devices from different manufacturing lots).

The two buffers here operate with precise gains of ±1, as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715ohm resistors- the value for using the AD812 on ±5V supplies.

In channel A, non-inverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network RFB1 and RG1 (Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor RFB1, and no gain resistor at all. Here, with input resistor RG1 added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of RFB1-RG1, the signal gain is maintained at unity. Given the matched open loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction which greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for RG2-RFB2. Here a worst case 2% mis-match will result in less than 0.2dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.
If desired, phase matching is trimmed via $R_{G1}$, so that the phase of channel A closely matches that of B. This can be done for new circuit conditions, by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as $R_{G1}$ is adjusted for the best null conditions at the sum node. The A-B gain/phase matching is quite effective in this driver, with test results of the circuit as shown 0.04dB and 0.1° between the A and B output signals at 10MHz, when operated into dual 150ohm loads. The 3dB bandwidth of the driver is about 60MHz.

Net input impedance of the circuit is set to a standard line termination value such as 75ohms (or 50ohms), by choosing $R_{IN}$ so that the desired value results with $R_{IN}$ in parallel with $R_{G2}$. In this example, an $R_{IN}$ value of 83.5ohms provides a standard input impedance of 75ohms when paralleled with 715ohms. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this is not totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813, with the third channel as a variable gain input buffer.

**CROSS-COUPLED DIFFERENTIAL DRIVER PROVIDES BALANCED OUTPUTS AND 250MHz BANDWIDTH**

![Cross-Coupled Differential Driver Circuit](image)

**Figure 2.30**

**Cross-Coupled Differential Driver**

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 2.30, by connecting AD8002 dual current feedback amplifier sections as cross-coupled inverters, their outputs are forced equal and opposite, assuring zero output common mode voltage.
The gain cell which results, U1A and U1B plus cross-coupling resistances $R_X$, is fundamentally a differential input and output topology, but it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The gain of the stage from $V_{IN}$ to $V_{OUT}$ is:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2R_1}{R_2}$$

where $V_{OUT}$ is the differential output, equal to $V_{OUTA} - V_{OUTB}$.

This circuit has some unique benefits. First, differential gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as is true in the case of a conventional current feedback amplifier. Thus they are not highly critical as to absolute value. This is unlike standard applications using current feedback amplifiers, and will be true as long as the equivalent resistance seen by U1A is reasonably low (less than 1kohm in this case). Third, the cell bandwidth can be optimized to the desired gain by a single optional resistor, $R_3$, as follows. If for instance, a net gain of 20 is desired ($R_1/R_2=10$), the bandwidth would otherwise be reduced by roughly this amount, since without $R_3$ the cell operates with a constant gain-bandwidth product. With $R_3$ present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of $R_3$, which, given an appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.

In the circuit as shown, no $R_3$ is necessary at the low working gain of 2 times differential, since the 511ohm $R_X$ resistors are already optimized for maximum bandwidth. Note that these four matched resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains as set by $R_1/R_2$, $R_3$ can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

$$R_3 = \frac{R_X}{(R_1 / R_2) - 1}$$

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, $C_1$, may be needed to optimize flatness of frequency response. In this example, a 0.9pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5-2pF. This capacitor is then value selected at board characterization for optimum frequency response.
For the dual trace, 1-500MHz swept frequency response plot of Figure 2.31, output levels were 0dBm into matched 50ohm loads, through back termination resistances RTA and RTB, at VOUTA and VOUTB. In this plot the vertical scale is 2dB/div, and it shows the 3dB bandwidth of the driver measuring about 250MHz, with peaking about 0.1dB. The four RX resistors along with RTA and RTB control low frequency amplitude matching, which was within 0.1dB in the lab tests, using 511ohm 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

Due to the high gain-bandwidths involved with the AD8002, the construction of this circuit should follow RF rules, with the use of a ground plane, chip bypass capacitors of zero lead length at the ±5V supply pins, and surface mount resistors for lowest inductance.

**Differential Receivers**

Another standard system application is the line receiver function, a stage which accepts signals from a single-ended (or differential) transmission line, and converts them into a buffered version for local processing (referring back to the system diagram of Figure 2.11). In a typical system, there is a single ended driving signal VIN at the origination point, a coaxial transmission line with the signal terminated in the characteristic line impedance at the local end, and finally, a differential input receiver. The system operates the same in principle for standard impedances of 50-100ohms, as long as the source and load impedances match that of the line, under which conditions bandwidth is maximized. In the receiver, input impedance is assumed high in relation to line impedance, and high common-mode rejection (CMR) allows rejection of spurious noise appearing between driver/receiver grounds. Noise is rejected in proportion to the CMR of the receiver amplifier, and typical CMR performance goal for such a stage is 60-70dB or better for frequencies up to 10MHz.
Functionally, this system delivers at the output of the receiver stage a signal \( V_{OUT} \), a replica of the original driving signal \( V_{IN} \). The receiver may also scale the received signal, and may also be called on to drive another transmission line. Critical performance parameters for the receiver are signal bandwidth and distortion specifications. For line receivers, video distortion is rated in terms of differential gain and differential phase at the 3.58 MHz subcarrier frequency.

**4 Resistor Differential Line Receiver**

Figure 2.32 shows a low cost, medium performance line receiver using a high speed op amp rated for video use. It is actually a standard 4 resistor instrumentation amplifier optimized for high speed, with a differential to single-ended gain of \( \frac{R_2}{R_1} \). Using low value, DC accurate/AC trimmed resistances for \( R_1-R_4 \) and a high speed, high CMR op amp provides the good performance. Practically speaking however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst case CMR (in dB) of this circuit due to resistor effects is:

\[
CMR = 20 \log_{10} \left( \frac{1 + \frac{R_2}{R_1}}{4Kr} \right)
\]

In this expression the term “\( Kr \)” is a single resistor tolerance in fractional form (1% = 0.01, etc.), and it is assumed the amplifier has significantly higher CMR (greater than 100dB). Using discrete 1% metal films for \( R_1/R_2 \) and \( R_3/R_4 \) yields a worst case CMR of 34dB, 0.1% types 54dB, etc. Of course 4 random 1% resistors will on the average yield a CMR better than 34dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Ohmtek 1005, (Reference 6) which has a ratio match of 0.1%, which will provide a worst case low frequency CMR of 66dB.
This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed ±5V supply rails in some cases without hazard. Operation at ±15V should constrain the inputs within the rails.

At frequencies above 1MHz, the bridge balance is dominated by AC effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values. In a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5pF increments, for best high frequency CMR. Using designated PC pads, production values then would use the trimmed value. Good AC matching is essential to achieving good CMR at high frequencies. C1-C2 should be types similar physically, such as NPO (or other stable) ceramic chip style capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit. Alternately, a scheme for continuous gain control without interaction with CMR is to follow this receiver with a scaling amplifier/driver with adjustable gain. The similar AD828 dual amplifier allows this with the addition of only two resistors.
Video gain/phase performance of this stage is dependent upon the device is used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of ±10 - ±15V, which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with low distortion video operation perform best. The circuit as shown can be used with supplies of ±5 to ±15V, but lowest NTSC video distortion occurs for supplies of ±10V or more, where differential gain/differential phase errors are less than 0.01%/0.05°. Operating at ±5V the distortion rises somewhat, but the lowest power drain of 70mW occurs.

One drawback to this circuit is that it does load a 75ohm video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

**Active Feedback Differential Line Receiver**

Fully integrating the line receiver function eliminates the resistor-related drawbacks of the 4 resistor line receiver, improving CMR performance, ease of use, and overall circuit flexibility. An IC designed for this function is the AD830 active feedback amplifier (Reference 7,8). Its use as a differential line receiver with gain is illustrated in Figure 2.33.

**VIDEO LOOP-THROUGH CONNECTION USING THE AD830**

![Figure 2.33](image)

The AD830 operates as a feedback amplifier with two sets of fully differential inputs, available at pins 1-2 and 3-4, respectively. Internally, the outputs of the two stages are summed and drive a buffer output stage. Both input stages have high CMR, and can handle differential signals up to ±2V, and CM voltages can range up to 

$-V_s+3V$ or $+V_s−2.1V$, with a ±1V differential input applied. While the AD830 does not normally need protection against CM voltages, if sustained transient voltage beyond the rails is encountered, an optional pair of equal value (approximately 200ohms) resistances can be used in series with pins 1-2.
In this device the overall feedback loop operates so that the differential voltages \( V_{1-2} \) and \( V_{3-4} \) are forced to be equal. Feedback is taken from the output back to one input differential pair, while the other pair is driven by a differential input signal. An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so CMR isn’t dependent on resistor bridges and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at DC.

The general expression for the U1 stage’s gain “G” is like a non-inverting op amp, or:

\[
G = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 + \frac{R_2}{R_1}
\]

For lowest DC offset, balancing resistor \( R_3 \) is used (equal to \( R_1 \| R_2 \)).

In this example of a video “loop-through” connection, the input signal tapped from a coax line and applied to one input stage at pins 1-2, with the scaled output signal tied to the second input stage between pins 3-4. With the \( R_1-R_4 \) feedback attenuation of 2/1, the net result is that the output of U1, is then equal to \( 2 \cdot V_{\text{IN}} \), i.e., a gain of 2.

Functionally, the input and local grounds are isolated by the CMR of the AD830, which is typically 75dB at frequencies below 1MHz, 60dB at 4.43MHz, and relatively supply independent.

With the addition of an output source termination resistor \( R_T \), this circuit has an overall loaded gain of unity at the load termination, \( R_L \). It is a ground isolating video repeater, driving the terminated 75ohm output line, delivering a final output equal to the original input, \( V_{\text{IN}} \).

NTSC video performance will be dependent upon supplies. Driving a terminated line as shown, the circuit has optimum video distortion levels for \( V_s \pm 15V \), where differential gain is typically 0.06%, and differential phase 0.08°. Bandwidth can be optimized by the optional 5.1pF (or 12pF) capacitor, \( C_A \), which allows a 0.1dB bandwidth of 10MHz with \( \pm 15V \) operation. The differential gain and phase errors deteriorate about 2 or more times at \( \pm 5V \).
REFERENCES:


SECTION 3

HIGH RESOLUTION SIGNAL CONDITIONING ADCs

- Sigma-Delta ADCs
- High Resolution, Low Frequency Measurement ADCs
SECTION 3

HIGH RESOLUTION SIGNAL CONDITIONING ADCs

Walt Kester, James Bryant, Joe Buxton

The trend in ADCs and DACs is toward higher speeds and higher resolutions at reduced power levels. Modern data converters generally operate on ±5V (dual supply) or +5V (single supply). There are now a few converters which operate on a single +3V supply. This trend has created a number of design and applications problems which were much less important in earlier data converters, where ±15V supplies were the standard.

Lower supply voltages imply smaller input voltage ranges, and hence more susceptibility to noise from all potential sources: power supplies, references, digital signals, EMI/RFI, and probably most important, improper layout, grounding, and decoupling techniques. Single-supply ADCs often have an input range which is not referenced to ground. Finding compatible single-supply drive amplifiers and dealing with level shifting of the input signal in direct-coupled applications also becomes a challenge.

In spite of these issues, components are now available which allow extremely high resolutions at low supply voltages and low power. This section discusses the applications problems associated with such components and shows techniques for successfully designing them into systems.

LOW POWER, LOW VOLTAGE ADC DESIGN ISSUES

- Low Power ADCs typically run on ±5V, +5V, +5/+3V, or +3V
- Lower Signal Swings Increase Sensitivity to All Types of Noise (Device, Power Supply, Logic, etc.)
- Device Noise Increases at Low Quiescent Currents
- Bandwidth Suffers as Supply Current Drops
- Input Common-Mode Range May be Limited
- Selection of Zero-Volt Input/Output Amplifiers is Limited
- Auto-Calibration Modes Highly Desirable at High Resolutions

Figure 3.1
SIGMA-DELTA ADCs
(COURTESY OF JAMES M. BRYANT)

Because Sigma-Delta is such an important and popular architecture for high resolution (16 to 24 bits) ADCs, the section begins with a basic description of this type of converter.

Sigma-Delta Analog-Digital Converters have been known for nearly thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of Sigma-Delta ADCs, but most commence with a maze of integrals and deteriorate from there. In the Applications Department at Analog Devices, we frequently encounter engineers who do not understand the theory of operation of Sigma-Delta ADCs and are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about Sigma-Delta ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A Sigma-Delta ADC contains very simple analog electronics (a comparator, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a Sigma-Delta ADC works one should be familiar with the concepts of over-sampling, noise shaping, digital filtering, and decimation.

SIGMA-DELTA (Σ-Δ) ADCs

- Sigma-Delta ADCs are low-cost and have high resolution, excellent DNL, low-power, although limited input bandwidth
- A Σ-Δ ADC is Simple
- The Mathematics, however is Complex
- This section Concentrates on What Actually Happens!

Figure 3.2
SIGMA-DELTA ADC KEY CONCEPTS

- Oversampling
- Noise Shaping
- Digital Filtering
- Decimation

Figure 3.3

An ADC is a circuit whose digital output is proportional to the ratio of its analog input to its analog reference. Often, but by no means always, the scaling factor between the analog reference and the analog signal is unity, so the digital signal represents the normalized ratio of the two.

Figure 3.4 shows the transfer characteristic of an ideal 3-bit unipolar ADC. The input to an ADC is analog and is not quantized, but its output is quantized. The transfer characteristic therefore consists of eight horizontal steps (when considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps).

![Transfer Characteristic of an Ideal 3-bit Unipolar ADC](image)

Figure 3.4

Digital full scale (all "1"s) corresponds to 1 LSB below the analog full scale (the reference or some multiple thereof). This is because, as mentioned above, the digital code represents the normalized ratio of the analog signal to the reference, and if this were unity, the digital code would be all "0"s and "1" in the bit above the MSB.
The (ideal) ADC transitions take place at _ LSB above zero and thereafter every LSB, until 1 LSB below analog full scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to _ LSB between the actual analog input and the exact value of the digital output. This is known as the quantization error or quantization uncertainty. In AC (sampling) applications, this quantization error gives rise to quantization noise. If we apply a fixed input to an ideal ADC, we will always obtain the same output, and the resolution will be limited by the quantization error.

Suppose, however, that we add some AC (dither) to the fixed signal, take a large number of samples, and prepare a histogram of the results. We will obtain something like the result in Figure 3.5. If we calculate the mean value of a large number of samples, we will find that we can measure the fixed signal with greater resolution than that of the ADC we are using. This procedure is known as over-sampling.

**OVERSAMPLING WITH DITHER ADDED TO INPUT**

![Histogram](image)

Figure 3.5

The AC (dither) that we add may be a sine-wave, a tri-wave, or Gaussian noise (but not a square wave) and, with some types of sampling ADCs (including Sigma-Delta ADCs), an external dither signal is unnecessary, since the ADC generates its own. Analysis of the effects of differing dither waveforms and amplitudes is complex and, for the purposes of this section, unnecessary. What we do need to know is that with the simple over-sampling described here, the number of samples must be doubled for each _bit of increase in effective resolution.

If, instead of a fixed DC signal, the signal that we are over-sampling is an AC signal, then it is not necessary to add a dither signal to it in order to over-sample, since the signal is moving anyway. (If the AC signal is a single tone harmonically related to the sampling frequency, dither may be necessary, but this is a special case.)

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a DC conversion has a quantization error of up to _ LSB, a sampled data system has quantization noise. As we have already seen, a perfect classical
N-bit sampling ADC has an rms quantization noise of \( q/(\sqrt{12}) \) uniformly distributed within the Nyquist band of DC to \( f_s/2 \) (where \( q \) is the value of an LSB and \( f_s \) is the sampling rate). Therefore, its SNR with a full-scale sinewave input will be \( (6.02N + 1.76) \) dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than \( N \)-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

\[
ENOB = \frac{SNR - 1.76\,dB}{6.02\,dB}.
\]

If we choose a much higher sampling rate, the quantization noise is distributed over a wider bandwidth as shown in Figure 3.7. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal - so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC.
OVERSAMPLING FOLLOWED BY DIGITAL FILTERING AND DECIMATION IMPROVES SNR AND ENOB

Figure 3.7

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (decem is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 3.8).

DECIMATION

Figure 3.8
If we simply use over-sampling to improve resolution, we must over-sample by a factor of \(2^{2N}\) to obtain an N-bit increase in resolution. The Sigma-Delta converter does not need such a high over-sampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order Sigma-Delta modulator as shown in Figure 3.9. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a Sigma-Delta ADC: the Sigma-Delta modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

**FIRST ORDER SIGMA-DELTA ADC**

![Figure 3.9](image)

By using more than one integration and summing stage in the Sigma-Delta modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio as is shown in Figure 3.10 for both a first and second-order Sigma-Delta modulator. The block diagram for the second-order Sigma-Delta modulator is shown in Figure 3.11. Third, and higher, order Sigma-Delta ADCs were once thought to be potentially unstable at some values of input - recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.
Figure 3.10
SECOND-ORDER SIGMA-DELTA ADC

Figure 3.11

Figure 3.12 shows the relationship between the order of the Sigma-Delta modulator and the amount of over-sampling necessary to achieve a particular SNR.
The Sigma-Delta ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from DC. Thus, their quantization noise is pushed up in frequency. At present, all commercially available Sigma-Delta ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system DC offsets). Sigma-Delta ADCs are available with resolutions up to 24-bits for DC measurement applications (AD7710, AD7711, AD7712, AD7713, AD7714), and with resolutions of 18-bits for high quality digital audio applications (AD1879).

But there is no particular reason why the filters of the Sigma-Delta modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a Sigma-Delta ADC with bandpass filters (BPFs), the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see Reference 1). If the digital filter is then programmed to have its pass-band in this region, we have a Sigma-Delta ADC with a bandpass, rather than a low pass characteristic (see Figure 3.13). Although studies of this architecture are in their infancy, such ADCs would seem to be ideally suited for use in digital radio receivers, medical ultrasound, and a number of other applications.
A Sigma-Delta ADC works by over-sampling, where simple analog filters in the Sigma-Delta modulator shape the quantization noise so that the SNR in the bandwidth of interest is much lower than would otherwise be the case, and by using high performance digital filters and decimation to eliminate noise outside the required passband. Because the analog circuitry is so simple and undemanding, it may be built with the same digital VLSI process that is used to fabricate the DSP circuitry of the digital filter. Because the basic ADC is 1-bit (a comparator), the technique is inherently linear.

Although the detailed analysis of Sigma-Delta ADCs involves quite complex mathematics, their basic design can be understood without the necessity of any mathematics at all. For further discussion on Sigma-Delta ADCs, refer to References 2 and 3.

SIGMA-DELTA SUMMARY

- Linearity is Inherently Excellent
- High Resolutions (16 - 24 Bits)
- Ideal for Mixed-Signal IC Processes, no Trimming
- No SHA Required
- Charge Injection at Input Presents Drive Problems
- Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio, but Bandpass Sigma-Delta Techniques Will Change This
- Analog Multiplexing Applications are Limited by Internal Filter Settling Time. Consider One Sigma-Delta ADC per Channel.
HIGH RESOLUTION, LOW-FREQUENCY MEASUREMENT ADCs

The AD7710, AD7711, AD7712, AD7713, and AD7714 are members of a family of sigma-delta converters designed for high accuracy, low frequency measurements. They have no missing codes at 24-bits and useful resolution of up to 21.5-bits (AD7710, AD7711, AD7712, and AD7713), and 22.5 bits (AD7714). They all use similar sigma-delta cores, and their main differences are in their analog inputs, which are optimized for different transducers. The AD7714 is the newest member of the family and is fully specified for either +5V (AD7714-5) or +3V (AD7714-3) operation.

The digital filter in the sigma-delta core may be programmed by the user for output update rates between 10Hz and 1kHz (AD7710, AD7711, AD7712), 2Hz and 200Hz (AD7713), and 2Hz and 1kHz (AD7714). The effective resolution of these ADCs is inversely proportional to the bandwidth. For example, for 22.5-bits of effective resolution, the output update rate of the AD7714 cannot exceed 10Hz. The AD771X family is ideal for such sensor applications as those shown in Figure 3.15.

SIGNAL CONDITIONING, TRANSDUCER INPUT ADCs
THE AD7710, AD7711, AD7712, AD7713, AD7714

- Ultra-High Resolution Measurement Systems
- Implemented Using ΣΔ Conversion
- Ideal for Applications Such As:
  - Weigh Scales
  - RTDs
  - Thermocouples
  - Strain Gauges
  - Process Control
  - Smart Transmitters
  - Medical

Figure 3.15

The AD771X family has a high level of integration which simplifies the design of data acquisition systems. For example, the AD7710 (Figures 3.16 and 3.17) has two high impedance differential inputs that can be interfaced directly to many different sensors, including resistive bridges. The two inputs are selected by the internal multiplexer, which passes the signal to a programmable gain amplifier (PGA). The PGA has a digitally programmable gain range of 1 to 128 to accommodate a wide range of signal inputs. After the PGA, the signal is digitized by the sigma-delta modulator. The digital filter notch frequency may be adjusted from 10Hz to 1kHz, which allows various input bandwidths.

To achieve this high accuracy, the AD771X family has four different internal calibration modes, including system and background calibration. All of these
functions are controlled via a serial interface. A benefit of this serial interface is that the AD771X-family fits into a 24-pin package, giving a small footprint for the high level of integration. All of the parts except the AD7713 and AD7714 can operate on either a single +5V or dual ±5V supplies. The AD7713 is designed exclusively for single supply (+5V) operation. The AD7714 is the newest member of the family and is designed for either single +3V (AD7714-3) or single +5V (AD7714-5) low power applications. The AD771X family has <0.0015% non-linearity.

THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE

Figure 3.16

KEY FEATURES OF THE AD7710

- ±0.0015% Nonlinearity
- Two Channels with Differential Inputs
- Programmable Gain Amplifier (G = 1 to 128)
- Programmable Low Pass Filter
- System or Self-Calibration Options
- Single or Dual 5V Supply Operation
- Microcontroller Serial Interface

Figure 3.17
The AD7710, AD7711, AD7712, and AD7713 have identical structures of PGA, sigma-delta modulator, and serial interface. Their main differences are in their input configurations. The AD7710 has two low level differential inputs, the AD7711 two low level differential inputs with excitation current sources which make it ideal for RTD applications, the AD7712 has one low level differential input and a single ended high level input that can accommodate signals of up to four times the reference voltage, and the AD7713 is designed for loop-powered applications where power dissipation is important. The AD7713 consumes only 3.5mW of power from a single +5V supply.

The AD7714 is designed for either +3V (AD7714-3) or +5V (AD7714-5) single-supply, low power applications. It has a buffer between the multiplexer and the PGA which can be enabled or bypassed using a control line. When the buffer is active, it isolates the analog inputs from the transient currents and variable impedance of the switched-capacitor PGA.

### SUMMARY TABLE OF AD771X DIFFERENCES

| AD7710: | 2-Channel Low-Level Differential Inputs |
| AD7711: | 1-Channel Low-Level Differential Input |
|  | 1-Channel Low-Level Single-Ended Input |
|  | Excitation Current Sources for 3 or 4-Wire RTDs |
| AD7712: | 1-Channel Low-Level Differential Input |
|  | 1-Channel High-Level Single-Ended Input |
| AD7713: | 2-Channel Low-Level Differential Inputs |
|  | 1-Channel High-Level Single-Ended Input |
|  | Excitation Current Sources for 3 or 4-Wire RTDs |
|  | Single 5V Operation Only |
|  | Low Power (3.5mW) |
|  | No Internal Reference |
| AD7714: | 3-Channel Low-Level Differential Inputs or 5-Channel Pseudo-Differential Inputs |
|  | Single +3V (AD7714-3) or Single +5V (AD7714-5) |
|  | Low Power (1.5mW: AD7714-3) |
|  | No Internal Reference |

Figure 3.18

Because of the differences in analog interfaces, each device is best suited to a particular sensor or system application. In other words, the sensor and the system requirements (i.e. type of sensor, single versus dual supply, power consumption, etc.) determine which converter should be used. Figure 3.19 lists the converters, and the sensors and applications to which they are best suited.
AD771X APPLICATIONS

■ AD7710:
  ◆ Weigh Scales
  ◆ Thermocouples
  ◆ Chromatography
  ◆ Strain Gauge

■ AD7711:
  ◆ RTD Temperature Measurement

■ AD7712:
  ◆ Smart Transmitters
  ◆ Process Control

■ AD7713:
  ◆ Loop-Powered Smart Transmitters
  ◆ RTD Temperature Measurement
  ◆ Process Control
  ◆ Portable Industrial Instruments

■ AD7714:
  ◆ Single +3V Supply Applications
  ◆ Portable Industrial Instruments
  ◆ Portable Weigh Scales

Figure 3.19

Although the AD7714 is often used as an example, the following discussion applies to all the converters in the family, with some minor exceptions. The basic AD7714 ADC (see Figure 3.20) is a switched capacitor sigma-delta converter which operates as has previously been discussed in this section. The signals on the input channels pass through a switching matrix (multiplexer) and into a bypassable buffer. The buffer (available only in the AD7714) allows the input signals to be isolated from the PGA switching transients and variable impedance (PGA operation will be described shortly). The PGA gain is programmable from 1 to 128, thereby allowing low level signals to be converted without the need for external amplification.
The functional block diagram of the AD7714 shows the PGA as separate from the sigma-delta modulator. In fact, it is part of the sigma-delta integrator (see Figure 3.21). The differential signal input charges C2, which is then discharged into the integrator summing node. This is done by closing S1 and S2, and then, after opening them, closing S3 and S4. When the PGA has a gain of 1 this happens once per cycle of the basic 19.2kHz clock, but for gains of 2, 4, and 8 respectively it happens 2, 4, or 8 times per cycle. The integrator charge is balanced by switching charge in the same way from the reference into C1, and thence to the integrator summing node. The polarity of reference switched depends on the state of the comparator output.
The AD7714 Σ-Δ modulator includes a PGA function

Figure 3.21

At a gain of 8, the sampling rate is 153.6kHz. Higher switching rates than this would not allow C2 sufficient time to charge, so for PGA gains greater than 8, the value of the reference capacitor, C1, is reduced, rather than the sampling rate being increased. Each time C1 is halved the gain of the system is doubled. The original value of C1 for gains of 1-8 is about 7pF in the AD7714 and 20pF for the other members of the AD771X family.

The internal digital filter has the sinc-cubed response illustrated in Figure 3.22. The first notch in the filter response is programmable according to the formula:

\[
f_{\text{notch}} = \left( \frac{f_{\text{clkin}}}{128} \right) \left( \frac{1}{\text{Decimal Value of Digital Code}} \right),
\]

where \( f_{\text{clkin}} \) is normally either 2.4576MHz or 1MHz for the AD7714. The decimal value of the digital code in the above equation is loaded into the appropriate register in the AD7714. The master clock \( f_{\text{clkin}} \) frequency of 2.4576MHz is chosen because 50Hz and 60Hz may be obtained by direct division as well as the popular communications frequencies of 19.2kHz and 9.6kHz.
The first notch frequency is 3.82 times the -3 dB frequency, so the notch frequency must be chosen so that the maximum signal frequency falls within the filter passband.

The lower the notch frequency, the lower the noise bandwidth, and therefore the higher the effective resolution of the converter. Moreover, the PGA gain will also set limits on the achievable resolution. With a 2.5V span, 1 LSB in a 24-bit system is only 150nV - with a gain of 128 it is 1.2nV!

As is evident from their pipeline architecture, sigma-delta ADCs have a conversion time which is related to the bandwidth of the digital filter:- the narrower the bandwidth, the longer the conversion. For a 10Hz notch frequency, the AD7714 has a 10Hz output data rate.

When the input to a sigma-delta ADC changes by a large step, the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not, but the time taken to change channels can be inconvenient. In the case of the AD771X-series, four conversions must take place after a channel change before the output data is again valid (Figure 3.23). The SYNC input pin resets the digital filter, and if it used, data is valid on the third output afterwards, saving one conversion cycle (when the internal multiplexer is switched, the SYNC is automatically operated). The SYNC input also allows several AD771X ADCs to be synchronized.
Although the AD771X sigma-delta ADCs are 24-bit devices, it is not possible to obtain 24 bits of useful resolution from a single sample because internal ADC noise limits the accuracy of the conversion. We thus introduce the concept of "Effective Resolution," or "Effective Number of Bits," ENOB. This is a measure of the useful signal-noise ratio of an ADC.

Noise in the ADC is generated by unwanted signal coupling and by components such as resistors and active devices. There is also intrinsic quantization noise which is inescapably linked to the analog-digital conversion process. As discussed in the first part of this section, sigma-delta ADCs use special techniques to shape their quantization noise and thus reduce their oversampling ratio for a given ENOB, but they cannot eliminate quantization noise entirely.

In an ideal noise-free ADC, it is possible to position a dc input signal so that the ADC digital output is always the same code from sample to sample. There is no quantization noise present, because only one code is being exercised. In a real-world high resolution ADC, however, there are internal noise sources which can cause the output code to change from sample to sample for a constant-value dc input signal. Figure 3.24 shows the comparison between an ideal ADC and an one which has internal noise. The results are plotted as a histogram, where the vertical axis represents the number of occurrences of each code out of the total number of 5000 samples used in this example. In the ideal ADC, all 5000 samples result in the same output code. In the practical ADC, however, internal noise generally results in a distribution of codes, centered around the primary code. In most cases, the noise is Gaussian, and a normal distribution can be fitted to the points on the histogram. The standard deviation of this distribution, sigma, represents the rms value of the sum of all internal noise sources reflected to the ADC output, measured in LSBs. This of course assumes a noise-free input. The rms value in LSBs can be converted easily to an effective rms voltage noise.
The signal-to-noise ratio can then be computed by dividing the full scale ADC input range by the rms noise computed from the histogram. The full scale input range for the AD771X-series is equal to twice the reference voltage divided by the gain of the PGA, and the equation for calculating the effective resolution in bits is given by:

\[
\text{Effective Resolution} = \log_2 \left( \frac{2 \times V_{\text{REF}}}{\text{gain}} \cdot \frac{1}{\text{RMS Noise}} \right)
\]

**Determining Effective Resolution**

- Effective Resolution (ENOB) = \( \log_2 \left( \frac{\text{Full Scale Signal}}{\text{RMS Noise}} \right) \)
- Output RMS Noise = Effective Noise in the Digital Output Code
- ENOBs is Greatest at Low Filter Frequency and Low Gain

Figure 3.25

Figure 3.26 shows how RMS noise in an AD7714 varies with gain and notch frequency. Figure 3.27 gives the same results in terms of effective resolution, or ENOB using the previous equation. The effective output noise comes from two sources. the first is the electrical noise in the semiconductor devices used in the implementation of the ADC front end and the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added.
The device noise is at a low level, and is largely independent of frequency. The quantization noise starts at an even lower level, but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100Hz approximately for \( f_{\text{clk}} = 2.4576 \text{MHz} \) tend to be device-noise dominated, while higher notch settings are dominated by quantization noise. Reducing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA, and therefore effective resolution suffers a little at high gains for lower notch frequencies.

Additionally, in the device-noise dominated region, the output noise (in \( \mu \text{V} \)) is largely independent of reference voltage, while in the quantization-noise dominated region, the noise is proportional to the value of the reference.

![Figure 3.26: Noise Variation as a Function of Gain and Filter Cutoff Frequency (AD7714-5, Unbuffered Mode, Clock = 2.4576 MHz)](image)

![Figure 3.27: Effective Resolution Versus Gain and First Notch Frequency (AD7714-5, Unbuffered Mode, Clock = 2.4576 MHz)](image)
It is important to distinguish between RMS and peak-to-peak noise. Noise in a sigma-delta ADC has a Gaussian (or near Gaussian) distribution. This means that if one waits long enough, any value of peak noise will eventually occur, and it is not possible to write a specification absolutely prohibiting a specified value of noise peak. For practical purposes, the peak-to-peak noise is defined as 6.6 times the RMS noise, since such peaks occur less than 0.1% of the time. The noise specified in the ENOB table in Figure 3.27 is expressed in RMS terms. If a figure for "noise-free" code resolution is required, it will be approximately 3-bits worse: 20-bits ENOB becomes 17-bits noise-free code, etc. Since most applications are concerned with noise power, however, the RMS ENOB figure is the more commonly used.

This does not mean that the original 24-bit resolution has no value, however. Additional external filtering, to narrower bandwidths than the internal filter, can further improve the resolution and ENOB at the expense of longer conversion times. The histogram approach using a large number of samples can also be used to more accurately define the input signal.

**ESTIMATING NOISE-FREE CODE RESOLUTION**

- **Determined Using Peak-to-Peak Noise**
- **Output RMS Noise** × 6.6 = **Peak-to-Peak Noise**
- **Factor of 6.6 is Approximately Equal to 3 bits:**
  \[ \log_2 (6.6) = 2.72 \]
- **Therefore, subtract 3 bits from Effective Resolution Given in Figure 3.27 to Determine Noise Free Code Resolution**

Figure 3.28

The results in Figures 3.27 and 3.28 assume the use of a low noise, heavily decoupled external reference and a noise-free analog input. Noisy inputs (and the reference is an input) reduce the effective resolution. For this reason, careful attention must be paid to external noise sources. Figure 3.29 lists aspects of board layout which may affect system noise, and hence the ENOB of the AD771X-series.
OPTIMIZING NOISE PERFORMANCE

- Pay Attention to Layout!
- Use Ground Planes
- Keep Analog PCB Tracks Short
- Interface Directly with Transducer
- Use Low Noise Amplifiers (AD797, OP-213, OP-177, AD707) (Only if Required)
- Connect Analog and Digital Grounds of Converters Together at the Device, and Connect them to Analog Ground Plane
- Route Digital PCB Tracks Clear of Analog Tracks
- Filter Signal and Reference Inputs
- Minimize Reference Noise
- The Evaluation Board is an Example of Good Layout

Figure 3.29

The AD771X-series is designed to interface directly with most transducers without the need for external buffering or amplification. If external amplifiers are used, however, low noise devices such as the OP-213 and AD797 should be chosen. To determine if external amplifiers will lower the AD771X system resolution, the total additional noise (in the bandwidth 0.1 Hz to the cutoff frequency set in the AD771X) should be calculated and compared with the RMS noise figures given in Figure 3.26. (Uncorrelated noise adds by root sum of squares, so if the additional noise is <50% of the AD7710 noise, it may be ignored; but if it exceeds this level, its effect on system performance must be studied carefully.)

An external filter on the input of the AD771X-series can improve its noise performance, because the modulator does not reject noise at integer multiples of the sampling frequency. This means that there are frequency bands $\pm f_{3dB}$ wide ($f_{3dB}$ is the cutoff frequency of the internal digital filter) where noise passes unattenuated to the output. However, due to the AD771X high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. The internal analog front end provides some filtering at these frequencies (the attenuation at 19.2kHz is approximately 70dB), but high level wideband noise can degrade system ENOB. A simple external RC low-pass filter is generally sufficient to minimize the effects of this noise, but the resistor and capacitor must be carefully chosen so that the gain accuracy of the AD771X is not affected. If the AD7714 is used in the buffered mode (i.e. the internal buffer is active), this restriction does not apply.
INPUT FILTER HELPS REDUCE WIDEBAND NOISE

A simplified model of the analog input of the AD7714 in the unbuffered mode is shown in Figure 3.31 (The AD7710, AD7711, AD7712, and AD7713 have similar structures). It consists of a resistor of approximately 7kohm (input multiplexer on-resistance) connected to the input terminal and to an analog switch which switches a 7pF sampling capacitor between the resistor and ground, with a mark-space ratio of 50%. The switching frequency depends on \( f_{\text{clkin}} \) and the gain which is being used: with a gain of unity and the standard clock frequency of 2.4576MHz, the switching frequency is 19.2kHz, and at gains of 2, 4, and 8 or more it is 38.4, 76.8, and 153.6kHz respectively.

If the converter is working to an accuracy of 20-bits, the capacitor must charge with an accuracy of 20-bits. The input RC time constant due to the switch on-resistance (7kohm) and the sampling capacitor (7pF) is 49ns. If the charge is to achieve 20-bit accuracy, it must charge for at least 14x the time constant, or 686ns. Any external resistor in series with the input will increase the time constant, and the chart in Figure 3.31 shows acceptable values of series resistance necessary to maintain 20-bit performance.

To determine the minimum charge time for 20-bit performance with an external resistance \( R_{\text{ext}} \) we use the equation:

\[
\text{Minimum Charge Time} = 14(R_{\text{ext}} + 7\text{kohm}) \times 7\text{pF}
\]

The minimum charge time must be less than half the period of the switching signal used (it has a 50% duty cycle). The fastest switching frequency with the standard 2.4576MHz clock is 153.6kHz (for a gain of 8 or greater), and half of that clock period is 3.3\( \mu \text{s} \), which allows a maximum \( R_{\text{ext}} \) of 26.8kohm. At lower gains \( R_{\text{ext}} \) may be larger.
It is not practical to use $R_{\text{ext}}$ in conjunction with a capacitor to ground from the input pin of the AD7710, AD7711, AD7712, or AD7713 (or the AD7714 operating in the unbuffered mode) to make an anti-aliasing filter (with a cutoff frequency less than one-half the input sampling frequency), unless the capacitor is dramatically larger than the 7pF $C_{\text{int}}$. This is because $C_{\text{int}}$ is discharged on every sampling clock cycle and will recharge from the filter capacitor. Therefore, either the filter capacitor must be so large that charging $C_{\text{int}}$ from it changes its voltage by less than an LSB at 20-bits (i.e. it is larger than 7µF), or the time constant $R_{\text{ext}}C_{\text{ext}}$ must be short enough for $C_{\text{ext}}$ to recharge before the next clock cycle - in which case the cutoff frequency due to $R_{\text{ext}}$ and $C_{\text{ext}}$ is not low enough to make an anti-aliasing filter with respect to the sampling frequency. There may, however, be some benefit in such a filter if there is input noise at high frequencies. The data sheets for the AD771X-series contain tables which give the allowable external capacitor and resistor values as a function of PGA gain for 16-bit and 20-bit gain accuracy (see Figure 3.32).

Note that if an external $R_{\text{ext}}$ and $C_{\text{ext}}$ are used, the capacitor type must have low non-linearities and dielectric absorption. Film types such as polystyrene or polypropylene are recommended.
AD7714 EXTERNAL FILTER RESTRICTIONS ON R AND C FOR NO 20-BIT GAIN ERROR (UNBUFFERED MODE ONLY)

<table>
<thead>
<tr>
<th>GAIN</th>
<th>EXTERNAL CAPACITOR (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>290 kΩ</td>
</tr>
<tr>
<td>2</td>
<td>141 kΩ</td>
</tr>
<tr>
<td>4</td>
<td>63.6 kΩ</td>
</tr>
<tr>
<td>8 - 128</td>
<td>25.8 kΩ</td>
</tr>
</tbody>
</table>

Figure 3.32

The advantage of the AD7714 operating in the buffered mode is that a true input antialiasing filter can be used without affecting the gain accuracy. The penalty is only a slight increase in noise (approximately 10%) and a small reduction in input common-mode voltage range. If the value of the series resistor is large, the effects of the input bias current must be considered, but this error can be removed using the calibration modes.

Some successive approximation and subranging ADCs draw large transient currents at their analog and reference inputs which load their respective drive circuitry and cause errors. Often, special drive amplifiers with low output impedance at frequencies well above the conversion clock frequency are necessary to avoid this problem, but these problems do not occur with the very small transient loads of the AD771X devices. The oscilloscope photograph in Figure 3.33 shows the transient current in an AD7710. It was taken with a 1kohm resistor in series with the input to measure the change in current. This circuit produces a 15mV spike of less than 1µs duration. The corresponding peak pulse current is only 15µA, which permits the use of quite high impedance signal sources with no risk of degrading the ENOB. As discussed earlier, the AD7714 operating in the buffered mode has no significant transients on its analog input.
The AD771X family was designed to simplify transducer interfacing. Many types of transducers can be connected directly to the input of one of the AD771X family without additional circuitry, but some care is necessary to achieve the best possible accuracy:- noise needs to be minimized (a simple capacitor across a resistive sensor may be all the filtering that is needed, but this must be checked - noise is particularly important, because noise cannot be removed by the system calibration which eliminates gain and offset errors); transducer source impedance may affect charge times (as mentioned above); and bias currents flowing in high impedance transducers may cause errors, although these can be removed by system calibration. In general, system calibration can remove most dc errors in systems using the AD771X family.
TRANSDUCER CONNECTION CONSIDERATIONS

- Filter Noisy Signals
- Use Shielded, Twisted Pair Cable (Shield Grounded at AGND/DGND Connection Point at ADC, floating at transducer)
- DC Leakage (bias) Current = 10pA can cause offset with $R_{source}$
- This causes drift over temperature
- To Maintain Accuracy:
  - Minimize $R_{source}$
  - Use Differential inputs and balance $R_{source}$
  - Use system calibration techniques

Figure 3.34

Circuitry connected to transducers must generally be protected against over-voltage from ESD, noise pickup, or accidental shorts. If signals are likely to go outside the positive or negative supplies, some form of clamp is necessary to keep them within them. Figure 3.35 shows a suitable circuit for protecting AD771X devices. The AD7710 has internal ESD protection diodes between the input and both supplies which conduct when the input exceeds either supply by more than about 0.6V. Excessive current in these diodes will vaporize metal tracks on the chip and damage the circuit, so an external resistor, $R_p$, is necessary to limit current to a safe 5mA during over-voltage events. $R_p$ may be determined by a simple calculation:

$$R_p = \frac{V_{max} - V_{supply}}{5mA}$$

$R_p$ will contribute noise to the system (the basic Johnson noise equation applies):

$$e_n = \sqrt{4kTBR_p}$$

where k is Boltzmann’s Constant, T is the absolute temperature and B is the bandwidth). If the noise due to $R_p$ is too high, $R_p$ can be reduced if external Schottky diodes are used in addition to the diodes on the chip.
There are no special requirements for these Schottky diodes, as long as they have low leakage current and can handle the necessary fault current levels while maintaining a low turn-on voltage.

As important as the analog signal input is the reference input. Figure 3.36 shows a simplified model of the reference input, which is very similar to that of the analog input (with the exception of the AD7714 operating in the buffered mode). The series resistor is 5kohm, and the value of the capacitor depends on the gain setting and the particular device. For gains of 1-8, the capacitor is approximately 7pF for the AD7714. Above 8, the capacitor's value is halved for each doubling of gain. The value of the capacitor (G = 1-8) for other members of the AD771X series is 20pF.
An important consideration in choosing a reference for the AD771X-series is noise. Many references have output noise which exceeds that of the AD771X and cause reduced accuracy. Filtering may help in such cases, but a low noise reference should be selected wherever possible.

Although the AD7710, AD7711, and AD7712 have internal +2.5V references which may be connected to their positive reference input, their use will degrade the effective resolution of the ADCs by approximately 1 bit for filter cut-off frequencies of 60Hz or less. The noise calculations using the AD7710 internal reference are shown in Figure 3.37. For optimum noise performance, a low noise external reference such as the AD780 should be used as shown in Figure 3.38.

**INTERNAL REFERENCE VOLTAGE NOISE CONSIDERATIONS FOR AD7710, AD7711, AD7712 ADCs**

- Specified Output Noise of AD7710, AD7711, AD7712 Internal +2.5V Reference
  - $8.3 \mu V$ rms typical (0.1 to 10Hz)
  - $3.4 \mu V$ rms (0.1 to 2.62Hz, for 10Hz Output Rate)

- Reference Noise adds to intrinsic ADC noise:
  - AD7710 Noise = $1.7 \mu V$ rms (G = +1)
  - Total Noise = $\sqrt{(1.7 \mu V)^2 + (3.4 \mu V)^2} = 3.8 \mu V$ rms, or 25 $\mu V$ p-p

- This reduces effective resolution from 21.5 to 20.5 bits
- Use low-noise external reference for highest resolution at low input bandwidths

**Figure 3.37**

**USE A LOW NOISE EXTERNAL REFERENCE FOR OPTIMUM NOISE PERFORMANCE AND RESOLUTION**

- AD780 has 4$\mu V$ peak-to-peak noise is 0.1 to 10Hz bandwidth.
- In a 2.62Hz bandwidth (notch frequency = 10Hz), the rms value of the noise is 0.31$\mu V$ rms
- Well below the noise of the AD771X

**Figure 3.38**
The AD780 2.5V reference has noise of 4µV p-p in the range 0.1 to 10Hz. This is equivalent to 0.606µV rms (obtained by dividing the peak-to-peak value by 6.6). This gives 0.31µV rms noise in the 2.62Hz bandwidth associated with a 10Hz update rate. This is negligible compared to the AD7710 inherent noise of 1.7µV rms (G = 1). With output rates of 1kHz or more, and cutoff frequency of 262Hz, the noise of the AD780 may be reduced by 50% if a 0.1µF capacitor is connected to its output (unlike many IC voltage references, the AD780 is stable with all values of capacitive load).

CALCULATING REFERENCE NOISE CONTRIBUTION

- If reference noise is given as a spectral density, \( V_n (nV/\sqrt{Hz}) \) rms,
  \[
  V_{\text{refnoise}} = V_n \sqrt{BW}, \text{ where } BW = 0.262 f_{\text{notch}}
  \]
- If reference noise is given as a peak-to-peak value in the 0.1 to 10Hz bandwidth, \( V_{p-p} \), then
  \[
  V_n = \frac{V_{p-p}}{6.6 \cdot \sqrt{10Hz}}
  \]
  \[
  V_{\text{refnoise}} = \frac{V_{p-p}}{6.6 \cdot \sqrt{10Hz}} \cdot \sqrt{BW}, \text{ BW = 0.262 } f_{\text{notch}}
  \]
- Above are approximations, but are sufficiently accurate for estimation of reference noise
- Reference noise should be no greater than 50\% of ADC noise

Figure 3.39

The AD780 is also a suitable reference for the AD7714 ADC, whose noise with a 10Hz update rate (G = 1, Vsupply = +5V) is 1.0µV rms. When the AD7714 is operating on a +3V supply, it requires a low-noise 1.25V reference, and the AD589 is a suitable choice.

When the AD771X-series ADCs are operated at higher output rates and higher input bandwidths, the ADC noise is significantly higher, and less effective resolution is required. This allows the use of higher noise, lower power references such as the REF192 (25µV p-p noise, 0.1 to 10Hz) which only requires 45µA of quiescent current, compared to 0.75mA for the AD780.

Regardless of the reference selected, it should be properly decoupled in order to act as a charge reservoir to transient load currents as well as a filter for wideband noise. This implies that the reference must be stable under capacitive loads, which is not necessarily the case in all references. In fact, some references actually require an external decoupling capacitor in order to maintain stability. Regardless of the reference selected, the data sheet should be carefully examined with respect to output capacitive loading. Further information on applying voltage references can be obtained in References 5, 6, and 7.
DC errors also affect conversion accuracy, but AD771X devices can calibrate themselves to correct dc errors. The AD7710, AD7711, AD7712, and AD7713 have four different calibration modes. These are summarized in Figure 3.41 and comprise Self Calibration, System Calibration, System-Offset Calibration, and Background Calibration. Each calibration cycle contains two conversions, one each for zero-scale and for full-scale calibration. The calibration modes for the AD7714 are similar, except that in the Background-Calibration Mode, only zero-scale is calibrated.

To initiate a calibration cycle, the appropriate code must be sent to the control register. After the code is sent, the AD771X automatically conducts the entire operation, and clears the control register of the calibration command so that a separate command to stop calibration is not necessary. Since the filter in the sigma-delta converter must purge itself of its previous result for four output update cycles whenever the input sees a full-scale step the total calibration operation takes nine such cycles.

Self Calibration removes errors in an AD771X by connecting the input to ground and performing a conversion, and then connecting the input to $V_{\text{ref}}$ and performing another. The results of these conversions are used to calibrate the device.
Background Calibration is a variation of Self Calibration. The only difference is that when an AD771X is placed in Background Calibration mode, it continually calibrates itself at regular intervals without further instructions. This ensures that the AD771X remains calibrated regardless of drift. The Background Calibration cycle alternates calibration conversions with signal conversions: zero calibrate/convert signal/full-scale calibrate/convert signal/zero calibrate/etc. This provides continuous calibration but reduces the output data rate by a factor of six. Background Calibration for the AD7714 only calibrates zero-scale.

System Calibration is intended to calibrate all the elements prior to the ADC which may contribute to system errors, as well as the ADC itself. (For example an instrumentation amplifier introduces errors into a system due to its own offset, drift and gain error. These errors can be removed by System Calibration.) However, System Calibration requires additional analog switches to connect system inputs to ground and a reference as well as to the original signal source. The first step in System Calibration requires external grounding of the system input terminal to calibrate out offsets. The second step requires that the input be connected to a reference, which calibrates gain error at full-scale. The System Calibration cycle requires the sending of two separate instructions to the control register as well as control of the analog switches at the system input. It must be repeated regularly to correct for drift with time and temperature.

The final calibration mode is System-Offset Calibration. This calibrates system offsets, and the AD771X gain. Again, it requires external analog switches at the system input, and separate instructions for zero and gain calibration. For the first cycle, the system input is connected to ground and the AD771X calibrates for system offsets. During the second cycle, the ADC input is connected to the reference for ADC gain calibration.

**CALIBRATION ISSUES**

- Always calibrate on power-up!
- Background calibration sequence: (Zero-Scale, Convert, Fullscale, Convert, Zero-Scale, Convert, . . . ) AD7710, AD7711, AD7712, AD7713
  
  This reduces the data rate by a factor of 6.
- DRDY signals when calibration cycle is complete by going low.
- DRDY may already be low if a conversion is taking place.

*Figure 3.42*
When calibration is complete, DRDY goes low - but it does not necessarily go high as soon as the calibration command is sent to the ADC, there may be a delay of up to one output data cycle before it does so. Controllers should therefore look for a 0 to 1 transition, rather than the presence of a 0, on DRDY to signal the completion of a calibration after it has been commanded.

Calibration is crucial to achieving the rated accuracy of AD771X devices and should be performed immediately after power-up and repeated regularly. A 1.25µV/°C temperature coefficient of input offset and a 2°C temperature change causes an LSB of error in a 20-bit 2.5V system. Any reference drift adds to the error. Frequent calibration ensures that temperature changes do not degrade the accuracy of conversions.

**CALIBRATE OFTEN TO MAINTAIN ACCURACY**

- Temperature Drift can cause errors
  - Unipolar offset drift of 2.5µV is 1 LSB in a 20 bit system (2.5V full-scale)
- Reference voltage drift adds to this error
- Calibration can remove gain errors created by input filters
- Therefore, to minimize errors, calibrate often.
- Always calibrate on power-up!
- Calibration coefficients can be manually adjusted

*Figure 3.43*

When the AD771X executes a calibration cycle, it saves two coefficients in internal registers. One register stores the full scale calibration coefficient, FSC, and the other stores the zero scale calibration coefficient, ZSC. Adjusting the calibration coefficients manually may be useful in some applications. For example, in a weigh scale application it may be necessary to insert an offset to account for a fixed weight. It is possible to read from and write to the calibration registers of members of the AD771X family, making adjustment of calibration coefficients a straightforward task. Details of this procedure are given in References 4 and 8.

A typical application of the AD7710 is in a weigh scale (Figure 3.44). These generally use a resistive bridge as their sensing element and require resolution of at least 16-bits and often more. The AD7710 dramatically simplifies the design of such a system: the bridge is connected directly to its differential inputs, making an external instrumentation amplifier unnecessary. The excitation for the bridge, and the reference for the AD7710, are provided by an AD780, whose low noise helps to preserve the system ENOB. Because the system bandwidth is limited (both by the conversion rate selected and the filter capacitors on the bridge) the ENOB achievable is quite high (approximately 20-bits) but the conversion (and output data) rate is rather low at 10Hz.
The converters in the AD771X family all have serial interfaces, which are described in greater detail in the data sheet. They have control registers that control all their operations. Changing the PGA gain, starting a calibration, and changing the filter parameters are all accomplished by writing to the appropriate register. On the other hand, data can be read either as a 16-bit or a 24-bit operation - one of the bits in the control register controls the size of the data word. The DRDY output indicates when a conversion is complete and valid data is available in the output register.

Figure 3.45 shows an isolated 4-wire interface to the AD7713 using common opto-isolators. Over 6kV of isolation is possible. The TFS, A0, and SYNC lines are tied together at the converter to minimize the number of control lines. Tying TFS to AO causes a write to the device to load data to the control register, and any read accesses the data register. The only restrictions of this method of control is that the controller cannot write to the calibration registers and cannot read from the control register. In many applications these capabilities are unnecessary. Four opto-isolators carry data and instructions from the controller to the ADC and a fifth, with a 74HC125 on each side of the isolation barrier, carries data to the controller. The AD7713 is ideal for this particular application because its low supply current minimizes the load on the isolated power supply.
The AD771X family generally interfaces with some type of microprocessor. Their data sheet includes circuits and micro-code for interfacing to the 8051 and 68HC11 microcontroller and the ADSP-2103/2105 DSP processor. Figure 3.46 shows how the AD7714 may be interfaced to the 68HC11 microcontroller. The diagram shows the minimum (three-wire) interface with CS on the AD7714 hard-wired low. In this scheme, the DRDY bit of the AD7714 Communications Register is monitored to determine when the Data Register is updated. Other schemes are described in the AD7714 data sheet.
Interfacing to the ADSP-2103/2105 is also relatively straightforward. The DRDY bit of the Communications Register is again monitored to determine when the Data Register in the AD7714 is updated.
The AD771X sigma-delta converters are powerful tools for building high accuracy systems. Every one of them combines high resolution, system calibration, a programmable gain amplifier, and high impedance differential inputs with great ease of design. Their adjustable digital filters provides flexibility in the choice of data rates and resolution and their serial interface minimizes their pin count, so that they fit in a 24-pin skinny DIP package, providing a high degree of functionality in a small space.

The AD7714 is especially suitable for low power applications. Figure 3.48 shows the total supply current required as a function of supply voltage for two clock frequencies: 2.4576MHz and 1MHz. These data are for an external clock with the AD7714 operating in the unbuffered mode. Figure 3.48 illustrates an important point which is applicable to a large number of low power data converters - the total power dissipation is a function of the clock frequency! Make sure to check the data sheet carefully for this dependency when estimating the total power requirement. The power dissipation of older, higher-power, bipolar data converters was generally much less sensitive to clock frequency than the modern low-power CMOS designs.
An area where the low power, single supply, three wire interface capabilities of the AD7714 is of benefit is in smart transmitters (Figure 3.49). The entire smart transmitter must operate from the 4mA to 20mA loop. Tolerances in the loop mean that the amount of current available to power the entire transmitter is as low as 3.5mA. The AD7714 consumes only 500µA, leaving 3mA available for the rest of the transmitter. Not shown in Figure 3.49 is the isolated power source required to power the front end circuits, including the AD7714.
REFERENCES


4. **AD7710, AD7711, AD7712, AD7713, AD7714 Data Sheets**, Analog Devices.


SECTION 4

HIGH SPEED SAMPLING ADCs

- ADC Dynamic Considerations
- Selecting the Drive Amplifier Based on ADC Dynamic Performance
- Driving Flash Converters
- Driving the AD9050 Single-Supply ADC
- Driving ADCs with Switched Capacitor Inputs
- Gain Setting and Level Shifting
- External Reference Voltage Generation
- ADC Input Protection and Clamping
- Applications for Clamping Amplifiers
- Noise Considerations in High Speed Sampling ADC Applications
Modern high speed sampling ADCs are designed to give low distortion and wide dynamic range in signal processing systems. Realization of specified performance levels depends upon a number of factors external to the ADC itself, including proper design of any necessary support circuitry. The analog input drive circuitry is especially critical, because it can degrade the inherent ADC dynamic performance if not designed properly.

Because of various process and design-related constraints, it is generally not possible to make the input of a high speed sampling ADC totally well-behaved, i.e., high impedance, low capacitance, ground-referenced, free from glitches, impervious to overdrive, etc. Therefore, the ADC drive amplifier must provide excellent ac performance while driving what may be a somewhat hostile load (depending upon the particular ADC selected).

The trend toward single-supply high speed designs adds additional constraints. The input voltage range of high speed single-supply ADCs may not be ground referenced (for valid design reasons), therefore level shifting with single-supply op amps (which may have limited common-mode input and output ranges) is usually required, unless the application allows the signal to be ac coupled.

Although there is no standard high speed ADC input structure, this section addresses the most common ones and provides guidelines for properly designing the appropriate input drive circuitry.

Some sampling ADCs also require external reference voltages. In other cases, performance improvements can be realized by using an external reference in lieu of an internal one. It is equally important that these reference circuits be designed with utmost care, since they too affect the overall ADC performance.
HIGH SPEED, LOW VOLTAGE SAMPLING ADCs

- Key Specifications for sampling ADCs:
  - Distortion
  - Noise
  - Distortion Plus Noise
  - Effective Number of Bits
  - Bandwidth (Full Power and Small Signal)
  - Sampling Rate

- Modern Trends
  - Low Power: CMOS, BiMOS, or XFCB Processes
  - Low Voltage: ±5V, +5V, +5V (Analog) / +3V (Digital)
  - Input Voltage Ranges not always Ground-Referenced
  - Analog Input Can Generate Transient Currents

Figure 4.1

ADC Dynamic Considerations

In order to make intelligent decisions regarding the input drive circuitry, it is necessary to understand first exactly how the dynamic performance of the ADC is characterized. Modern signal processing applications require ADCs with wide dynamic range, high bandwidth, low distortion, and low noise. As well as having traditional dc specifications (offset error, gain error, differential linearity error, and integral linearity error), sampling ADCs (ADCs with an internal sample-and-hold function) are generally specified in terms of Signal-to-Noise Ratio (SNR, or S/N), Signal-to-Noise-Plus Distortion Ratio [S/(N+D), or SINAD], Effective Number of Bits (ENOB), Harmonic Distortion, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD+N), Intermodulation Distortion (IMD), and Spurious Free Dynamic Range (SFDR). Sampling ADC data sheets may provide some, but not all of these ac specifications. The ac specifications are usually tested by applying spectrally pure sinewaves to the ADC and analyzing its output in the frequency domain with a Fast Fourier Transform (FFT). The process is similar to using an analog spectrum analyzer to measure the ac performance of an amplifier. Because of the quantization process, however, an ADC produces some errors not found in amplifiers.
ADC DYNAMIC PERFORMANCE SPECIFICATIONS

- Distortion Specifications: (Narrowband)
  - Harmonic Distortion
  - Total Harmonic Distortion (THD)
  - Spurious Free Dynamic Range (SFDR)
  - Intermodulation Distortion (IMD), Two-Tone Input

- Noise Specifications: dc to \( f_s / 2 \)
  - Signal-to-Noise Ratio without Harmonics (often called SNR, or S/N)

- Noise Plus Distortion Specifications: dc to \( f_s / 2 \)
  - Signal-to-Noise and Distortion (S/N+D, SINAD), but often referred to as SNR (check definition carefully when evaluating ADCs), often converted to Effective Bits (ENOB)
  - Total Harmonic Distortion Plus Noise (THD + N)

- Broadband Noise can be reduced by filtering or averaging

Figure 4.2

An ideal N-bit ADC, sampling at a rate \( f_s \), produces quantization noise having an rms value of \( q/\sqrt{12} \) measured in the Nyquist bandwidth dc to \( f_s / 2 \), where \( q \) is the weight of the Least Significant Bit (LSB). The value of \( q \) is obtained by dividing the full scale input range of the ADC by the number of quantization levels, \( 2^N \). For example, an ideal 10-bit ADC with a 2.048V peak-to-peak input range has \( 2^{10} = 1024 \) quantization levels, an LSB of 2mV, and an rms quantization noise of \( 2mV/\sqrt{12} = 577\mu V \) rms. The derivation of the theoretical value of quantization noise, \( q/\sqrt{12} \), makes the assumption that the quantization noise is not correlated in any fashion to the input signal, and may therefore be treated as Gaussian noise. This is normally true, but in certain cases where the input sinewave frequency happens to be an exact submultiple of the sampling rate, the quantization noise may tend to be concentrated at the harmonics of the input signal, even though the rms value is still approximately \( q/\sqrt{12} \).

Another way to express quantization noise is to convert it into a Signal-to-Noise ratio by dividing the rms value of the input sinewave by the rms value of the quantization noise. Normally, this is measured with a full scale input sinewave, and the expression relating the two is given by the well-known equation,

\[
\text{SNR} = 6.02N + 1.76\text{dB}.
\]

An actual ADC will produce noise in excess of the theoretical quantization noise, as well as distortion products caused by a non-linear transfer function. An FFT is used to calculate the rms value of all the distortion and noise products, and the actual
signal-to-noise-plus-distortion, S/(N+D), is computed. The above equation is solved for N, yielding the well-known expression for Effective Number of Bits, ENOB:

\[
ENOB = \frac{S/(N+D)_{\text{ACTUAL}} - 1.76\text{dB}}{6.02}.
\]

For example, if a 10-bit ADC has an actual measured S/(N+D) of 56dB (theoretical would be 61.96dB), then it will have 9 effective bits, i.e., the non-ideal 10-bit ADC yields the same performance as an ideal 9-bit one.

**EFFECTIVE NUMBER OF BITS (ENOB)**

**INDICATES OVERALL DYNAMIC PERFORMANCE OF ADCs**

- S/(N+D) = 6.02N + 1.76dB (Theoretical)
- ADC ACHIEVES S/(N+D) = XdB (Actual)
- ENOB = (XdB - 1.76dB) / (6.02dB)
- ENOB Includes Effects of All Noise and Distortion in the bandwidth DC to \(f_s/2\)

**Figure 4.3**

Even well-designed sampling ADCs have non-linearities which contribute to non-ideal low frequency performance, and additionally, performance degrades as the input frequency is increased. A useful way to evaluate the ac performance of ADCs is to plot Signal-to-Noise Plus Distortion, S/(N+D), (or convert it to ENOB) as a function of input frequency. This measurement is somewhat all-inclusive and includes the effects of both noise and distortion products.

In some instances, SNR may be specified both with and without the distortion products, and in other cases, distortion may be specified separately, either as individual harmonic components, or as total harmonic distortion (THD). Spurious Free Dynamic Range (SFDR) is simply another way of describing distortion products and is the ratio of the signal level to the worst frequency spur, under a given set of conditions. Intermodulation Distortion (IMD) is measured by applying two tones (F1 and F2) to the ADC and determining the ratio of the power in one of the tones to the various IMD as shown in Figure 4.4. Unless otherwise specified, the third-order products which occur at the frequencies 2F1 – F2 and 2F2 – F1 are the ones used in the measurement because they lie close to the original tones and are difficult to filter.
If we plot the gain of an amplifier with a small signal of a few millivolts or tens of millivolts, we find that as we increase the input frequency, there is a frequency at which the gain has dropped by 3 dB. This frequency is the upper limit of the small signal bandwidth of the amplifier and is set by the internal pole(s) in the amplifier response. If we drive the same amplifier with a large signal so that the output stage swings with its full rated peak-to-peak output voltage, we may find that the upper 3dB point is at a lower frequency, being limited by the slew rate of the amplifier output stage. This high-level 3dB point defines the large signal bandwidth of an amplifier. When defining the large signal bandwidth of an amplifier, a number of variables must be considered, including the power supply, the output amplitude (if slew rate is the only limiting factor, it is obvious that if the large signal amplitude is halved, the large signal bandwidth is doubled), and the load. Thus large signal bandwidth is a rather uncertain parameter in an amplifier, since it depends on so many uncontrolled variables - in cases where the large signal bandwidth is less than the small signal bandwidth, it is better to define the output slew rate and calculate the maximum output swing at any particular frequency.

In an ADC, however, the maximum signal swing is always full scale, and the load seen by the signal is defined. It is therefore quite reasonable to define the large signal bandwidth (or full-power bandwidth) of an ADC and report it on the data sheet. In some cases, the small signal bandwidth may also be given.
ADC LARGE SIGNAL (OR FULL POWER) BANDWIDTH

- With Small Signal, the Bandwidth of a Circuit is limited by its Overall Frequency Response.
- At High Levels of Signal the Slew Rate of Some Stage May Control the Upper Frequency Limit.
- In Amplifiers There are so many Variables that Large Signal Bandwidth needs to be Redefined in every Individual Case, and Slew Rate is a more Useful Parameter for a Data Sheet.
- In ADCs the Maximum Signal Swing is the ADC’s Full Scale Span, and is therefore Defined, so Full Power Bandwidth (FPBW) may Appear on the Data Sheet.
- HOWEVER the FPBW Specification Says Nothing About Distortion Levels. Effective Number of Bits (ENOB) is Much More Useful in Practical Applications.

Figure 4.5

However, the large signal bandwidth tells us the frequency at which the amplitude response of the ADC drops by 3dB - it tells us nothing at all about the relationship between distortion and frequency. If we study the behavior of an ADC as its input frequency is increased, we discover that, in general, noise and distortion increase with increasing frequency. This reduces the resolution that we can obtain from the ADC.

If we draw a graph of the ratio of signal-to-noise plus distortion (S/N+D) against its input frequency, we find a much more discouraging graph than that of its frequency response. The ratio of S/N+D can be expressed in dB or as effective number of bits (ENOB) as discussed above. As we have seen, the SNR of a perfect N-bit ADC (with a full scale sinewave input) is (6.02N + 1.76)dB. A graph of ENOB against the variations of input amplitude can be depressing when we see just how little of the dc resolution of the ADC can actually be used, but can sometimes show interesting features: the ADC in Figure 4.6, for instance, has a larger ENOB for signals at 10% of FS at 1MHz than for FS signals of the same frequency. A simple frequency response curve cannot have plots crossing in this way.
The causes of the loss of ENOB at higher input frequencies are varied. The linearity of the ADC transfer function degrades as the input frequency increases, thereby causing higher levels of distortion. Another reason that the SNR of an ADC decreases with input frequency may be deduced from Figure 4.7, which shows the effects of phase jitter on the sampling clock of an ADC. The phase jitter causes a voltage error which is a function of slew rate and results in an overall degradation in SNR as shown in Figure 4.8. This is quite serious, especially at higher input/output frequencies. Therefore, extreme care must be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system. This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. A very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry.
A decade or so ago, sampling ADCs were built up from a separate SHA and ADC. Interface design was difficult, and a key parameter was aperture jitter in the SHA. Today, most sampled data systems use sampling ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a cause of concern if the SNR or ENOB is clearly specified, since a guarantee of a specific SNR is an implicit guarantee of an adequate aperture jitter specification. However, the use of an additional high-performance SHA will sometimes improve
the high-frequency ENOB of a sampling ADC, and may be more cost-effective than replacing the ADC with a more expensive one.

It should be noted that there is also a fixed component which makes up the ADC aperture time. This component, usually called effective aperture delay time, does not produce an error. It simply results in a time offset between the time the ADC is asked to sample and when the actual sample takes place (see Figure 4.9). The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications such as I and Q demodulation where several ADCs are required to track each other.

**EFFECTIVE APERATURE DELAY TIME**

![Figure 4.9](image)

The distortion produced by an ADC or DAC cannot be analyzed in terms of second and third-order intercepts, as in the case of an amplifier. This is because there are two components of distortion in a high performance data converter. One component is due to the non-linearity associated with the analog circuits within the converter. This non-linearity has the familiar "bow" or "s"-shaped curve shown in Figure 4.10. (It may be polynomial or logarithmic in form). The distortion associated with this type of non-linearity is sometimes referred to as soft distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner, and is a function of signal level. In a practical data converter, however, the soft distortion is usually much less than the other component of distortion, which is due to the differential nonlinearity of the transfer function. The converter transfer function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 4.10.
The actual location of the points of discontinuity depends on the particular data converter architecture, but nevertheless, such discontinuities occur in practically all converters. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level, and therefore such specifications as third order intercept point may be less relevant to converters than to amplifiers and mixers. For lower-amplitude signals, this constant level hard distortion causes the SFDR of the converter to decrease as input amplitude decreases. The soft distortion in a well-designed converter is only significant for high frequency large-amplitude signals where it may rise above the hard distortion floor.

In a practical system design, the ADC is usually selected based primarily on the required dynamic performance at the required sampling rate and input signal frequency, using one or more of the above specifications. DC performance may be important also, but is generally of less concern in signal processing applications. Once the ADC is selected, the appropriate interface circuitry must be designed to preserve these levels of ac and dc performance.

**SELECTING THE DRIVE AMPLIFIER BASED ON ADC DYNAMIC PERFORMANCE**

The ADC drive amplifier performs several important functions in a system. First, it isolates the signal source and provides a low-impedance drive to the ADC input. A low-impedance dc and ac drive source is important because the input impedance of the ADC may be signal-dependent, and the input may also generate transient load currents during the actual conversion process. A low source impedance at high frequencies minimizes the errors produced by these effects. Second, the drive amplifier provides the necessary gain and level shifting to match the signal to the ADC input voltage range.
FUNCTIONS OF THE ADC DRIVE AMPLIFIER

- Buffer the analog signal from the ADC input:
  - ADC input may not be a constant high impedance
  - ADC input may generate transient loads

- Provide other functions:
  - Gain
  - Level Shifting

- If the ADC input is constant high impedance with no transient loading, do not use a buffer amplifier unless required for gain or level shifting!!

Figure 4.11

The S/(N+D) plot of the ADC should generally be used as the first selection criterion for the drive amplifier. If the Total Harmonic Distortion Plus Noise (THD+N) of the drive amplifier is always 6 to 10dB better than the S/(N+D) of the ADC over the frequency range of interest, then the overall degradation in S/(N+D) caused by the amplifier will be limited to between approximately 0.5dB and 1db, respectively. This will be illustrated using two state of the art components: the AD9022 12 bit, 20MSPS ADC and the AD9631 op amp. A block diagram of the AD9022 is shown in Figure 4.12, and key specifications in Figure 4.13. AD9631/AD9632 key specifications are given in Figure 4.14.

The AD9022 employs a three-pass subranging architecture and digital error correction. The analog input is applied to a 300Ω attenuator and passed to the sampling bridge of the first internal track-and-hold amplifier (T/H). The held value of the first T/H is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These 5 bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal. A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again, the 5-bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the 3 least significant bits (LSBs) of the digital output and one bit of error correction. The digital error correction logic combines the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage is TTL (AD9022), or ECL (AD9023). Output data can be strobed on the rising edge of the ENCODE command.
AD9022 12-BIT, 20MSPS SAMPLING ADC

AD9022 ADC KEY SPECIFICATIONS

- 12-bit, 20MSPS Sampling ADC
- TTL Outputs (AD9023 has ECL outputs)
- On-Chip reference and SHA
- High Spurious Free Dynamic Range (SFDR):
  - 76dB @ 1MHz Input \( f_s = 20\text{MSPS} \)
  - 74dB @ 9.6MHz Input \( f_s = 20\text{MSPS} \)
- Analog Input Bandwidth: 110MHz
- Well-Behaved analog input with no transients
- Input Range: \pm 1.024V, Input Impedance: 300\( \Omega \), 5pF
- Dual Supplies (+5, -5.2V), 1.4W Power Dissipation

Figure 4.13
AD9632 OP AMP KEY SPECIFICATIONS

- Current-Feedback performance with voltage-feedback amps
- Small Signal Bandwidth:
  - 320MHz (AD9631, G = +1)
  - 250MHz (AD9632, G = +2)
- Low Distortion:
  - -113dBc @ 1MHz
  - -95dBc @ 5MHz
  - -72dBc @ 20MHz
- Slew Rate: 1300V/\mu s
- Settling Time: 16ns to 0.01%, 2V step
- Low Noise: Voltage: 7nV/√Hz, Current: 2pA/√Hz
- ±3V to ±5V Supply Operation, 17mA Supply Current

Figure 4.14

Figure 4.15 shows the THD+N of the AD9631 drive amplifier superimposed on the S/(N+D) plot for the AD9022 ADC (12-bits, 20MSPS). Notice that the amplifier THD+N is at least 10dB better than the ADC S/(N+D) for input frequencies up to about 10MHz (the Nyquist frequency). In performing this comparison, it is important that the data for the op amp be obtained under the final operating conditions encountered in the actual circuit, i.e., gain, signal level, power supply voltage, etc.

Figure 4.15
While \( S/(N+D) \) and THD+N are useful ac performance indicators, there are a number of applications where low distortion is more important than low noise. In spectral analysis using FFTs, or other applications where averaging techniques can be used to reduce the effects of noise, the amplifier THD and the ADC distortion (generally SFDR) should be used as the selection criteria. These characteristics should be plotted on the same scale, and the drive amplifier THD should be at least 6 to 10dB better than the ADC SFDR over the frequency range of interest. Such a plot for the AD9631 op amp and the AD9022 ADC is shown in Figure 4.16.

![AD9022 ADC SFDR and AD9631 OP AMP THD Plotted as a Function of Input Frequency](image)

Figure 4.16

The above ac selection criterion works well if the ADC input is relatively benign, but may give overly optimistic results if the input impedance is signal dependent, or the input produces transient currents. The existence of either of these two conditions requires further investigation. The implications of signal-dependent input impedance will be demonstrated using a flash converter. Dealing with ADC input transient currents will be illustrated by examining a fast single-supply sampling ADC with a CMOS switched capacitor input stage.

**Driving Flash Converters**

A typical flash converter (Figure 4.17) generally exhibits a signal-dependent input impedance (often referred to as *non-linear* input impedance), where the effective input capacitance is a function of signal level. The signal-dependent capacitance can be modeled as the junction capacitance of a diode, \( C_j \). At the negative end of the input range, all the parallel comparators in the flash converter are "off", and the capacitance is low (modeled by a reverse-biased diode). At the positive end of the input range, all comparators are "on", thereby increasing the effective input capacitance (modeled by a zero-biased diode). For the example in the diagram, the Spice model (Figure 4.18) for the flash converter input under consideration is a
7.5nH inductor (simulating package pin and wirebond inductance), a 10pF fixed capacitor, and a diode having a 6pF zero-bias junction capacitance ($C_{JO}$). The total input capacitance changes from 16pF (0V input) to 12.5pF (–2V input) as shown in Figure 4.18. The 50ohm series resistor, $R_s$, is required to isolate the wideband op amp output from the flash converter input capacitance. Selecting the correct value for the series resistance is critical. If it is too low, the wideband, low-distortion op amp may be unstable because of the flash converter capacitive load. If it is too large, the distortion due to the non-linear input impedance may become significant, and bandwidth will be reduced because of the lowpass filter formed by the series resistor and the input capacitance. Data sheets for wideband low distortion amplifiers generally have curves showing the optimum value of series resistance as a function of the load capacitance. Typical recommended resistor values range from about 10ohms to 100ohms, depending on the amplifier and the load capacitance. In the model, a value of 50ohm was chosen. Figure 4.19 shows the simulated THD produced by the equivalent circuit (assuming an ideal op amp, of course).

![Typical Flash ADC Block Diagram](image)

Figure 4.17
FLASH ADC INPUT MODEL SHOWS
CAPACITANCE IS A FUNCTION OF INPUT SIGNAL

![Flash ADC Input Model Diagram](image)

Figure 4.18

ADC TOTAL HARMONIC DISTORTION VERSUS
INPUT FREQUENCY AS PREDICTED BY MODEL

![THD vs Frequency Graph](image)

Figure 4.19
**DRIVING THE AD9050 SINGLE-SUPPLY 10-BIT, 40MSPS ADC**

The AD9050 is a 10-bit, 40MSPS single supply ADC designed for wide dynamic range applications such as ultrasound, instrumentation, digital communications, and professional video. A block diagram of the AD9050 (Figure 4.20) illustrates the two-step subranging architecture, and key specifications are summarized in Figure 4.21.

![AD9050 10-BIT, 40MSPS SINGLE SUPPLY ADC](image)

**Figure 4.20**
AD9050 10-BIT, 40MSPS ADC KEY SPECIFICATIONS

- 10-Bits, 40MSPS, Single +5V Supply
- Selectable Digital Supply: +5V, or +3V
- Low Power: 300mW on BiCMOS Process
- On-Chip SHA and +2.5V reference
- 56dB S/(N+D), 9 Effective Bits, with 10.3MHz Input Signal
- No input transients, Input Impedance 5kΩ, 5pF
- Input Range +3.3V ±0.5V Single-Ended or Differential
- 28-pin SOIC / SSOP Packages
- Ideal for Digital Beamforming Ultrasound Systems

Figure 4.21

The analog input circuit of the AD9050 (see Figure 4.22) is differential, but can be driven either single-endedly or differentially with equal performance. The input signal range of the AD9050 is ±0.5V centered around a common-mode voltage of +3.3V.

AD9050 SIMPLIFIED INPUT CIRCUIT

The input circuit of the AD9050 is a relatively benign and constant 5kΩ in parallel with approximately 5pF. Because of its well-behaved input, the AD9050 can be driven directly from 50, 75, or 100ohm sources without the need for a low-distortion buffer amplifier. In ultrasound applications, it is normal to ac couple the signal (generally between 1MHz and 15MHz) into the AD9050 differential inputs using a wideband transformer as shown in Figure 4.23 (A). Signal-to-noise plus distortion (S/N+D) values of 57dB (9.2 ENOB) are typical for a 10MHz input signal. If the
input signal comes directly from a 50, 75, or 100ohm single-ended source, capacitive coupling as shown in Figure 4.23 (B) can be used.

**AC COUPLING INTO THE INPUT OF THE AD9050 ADC**

![AC Coupling Diagram](image)

**Figure 4.23**

**DRIVING ADCs WITH SWITCHED CAPACITOR INPUTS**

Many ADCs, including fast sampling ones, have switched capacitor input circuits. Not only can the effective input impedance be a function of the sampling rate, but the switches (usually CMOS) may inject charge on the ADC's analog input. For instance, the internal track-and-hold amplifier (THA) may generate a current spike on the analog input when it switches from the *track* mode to the *hold* mode, and vice versa. Other spikes may be generated during the actual conversion. These fast current spikes appear on the output of the external ADC drive amplifier, producing corresponding voltage spikes (because of the closed-loop high frequency op amp output impedance), and conversion errors will result if the amplifier settling time to them is not adequate.

The AD876 is a 10-bit, 20MSPS, low power (150mW), CMOS ADC with a switched capacitor track-and-hold input circuit. The overall block diagram of the ADC is shown in Figure 4.24, and key specifications are given in Figure 4.25.
AD876 10-BIT, 20MSPS LOW POWER SINGLE SUPPLY ADC SIMPLIFIED BLOCK DIAGRAM

Figure 4.24

AD876 LOW POWER SINGLE SUPPLY ADC

KEY SPECIFICATIONS

- 10-Bits, 20MSPS, Single-Supply
- Low Power CMOS Design: 140mW
- Standby Mode Power: <50mW
- $S/(N+D)$: 56dB @ 1MHz
  55dB @ 3.58MHz
  51dB @ 10MHz
- Input Bandwidth: 250MHz
- Input Range: 2V peak-to-peak
- Differential Gain: 1%, Differential Phase: 0.5°

Figure 4.25

Operation of the AD876 switched capacitor input circuit is illustrated in Figure 4.26, and the associated switching waveforms in Figure 4.27. The CMOS switches S1, S2, and S3 control the action of the internal sample and hold. They are shown in the track mode. Notice that in the track mode, the CMOS switch, S2, connects the input, $V_{IN}$, to the 3pF hold capacitor which must be charged by the drive amplifier.

When the circuit goes into the hold mode the following sequential switching occurs: S1 opens, S2 opens, and S3 closes (the entire sequence occurs in a few nanoseconds). The held voltage across $C_H$ is thus transferred to the output of the internal op amp, A1. Opening CMOS switch S2 injects a small amount of charge into the ADC input (equivalent to approximately 1mA of current, having a duration of a few nanoseconds). This current produces a transient voltage across the op amp closed loop output impedance (approximately 10ohms at 10MHz, and 100ohms at 100MHz)
in series with the 30ohm isolation resistor, $R_s$. The resulting voltage spike is approximately 100mV, corresponding to the product of the 1mA transient and the total ac source impedance of 100ohms (the op amp $Z_o$ of about 70ohms plus the 30ohm isolation resistor). During the hold mode, the AD876 performs the conversion, while the input signal may continue to change. The ADC input signal in Figure 4.27 goes from negative full scale (+1.7V) to positive full scale (+3.7V) during the first hold interval shown in the timing diagram. This represents a worst case condition, and input slew rates (and the corresponding charging transient) are quite likely to be less in a practical application.

At the end of the conversion, the switches return to their track mode state in the following sequence: S3 opens, S1 closes, and S2 closes (the entire sequence occurs in a few nanoseconds). When S2 closes, a small amount of charge is injected into the op amp output, but the dominant current spike (5mA) is the instantaneous current required to charge the hold capacitor, $C_H$, to the new signal value. The external drive amplifier must therefore charge $C_H$ to the new signal value and settle to the required accuracy (1/2 LSB, or 1mV) before the initiation of the next conversion (the settling time must be less than 25ns if the ADC is sampling at its maximum rate of 20MSPS as shown). The charging current dominates and is shown on the ADC input waveform as a negative-going 500mV spike. The addition of an external capacitor, $C_p = 15pF$, in parallel with the ADC input helps absorb some of the transient charge and is small enough so that bandwidth is not compromised. The optimum value of 15pF was determined empirically.
An empirical way to determine if the op amp transient load current settling time is adequate is to connect it to the ADC and observe the ADC input directly with a fast digital oscilloscope which is not sensitive to overdrive. If this is not possible, a good rule of thumb is to estimate the closed loop bandwidth, $f_{cl}$, required of the op amp to meet the required settling time. This is done as follows. The amplitude of the voltage spike, $V_{\text{error}}(t)$, at the ADC input is estimated by multiplying the input step current, $\Delta I$, by the total driving impedance, $Z_{\text{out}}$, (composed of the closed loop output impedance plus the series isolation resistor, $R_s$). The output impedance of a typical high speed op amp (bandwidth of 50MHz or greater) is generally between 50ohms and 100ohms at the frequencies contained in the transient. If we assume a single-pole system with a bandwidth of $f_{cl}$, the transient exhibits an exponential decay described by the following equation:

$$V_{\text{error}}(t) = \Delta I \cdot Z_{\text{out}} \cdot e^{-t/\tau}.$$ 

Solving the equation for $t$:

$$t = -\tau \ln\left(\frac{V_{\text{error}}(t)}{\Delta I \cdot Z_{\text{out}}}\right).$$

Substituting $\tau = \frac{1}{2\pi f_{cl}}$, and solving for $f_{cl}$:

$$f_{cl} = \frac{1}{2\pi} \ln\left(\frac{V_{\text{error}}(t)}{\Delta I \cdot Z_{\text{out}}}\right).$$
Now, let \( t = T_s/2 = 1/2f_s \) (where \( T_s = \) Sampling Period = \( 1/f_s \)), and \( V_{\text{error}}(t) = q/2, q = \) weight of LSB:

\[
f_{\text{cl}} = -\frac{f_s}{\pi} \ln \left( \frac{q/2}{\Delta I \cdot Z_{\text{out}}} \right),
\]

the minimum required op amp closed loop bandwidth.

This equation determines the minimum closed-loop op amp bandwidth required based on the sampling rate, LSB weight, and the input voltage step \((\Delta I) \cdot Z_{\text{out}}\).

In the example previously shown for the AD876 ADC, we can use the above equation to estimate the required op amp closed loop bandwidth by letting \( f_s = 20\text{MSPS}, q = 2\text{mV}, \) and \((\Delta I) \cdot Z_{\text{out}} = 500\text{mV}\). Solving yields \( f_{\text{cl}} = 39.6\text{MHz} \). The AD812 closed-loop bandwidth is approximately 60MHz in the configuration shown in Figure 4.28, which is more than sufficient to provide adequate settling time to the transient. Key specifications for the AD812 single-supply op amp are given in Figure 4.29.

**Simplified Model Predicts Input Transient Settling Time of ADC Drive Amp**
Figure 4.28

KEY SPECIFICATIONS OF AD812 DUAL OP AMP

- Dual, Current Feedback, Low Current (11mA)
- Specified for ±15, ±5, +5, and +3V
- Input and Output CM Voltage Range (+1V to +4V), $V_s = +5V$
- Optimized for Video Applications:
  - Gain Flatness: 0.1dB to 40MHz
  - Differential Gain: 0.2%, Differential Phase: 0.02°
- 145MHz Bandwidth (3dB)
- 1600V / μs Slew Rate
- 50mA Output Current

Figure 4.29

It is generally true that if you select the op amp first based on the required distortion performance at the maximum input frequency of interest, then its bandwidth will be much greater than the ADC sampling rate, and the op amp will have adequate transient load current settling time.

The drive amplifier selection process can be summarized as follows. First, choose an op amp which provides the necessary bandwidth, distortion, and output voltage compatible with the ADC. A good ADC data sheet will recommend one or two op amps, generally selected to optimize ac performance at the higher frequencies. However, other choices may be better because of system considerations. For example, many tradeoffs are possible between ac and dc performance. If extremely low distortion at low frequencies is required (at the expense of high frequency performance), other low distortion amplifiers may provide optimum system performance. Other factors such as single-supply versus dual-supply may influence the decision.

The next step is to examine the ADC data sheet carefully to determine if the input structure presents any transient loads to the op amp. If transient loads are present, the op amp settling time is important, and the ADC data sheet should be consulted for specific requirements. If the data sheet does not specify the op amp settling time, a conservative approach is to choose an op amp with a settling time (to the required accuracy) of less than one-half the minimum sampling period. The required closed-loop bandwidth, $f_{cl}$, corresponding to the settling time can be estimated using the procedure and equations previously described. Finally, it is most important to construct a prototype of the system and perform an actual evaluation of the combined op amp and ADC performance. Manufacturer’s evaluation boards are useful for this purpose.
DRIVE OP AMP SELECTION CRITERIA BASED ON ADC DYNAMIC PERFORMANCE: SUMMARY

- Select Op Amp with distortion and noise better than ADC
- Consider other factors also:
  - Output Voltage Swing must match ADC input
  - Single or Dual-Supply System?
  - DC Accuracy / Drift if DC coupled
- Examine ADC for transient load currents, if any
  - Op amp must have sufficient closed-loop bandwidth to settle to transient currents
  - Use exponential decay model to estimate required $f_{cl}$

Figure 4.30

GAIN SETTING AND LEVEL SHIFTING

In dc coupled applications, the drive amplifier must provide the required gain and offset to match the signal to the input voltage range of the ADC. Figure 4.31 summarizes various gain and level shifting options. The circuit of Figure 4.31A operates in the non-inverting mode and uses a reference voltage, $V_{ref}$, to offset the output. Gain and offset interact according to the equation:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)V_{in} - \frac{R_2}{R_1}V_{ref}$$

The circuit in Figure 4.31B operates in the inverting mode, and the signal gain is independent of the offset. The disadvantage of this circuit is that the addition of $R_3$ increases the noise gain, and hence the sensitivity to the op amp input offset voltage and noise. The input/output equation is given by:

$$V_{out} = -\frac{R_2}{R_1}V_{in} - \frac{R_2}{R_3}V_{ref}$$

The circuit in Figure 4.31C operates in the inverting mode, and the offset is applied to the non-inverting input, with no noise gain penalty. This circuit is also attractive for single-supply applications where $V_{ref} > 0$. The input/output equation is given by:

$$V_{out} = -\frac{R_2}{R_1}V_{in} + \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right)V_{ref}$$
A practical example of a single-supply video signal-processing digitizing circuit is shown in Figure 4.32. The AD876 (10-bit, 20MSPS) ADC operates on a single +5V supply, and its nominal input voltage range is 2V peak-to-peak centered around an allowable common-mode voltage between +2.7V and +3.1V. The input voltage range of the AD876 is set by external references. The AD812 drive amplifier is a fast video op amp with a common-mode input voltage range of +1V to +4V, and a +1V to +4V output voltage range. With this amplifier/ADC combination, optimum performance is obtained by setting the AD876 input common-mode voltage at +2.7V (corresponding to an upper and lower input range of +3.7 and +1.7V, respectively).
The Thevenin equivalent circuit of the video signal is a ground-referenced, 0 to +2V source with a 75ohm source impedance designed to drive a 75ohm terminated coaxial cable, producing a standard 0 to +1V video signal level at the load termination, $R_T$. (The video source can also be modeled as a Norton equivalent circuit with a 0 to +2.67mA current source in parallel with the 75ohm source resistance.)

The AD812 op amp is operated as an inverting level shifter, similar to the circuit previously shown in Figure 4.31C. The feedback resistor, $R_2$, is chosen to be 681ohms for optimum flatness over the video bandwidth per the AD812 data sheet. The feedforward resistor, $R_1$, is selected to give a signal gain of –2. The termination resistor, $R_T$, is chosen so that the parallel combination of $R_T$ and $R_1$ is 75ohms. The common-mode voltage, $V_{cm}$, required on the non-inverting op amp input must now be determined. Assume that the video source is zero volts. The corresponding op amp output voltage should be +3.7V. The common-mode voltage is determined by the voltage divider formed by $R_2$, $R_1$, $R_T$, and the 75ohm source resistance:

$$V_{cm} = 3.7 \left( \frac{R_s R_T + R_1}{R_s R_T + R_1 + R_2} \right) = 3.7 \left( \frac{42 + 340}{42 + 340 + 681} \right) = 133 \text{V}.$$  

The +1.33V common-mode voltage is derived from the AD680 +2.5V reference using a resistor divider and is decoupled with a 10µF/25V tantalum capacitor in parallel with a 0.1µF low-inductance ceramic one.

The AD9050 10-bit, 40MSPS single-supply ADC input range of ±0.5V is centered around a common-mode voltage of +3.3V (corresponding to an upper and lower limit of +3.8V and +2.8V, respectively). An appropriate single-supply dc-coupled drive circuit based upon the AD8011 low power, low distortion op amp is shown in Figure 4.33. The source is a ground-referenced 0 to +2V signal which is series-terminated in 75ohms. The termination resistor, $R_T$, is chosen such that the parallel combination of $R_T$ and $R_1$ is 75ohms. The AD8011 current-feedback op amp is configured for a gain of –1. The feedback resistor, $R_2$, is the value recommended for optimum bandwidth. Assume that the video source is at zero volts. The corresponding ADC input voltage should be +3.8V. The common-mode voltage, $V_{cm}$, is determined from the following equation:

$$V_{cm} = 3.8 \left( \frac{R_s R_T + R_1}{R_s R_T + R_1 + R_2} \right) = 3.8 \left( \frac{388 + 1000}{38.8 + 1000 + 1000} \right) = 1.94 \text{V}.$$  

The common-mode voltage, $V_{cm}$, is derived from the common-mode voltage at the inverting input of the AD9050. The +3.3V is buffered by the AD820 single-supply FET-input op amp. A divider network generates the required +1.94V for the AD8011, and a potentiometer provides offset adjustment capability.

The AD8011 current feedback op amp was chosen because of its low power (5mW), wide bandwidth (200MHz), and low distortion (~70dBc at 5MHz). It is fully specified for both ±5V and ±5V operation. When operating on a single +5V supply, the input common-mode range is +1.5V to +3.5V, and the output swing is +1.2V to +3.5V. The high speed level-shifting PNP transistor at the output of the AD8011 allows the op
amp to operate within its recommended output range and ensures best distortion performance. Distortion performance of the entire circuit including the ADC is better than –60dBc for an input frequency of 10MHz and a sampling rate of 40MSPS.

DC-COUPLED SINGLE-SUPPLY DRIVE CIRCUIT FOR AD9050 10-BIT, 40MSPS ADC USING AD8011 OP AMP

![Circuit Diagram]

Figure 4.33

AD8011 OP AMP KEY SPECIFICATIONS

- Low Power: 1mA Current (5mW on +5V Supply)
- Bandwidth: 320MHz (G=+1), 180MHz (G=+2)
- Settling Time: 25ns to 0.1%
- Low Distortion: -76dBc at 5MHz
- Input Common Mode Voltage (+5V Supply): +1.5V to +3.5V
- Output Voltage Swing (+5V Supply): +1.2V to +3.8V
- Fully Specified for Single or Dual-Supply Operation

Figure 4.34
HIGH SPEED SAMPLING ADC EXTERNAL REFERENCE VOLTAGE GENERATION

Due to process and design-related constraints, it is not always possible to integrate the reference and the ADC on the same chip. In some ADCs which do have an internal reference, performance improvements (less noise and drift) may be obtained by using an external reference rather than the internal one. We saw in the case of the AD77XX series that this was the case.

There are a number of low-cost, low-noise, low-voltage references suitable for use with high performance sampling ADCs. Reference voltages of +1.25V, +2.048V, +2.5V, +3.0V, +3.3V, +4.096V, and +4.5V are ideal for single-supply (+3V or +5V) ADCs. (See Figure 4.35).

LOW VOLTAGE REFERENCE SUMMARY

<table>
<thead>
<tr>
<th>REFERENCE PART #</th>
<th>OUTPUT (V)</th>
<th>TOLERANCE (mV)</th>
<th>DRIFT ppm/°C (max)</th>
<th>NOISE (µV p-p, typ) 0.1 to 10Hz</th>
<th>SUPPLY CURRENT (mA) typ</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD780</td>
<td>+2.5 / +3.0</td>
<td>1 - 5</td>
<td>3 - 20</td>
<td>4</td>
<td>0.050 - 5</td>
</tr>
<tr>
<td>AD680</td>
<td>+2.5</td>
<td>5 - 10</td>
<td>20 - 30</td>
<td>8</td>
<td>0.100 - 5</td>
</tr>
<tr>
<td>REF43</td>
<td>+2.5</td>
<td>15 - 50</td>
<td>10 - 25</td>
<td>5</td>
<td>0.050 - 5</td>
</tr>
<tr>
<td>REF191</td>
<td>+2.048</td>
<td>2 - 10</td>
<td>5 - 25</td>
<td>20</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>REF192</td>
<td>+2.5</td>
<td>2 - 10</td>
<td>5 - 25</td>
<td>25</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>REF193</td>
<td>+3.0V</td>
<td>10 - 10</td>
<td>10 - 25</td>
<td>30</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>REF195</td>
<td>+3.3V</td>
<td>10 - 10</td>
<td>10 - 25</td>
<td>33</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>REF196</td>
<td>+4.096V</td>
<td>2 - 10</td>
<td>5 - 25</td>
<td>40</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>REF197</td>
<td>+4.5V</td>
<td>2 - 10</td>
<td>5 - 25</td>
<td>45</td>
<td>0.045 - 5</td>
</tr>
<tr>
<td>AD589</td>
<td>+1.235</td>
<td>35</td>
<td>25 - 100</td>
<td>4</td>
<td>0.050 - 5</td>
</tr>
</tbody>
</table>

* Two Terminal

Figure 4.35

The AD876 requires two references: one for each end of its input range which is nominally set for +1.7V and +3.7V. The output impedance of the drive sources must be low at high frequencies to absorb the transient currents generated at the ADC reference input terminals by the internal switched capacitor circuits.

The circuit shown in Figure 4.36 makes use of the REF198 (+4.096V) reference (see previous discussion regarding the analog input drive circuit for the AD876) and a dual FET-input single-supply op amp (AD822) to generate the two voltages. The AD876 reference inputs each have a FORCE (F) and SENSE (S) pin. The Kelvin connection compensates for the voltage drop in the internal parasitic resistances (approximately 5ohms). The internal ADC reference ladder impedance is approximately 300ohms, requiring the AD822s to source and sink approximately 6.7mA. There is an additional resistance of approximately 300ohms in series with each SENSE line. The two reference FORCE pins are decoupled at low and high frequencies using both a tantalum and a ceramic capacitor. The additional 20µF across the two SENSE pins adds additional decoupling for differential transients.
Note that the AD822 must be properly compensated to drive the large capacitive load. Key specifications for the AD822 are summarized in Figure 4.37.

**REFERENCE VOLTAGE GENERATOR FOR AD876 10-BIT, 20MSPS SINGLE-SUPPLY ADC**

![Reference Voltage Generator Circuit Diagram](image)

**Figure 4.36**

**AD822 OP AMP KEY SPECIFICATIONS**

- True Single-Supply FET-Input Dual Op Amp
- Complete Specifications for ±15V, ±5V, +5V, +3V
- Input Voltage Range Extends 200mV Below Ground and to within 1V of +V_s
- Output Goes to Within 5mV of Supplies (Open-Collector Complementary Output Stage Limited by V_{cesat})
- 1.8MHz Unity-Gain Bandwidth
- 800µV Offset Voltage, 2µV/°C Offset Drift
- Low Noise: 13nV/√Hz
- Low Power: 800µA / Amplifier
- Single Version Available (AD820)

**Figure 4.37**
ADC Input Protection and Clamping

The input to high speed ADCs should be protected from overdrive to prevent catastrophic damage or performance degradation. A good rule of thumb is never let the analog input exceed the supply voltage by more than 0.3V (this not only applies when the supply is on, but also when it is off, i.e., if the supply is off, the analog input should not exceed ±0.3V). In a dual supply system, this rule applies to both supplies. The rule of thumb protects most devices, but the data sheet Absolute Maximum specifications should always be consulted to determine possible exceptions. In some ADCs, the analog input is protected internally by diodes connected to the supplies. In these cases, an external resistor is required to limit the input current to 5mA or less under the overvoltage condition. Several overdrive protection schemes which use external diodes are shown in Figure 4.38.

In Figure 4.38A, the op amp is powered from ±15V, and the ADC from ±5V. The addition of the Schottky diodes on the input will prevent the analog input from exceeding the ADC supplies. Some ADCs have internal diodes, but the addition of the external ones ensures protection for higher currents. An alternative solution is to generate the ±5V for the ADC from the op amp ±15V supplies using three terminal regulators (such as the 78L05 and 79L05). This eliminates possible sequencing and overdrive problems, and power dissipation in the regulator is not excessive if low power CMOS ADCs are used (see Figure 4.38B).

With the proliferation of high speed op amps and ADCs, both of which operate on dual 5V supplies, the situation shown in Figure 4.38C is quite common, and there is no sequencing problem provided both the amplifier and the ADC are operated from the same supplies.

Figure 4.38D shows the case where a flash converter (powered from a single −5V supply) is driven from an amplifier powered from ±5 V. The series resistor and the Schottky diode provide protection from forward-biasing the flash substrate diode more than a few tenths of a volt, thereby preventing possible damage.
Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high (V_H) and low (V_L) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to traditional output-clamping devices. Recovery time from overdrive is less than 5ns.

The key to the AD8036 and AD8037’s fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. This new design reduces clamp errors by more than 10x over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.

Figure 4.39 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200V/µs, 240MHz high voltage gain, differential to single-ended amplifier) and A2 (a G=+1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.
The input clamp section is comprised of comparators $C_H$ and $C_L$, which drive switch $S_1$ through a decoder. The unity-gain buffers in series with the $+V_{IN}$, $V_H$, and $V_L$ inputs isolate the input pins from the comparators and $S_1$ without reducing bandwidth or precision.

The two comparators have about the same bandwidth as $A_1$ (240MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the input clamp circuit, consider the case where $V_H$ is referenced to $+1V$, $V_L$ is open, and the AD8036 is set for a gain of $+1$ by connecting its output back to its inverting input through the recommended 140ohm feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects $A_1$'s noninverting input.

If a 0V to $+2V$ voltage ramp is applied to the AD8036's $+V_{IN}$ for the connection just described, $V_{OUT}$ should track $+V_{IN}$ perfectly up to $+1V$, then should limit at exactly $+1V$ as $+V_{IN}$ continues to $+2V$.

In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1V, the output of the high limit comparator $C_H$ starts in the off state, as does the output of $C_L$. When $V_{IN}$ just exceed $V_H$ (practically, by about 18mV), $C_H$ changes state, switching $S_1$ from "A" to "B" reference level. Since the + input of $A_1$ is now connected to $V_H$, further increases in $+V_{IN}$ have no effect on the AD8036's output voltage. The AD8036 is now operating as a unity-gain buffer for the $V_H$ input, as any variation in $V_H$, for $V_H > 1V$, will be faithfully produced at $V_{OUT}$.

Operation of the AD8036 for negative input voltages and negative clamp levels on $V_L$ is similar, with comparator $C_L$ controlling $S_1$. Since the comparators see the
voltage on the $+V\text{IN}$ pin as their common reference level, the voltage $V_H$ and $V_L$ are defined as "High" or "Low" with respect to $+V\text{IN}$. For example, if $V\text{IN}$ is set to zero volts, $V_H$ is open, and $V_L$ is $+1\text{V}$, comparator $C_L$ will switch $S_1$ to "C", so the AD8036 will buffer the voltage on $V_L$ and ignore $+V\text{IN}$.

The performance of the AD8036/AD8037 closely matches the ideal just described. The comparator's threshold extends from $60\text{mV}$ inside the clamp window defined by the voltages on $V_L$ and $V_H$ to $60\text{mV}$ beyond the window's edge. Switch $S_1$ is implemented with current steering, so that $A_1$'s $+$ input makes a continuous transition from say, $V\text{IN}$ to $V_H$ as the input voltage traverses the comparator's input threshold from $0.9\text{V}$ to $1.0\text{V}$ for $V_H = 1.0\text{V}$.

The practical effect of the non-ideal operation is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 4.40 is a graph of $V_{\text{OUT}}$ versus $V\text{IN}$ for the AD8036 and a typical output clamp amplifier. Both amplifiers are set for $G=+1$ and $V_H = +1\text{V}$.

**Figure 4.40**

The worst case error between $V_{\text{OUT}}$ (ideally clamped) and $V_{\text{OUT}}$ (actual) is typically $18\text{mV}$ times the amplifier closed-loop gain. This occurs when $V\text{IN}$ equals $V_H$ (or $V_L$). As $V\text{IN}$ goes above and/or below this limit, $V_{\text{OUT}}$ will stay within $5\text{mV}$ of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of $0.8\text{V}$, and can have an output voltage as far as $200\text{mV}$ over the clamp limit. In addition, since the output clamp causes the amplifier
to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.

It is important that a clamped amplifier such as the AD8036/AD8037 maintain low levels of distortion when the input signals are close the clamping voltages. Figure 4.41 shows the second and third harmonic distortion for the amplifiers as the output approaches the clamp voltages. The input signal is 20MHz, the output signal is 2V peak-to-peak, and the output load is 100ohms.

Recovery from step voltage which is two times over the clamping voltage is shown in Figure 4.42. The input step voltage starts at +2V and goes to 0V (left-hand traces on scope photo). The input clamp voltage (V_H) is set at +1V. The right-hand trace shows the output waveform. The key specifications for the AD8036/AD8037 clamped amplifiers are summarized in Figure 4.43.

**AD8036/AD8037 DISTORTION NEAR CLAMPING REGION, OUTPUT = 2V p-p, LOAD = 100Ω, f = 20MHz**

![Graph showing harmonic distortion](image-url)

Figure 4.41
AD8036 / AD8037 OVERDRIVE (2x) RECOVERY

Figure 4.42

AD8036 / AD8037 SUMMARY SPECIFICATIONS

- Proprietary Input Clamping Circuit with Minimized Nonlinear Clamping Region
- Small Signal Bandwidth: 240MHz (AD8036), 270MHz (AD8037)
- Slew Rate: 1500V/\mu s
- 1.5ns Overdrive Recovery
- Low Distortion: -72dBc @ 20MHz (500\Omega load)
- Low Noise: 4.5nv/√Hz, 2pA/√Hz
- 20mA Supply Current on ±5V

Figure 4.43

Figure 4.44 shows the AD9002 8-bit, 125MSPS flash converter driven by the AD8037 (240MHz bandwidth) clamping amplifier. In the circuit, the bandwidth of the AD8037 is 240MHz. The clamp voltages on the AD8037 are set to +0.55 and –0.55V, referenced to the ±0.5V input signal, with the external resistive dividers. The AD8037 also supplies a gain of two, and an offset of –1V (using the AD780 voltage reference), to match the 0 to –2V input range of the AD9002 flash converter. The output signal is clamped at +0.1V and –2.1V. This multi-function clamping circuit therefore performs several important functions as well as preventing damage to the
flash converter which occurs if its input exceeds +0.5V, thereby forward biasing the substrate diode. The 1N5712 Schottky diode adds further protection during power-up.

**AD9002 8-BIT, 125MSPS FLASH CONVERTER DRIVEN BY AD8037 CLAMP AMPLIFIER**

![AD9002 8-BIT, 125MSPS FLASH CONVERTER DRIVEN BY AD8037 CLAMP AMPLIFIER](image)

**Figure 4.44**

The feedback resistor, $R_2 = 301$Ω, is selected for optimum bandwidth per the manufacturer's data sheet recommendation. In order to give a gain of two, the parallel combination of $R_1$ and $R_3$ must also equal $R_2$:

$$\frac{R_1 \cdot R_3}{R_1 + R_3} = R_2 = 301\Omega$$

(nearest 1% standard resistor value).

In addition, the Thevenin equivalent output voltage of the AD780 +2.5V reference and the $R_3 / R_1$ divider must be +1V to provide the –1V offset at the output of the AD8037.

$$\frac{25 \cdot R_1}{R_1 + R_3} = 1\text{volt}$$

Solving the two simultaneous equations yields $R_1 = 499$Ω, $R_3 = 750$Ω (using the nearest 1% standard resistor values).

Other input and output voltages ranges can be accommodated by appropriate changes in the external resistors.
OTHER APPLICATIONS FOR CLAMPING AMPLIFIERS

The AD8036/AD8037’s clamp output can be set accurately and has a well controlled flat level. This, along with wide bandwidth and high slew rate make them well suited for a number of other applications. Figure 4.45 is a diagram of a programmable level pulse generator. The circuit accepts a TTL timing signal for its input and generates pulses at the output up to 24V p-p with 2500V/µs slew rate. The output levels can be programmed to anywhere in the range between –12V to +12V.

PROGRAMMABLE PULSE GENERATOR USING AD8037 CLAMP AMP AND AD811 OP AMP

![Programmable Pulse Generator Diagram]

The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12V range. The AD811 was chosen for its ability to operate with ±15V supplies and its high slew rate.

R1 and R2 act as a level shifter to make the TTL signal levels approximately symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels result from the clamping action of the AD8037 and are not controlled by either the high or low logic levels passing through a linear amplifier. For good rise and fall times at the output pulse, a logic family with high speed edges should be used.

The high logic levels are clamped at 2 times the voltage at 

\[ V_H \]

while the low logic levels are clamped at two times the voltage at 

\[ V_L \].

The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at 

\[ V_H \], and the low output level to be 10 times the voltage at 

\[ V_L \].

The clamping inputs are additional inputs to the input stage of the AD8036/AD8037. As such, they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 4.46 is a schematic for a full wave rectifier, sometimes called an absolute value generator. It works well up to 20MHz and can operate at significantly higher...
frequencies with some degradation in performance. The distortion performance is significantly better than diode-based full-wave rectifiers, especially at high frequencies.

**FULL-WAVE RECTIFIER USING AD8037 CLAMP AMP**

![Diagram of the AD8037 clamp amp circuit](figure)

The AD8037 is configured as an inverting amplifier with a gain of unity. The input drives the inverting amplifier and also directly drives $V_L$, the lower level clamping input. The high level clamping input, $V_H$, is left floating and plays no role in the circuit.

When the input is negative, the amplifier acts as a unity-gain inverter and outputs a positive signal at the same amplitude as the input, with opposite polarity. $V_L$ is driven negative by the input, so it performs no clamping action, because the positive output signal is always higher than the negative level driving $V_L$.

When the input is positive, the output result is the sum of two separate effects. First, the inverting amplifier multiplies the input by $-1$ because of the unity-gain inverting configuration. This effectively produces an offset as explained above, but with a dynamic level that is equal to $-1$ times the input. Second, although the positive input is grounded (through 100ohms), the output is clamped at two times the voltage applied to $V_L$ (a positive, dynamic voltage in this case). The factor of two is because the noise gain of the amplifier is two.

The sum of these two actions results in an output that is equal to unity times the input signal for positive input signals as shown in Figure 4.47. An input/output scope photo with an input signal of 20MHz and an amplitude of $\pm 1V$ is shown in Figure 4.48. Thus, for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to $V_H$ rather than $V_L$. 
The circuit can get to within about 40mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range, and is a result of the switching between the conventional op amp input and the clamp input. But because
there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds diode-based full wave rectifiers.

The 40mV offset can be removed by adding an offset to the circuit. A 27.4kohm input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4V dc level (depending on the polarity of the rectifier) into this resistor will compensate for the offset.

Full wave rectifiers are useful in many applications including AM signal detection, high frequency ac voltmeters, and various arithmetic operations.

The AD8037 can also be configured as an amplitude modulator as shown in Figure 4.49. The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels. This is the higher frequency carrier signal. The modulation signal is applied to both the input of a unity gain inverting amplifier and to $V_L$, the lower clamping input. $V_H$ is biased at +0.5V.

![AD8037 AMPLITUDE MODULATOR](image)

Figure 4.49
Figure 4.50

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both $V_L$ and $V_H$ are dc biased at $-0.5V$ and the carrier and modulation inputs driven as above, the output would be a 2V p-p square wave at the carrier frequency riding on a waveform at the modulating frequency. The inverting input (modulation signal) is creating a varying offset to the 2V p-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When $V_L$ is driven by the modulation signal instead of being held at a dc level, a more complicated situation results. The resulting waveform is composed of an upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelopes are $180^\circ$ out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simpler circuit above. The polarity of this offset is in the same direction as the upper envelope. Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to $V_L$. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an AM waveform. The depth of modulation can be modified by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms. The modulation depth can also be changed by changing the dc bias applied to $V_H$. In this case, the amplitudes
of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

**NOISE CONSIDERATIONS IN HIGH SPEED SAMPLING ADC APPLICATIONS**

High speed, wide bandwidth sampling ADCs are optimized for dynamic performance over a wide range of analog input frequencies. Because of the wide bandwidth front ends coupled with internal device and resistor noise, DC inputs generally produce a range of output codes as shown in Figure 4.51. The correct code appears most of the time, but adjacent codes appear with reduced probability. If a normal probability density curve is fitted to this distribution, the standard deviation will be equal to the equivalent rms input noise of the ADC.

For instance, the equivalent input noise of the AD9022 12-bit, 20MSPS ADC is approximately 0.57LSB rms. This implies that the best full scale sinewave signal-to-noise ratio that can be obtained is approximately 68dB. (Full scale sinewave peak-to-peak amplitude = 4096LSBs, or 1448LSBs rms, from which the SNR is calculated as $20 \log_{10}[1448/0.57] = 68\text{dB}$). In fact, the SNR of the ADC is limited by other factors, such as quantization noise and distortion.

When driving sampling ADCs with wideband op amps, the output noise of the drive amplifier can contribute to the overall ADC noise floor. A few quick calculations
should be made to estimate the total output noise of the op amp and see if it is significant with respect to the ADC noise.

The complete noise model for an op amp is shown in Figure 4.52. This model is accurate, provided there is less than 1 or 2dB peaking in the closed-loop output frequency response. Excessive peaking in the frequency response increases the effects of the wide band noise, and the simple approximation will give optimistic results.

**GENERALIZED OP AMP NOISE MODEL**

![Figure 4.52](image)

It is rarely necessary to consider all noise sources, since sources which have noise contributions 50% smaller than the largest can be neglected. In high speed systems, where the resistors of the source and the op amp feedback network rarely exceed 1kohm, the resistor Johnson noise can usually be neglected.

In the case of voltage feedback op amps, the input current noise can usually be neglected. For current feedback op amps operating at noise gains of approximately 4 or less, the inverting input current noise generally dominates. At higher noise gains, however, the effects of voltage noise become significant and should be included.
SIMPLIFICATIONS IN NOISE CALCULATIONS

- **Voltage Feedback Op Amps:**
  - Neglect Resistor Noise if Resistors < 1kΩ
  - Neglect Input Current Noise

- **Current Feedback Op Amps:**
  - Neglect Resistor Noise if Resistors < 1kΩ
  - Neglect Non-Inverting Input Current Noise
  - Evaluate Effects of Both Input Voltage Noise (Dominates at High Noise Gains)
  - Evaluate Effects of Inverting Input Current Noise (Dominates at Low Noise Gains)

**Figure 4.53**

As an example to show the effects of noise, consider the circuit shown in Figure 4.54, where the AD9022 12-bit, 20MSPS ADC is driven by the AD9632 low-distortion op amp. Because the AD9632 is a voltage feedback op amp and the external resistor values are less than 1kohm, only the voltage noise (4.3nV/rtHz) is significant to the calculation. Because the AD9632 is operated with a noise gain of 2, the output voltage noise is 8.6nv/rtHz (excluding any source noise).

**NOISE CALCULATIONS FOR AD9632 OP AMP DRIVING AD9022 12-BIT, 20MSPS ADC**

![AD9632 and AD9022 Diagram]

**Figure 4.54**

The bandwidth for integration is either the op amp closed-loop bandwidth (250MHz), or the ADC input bandwidth (110MHz), whichever is less. This is an important point, because in most cases (especially when dealing with low-distortion, wide
bandwidth amplifiers), the input of the ADC acts as the low pass filter to the op amp noise.

The calculation for the op amp noise contribution at the ADC input is simple:

\[ V_{ni} = \frac{86 \text{nV}}{\sqrt{Hz}} \times \sqrt{110 \times 10^6 \times 157 \text{Hz}} = 113 \mu \text{V rms} \]

The factor of 1.57 is required to convert the single-pole 110MHz ADC input bandwidth into an equivalent noise bandwidth. The op amp contribution of 113µV rms is less than one-half the effective input noise of the AD9022 (0.57LSB = 285µV rms), and can therefore be neglected.

In most high speed system applications, a passive antialiasing filter (either lowpass for baseband sampling, or bandpass for harmonic or undersampling) is required. Placing this filter between the op amp and the ADC will further reduce the effects of the drive amplifier noise.

**PROPER POSITIONING OF THE ANITALIASING FILTER WILL REDUCE THE EFFECTS OF THE OP AMP NOISE**

![Diagram showing the positioning of the antialiasing filter](image)

**Figure 4.55**

The op amp noise rarely limits the performance of high speed systems. The largest source of unwanted noise generally comes from improper attention to good high speed layout, grounding, and decoupling techniques.
ADC NOISE SOURCES

- ADC Distortion and Quantization Noise
- ADC Equivalent Input Noise
- Internal SHA Aperture Jitter
- External Drive Amplifier
- Poor Grounding and Decoupling Techniques
- Poor Layout and Signal Routing Techniques
- Noisy Sampling Clock
- External Switching Power Supply

Figure 4.56

Proper power supply decoupling techniques must be used on each PC board in the system. Figure 4.57 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL and low ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and 5µF). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!
PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO ACHIEVING GOOD HIGH SPEED SYSTEM PERFORMANCE

Figure 4.57

If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multicard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 4.58. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system star ground, or single-point ground, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent accidental dc voltages from developing between the two ground systems.
Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 4.59 will help to explain this seeming dilemma.
Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 4.59 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, $C_{STRAY}$. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It’s the IC designer’s job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the analog ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name “DGND” on an IC tells us that this pin connects to the digital ground of the IC. It does not say that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/output does not drive a large fanout. Minimizing the fanout on the converter’s digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin ($V_D$) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 4.60. The internal digital currents of the converter will return to ground through the $V_D$ pin decoupling capacitor (mounted as close to the converter
as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 4.60) to place a buffer latch adjacent to the converter to isolate the converter’s digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

**POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS**

![Diagram of power supply and grounding](image)

**Figure 4.60**

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V\textsubscript{D}), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A low phase-noise crystal oscillator should be used to generate the ADC sampling clock, because sampling clock jitter modulates the input signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.
It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

**SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS**

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC/DAC analog runs.
- Use lots of ground plane.
- Use microstrip techniques at high frequencies for controlled impedances and controlled return current paths.
- Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.

**Figure 4.61**

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 4.62 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

**A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING**

**Figure 4.62**
There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

**EDGE CONNECTIONS**

- Separate sensitive signal by ground pins.
- Keep down ground impedances with multiple (30-40% of total) ground pins.
- Have several pins for each power line.
- Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.

**Figure 4.63**

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 milliohms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

**USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS**

- DON’T! (If at all possible)
- Use “Pin sockets” or “Cage jacks” such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively)
- Always test the effect of sockets by comparing system performance with and without the use of sockets.
- Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.

**Figure 4.64**

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the
IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called “cage jacks”) to make up a multi-pin socket in the PCB itself (see Section 9).

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be, and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.
SWITCHING-MODE POWER SUPPLIES

- Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)
- Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits
- Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields
- Physically Isolate Supply from Analog Circuits
- Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise

Figure 4.65

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 4.66 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.
FILTERING A SWITCHING SUPPLY OUTPUT

- C₁ must have low inductance and be close to the supply to minimize HF current loops and resultant HF magnetic fields.

- C₂ is also low inductance, C₃ is electrolytic.

- If the switching supply is internally grounded, L₂ should be omitted.

Figure 4.66
REFERENCES

1. **Linear Design Seminar**, Analog Devices, 1995, Chapter 4, 5.
SECTION 5

UNDERSAMPLING APPLICATIONS

- Fundamentals of Undersampling
- Increasing ADC SFDR and ENOB using External SHAs
- Use of Dither Signals to Increase ADC Dynamic Range
- Effect of ADC Linearity and Resolution on SFDR and Noise in Digital Spectral Analysis Applications
- Future Trends in Undersampling ADCs
SECTION 5

UNDERSAMPLING APPLICATIONS

Walt Kester

An exciting new application for wideband, low distortion ADCs is called undersampling, harmonic sampling, bandpass sampling, or Super-Nyquist Sampling. To understand these applications, it is necessary to review the basics of the sampling process.

The concept of discrete time and amplitude sampling of an analog signal is shown in Figure 5.1. The continuous analog data must be sampled at discrete intervals, \( t_s \), which must be carefully chosen to insure an accurate representation of the original analog signal. It is clear that the more samples taken (faster sampling rates), the more accurate the digital representation, but if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. This leads us to the statement of Shannon’s Information Theorem and Nyquist’s Criteria given in Figure 5.2. Most textbooks state the Nyquist theorem along the following lines: A signal must be sampled at a rate greater than twice its maximum frequency in order to ensure unambiguous data. The general assumption is that the signal has frequency components from dc to some upper value, \( f_a \). The Nyquist Criteria thus requires sampling at a rate \( f_s > 2f_a \) in order to avoid overlapping aliased components. For signals which do not extend to dc, however, the minimum required sampling rate is a function of the bandwidth of the signal as well as its position in the frequency spectrum.

**SAMPLING AN ANALOG SIGNAL**

![Sampling an Analog Signal](image)

**Figure 5.1**
SHANNON’S INFORMATION THEOREM
AND NYQUIST’S CRITERIA

■ Shannon:

♦ An Analog Signal with a Bandwidth of \( f_a \) Must be Sampled at a Rate of \( f_s > 2f_a \) in Order to Avoid the Loss of Information.
♦ The signal bandwidth may extend from DC to \( f_a \) (Baseband Sampling) or from \( f_1 \) to \( f_2 \), where \( f_a = f_2 - f_1 \) (Undersampling, Bandpass Sampling, Harmonic Sampling, Super-Nyquist)

■ Nyquist:

♦ If \( f_s < 2f_a \), then a Phenomena Called Aliasing Will Occur.
♦ Aliasing is used to advantage in undersampling applications.

Figure 5.2

In order to understand the implications of aliasing in both the time and frequency domain, first consider the four cases of a time domain representation of a sampled sinewave signal shown in Figure 5.3. In Case 1, it is clear that an adequate number of samples have been taken to preserve the information about the sinewave. In Case 2 of the figure, only four samples per cycle are taken; still an adequate number to preserve the information. Case 3 represents the ambiguous limiting condition where \( f_s = 2f_a \). If the relationship between the sampling points and the sinewave were such that the sinewave was being sampled at precisely the zero crossings (rather than at the peaks, as shown in the illustration), then all information regarding the sinewave would be lost. Case 4 of Figure 5.3 represents the situation where \( f_s < 2f_a \), and the information obtained from the samples indicates a sinewave having a frequency which is lower than \( f_s / 2 \), i.e. the out-of-band signal is aliased into the Nyquist bandwidth between dc and \( f_s / 2 \). As the sampling rate is further decreased, and the analog input frequency \( f_a \) approaches the sampling frequency \( f_s \), the aliased signal approaches dc in the frequency spectrum.
The corresponding frequency domain representation of the above scenario is shown in Figure 5.4. Note that sampling the analog signal $f_a$ at a sampling rate $f_s$ actually produces two alias frequency components, one at $f_s + f_a$, and the other at $f_s - f_a$. The upper alias, $f_s + f_a$, seldom presents a problem, since it lies outside the Nyquist bandwidth. It is the lower alias component, $f_s - f_a$, which causes problems when the input signal exceeds the Nyquist bandwidth, $f_s/2$. 
From Figure 5.4, we make the extremely important observation that regardless of where the analog signal being sampled happens to lie in the frequency spectrum (as long as it does not lie on multiples of \( f_s/2 \)), the effects of sampling will cause either the actual signal or an aliased component to fall within the Nyquist bandwidth between \( dc \) and \( f_s/2 \). Therefore, any signals which fall outside the bandwidth of interest, whether they be spurious tones or random noise, must be adequately filtered before sampling. If unfiltered, the sampling process will alias them back within the Nyquist bandwidth where they can corrupt the wanted signals.

Methods exist which use aliasing to our advantage in signal processing applications. Figure 5.5 shows four cases where a signal having a 1MHz bandwidth is located in different portions of the frequency spectrum. The sampling frequency must be chosen such that there is no overlapping of the aliased components. In general, the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of \( f_s/2 \).
MINIMUM SAMPLING RATE REQUIRED FOR NON-OVERLAPPING ALIASING OF A 1MHz BANDWIDTH SIGNAL

Figure 5.5

In the first case, the signal occupies a band from dc to 1MHz, and therefore must be sampled at greater than 2MSPS. The second case shows a 1MHz signal which occupies the band from 0.5 to 1.5MHz. Notice that this signal must be sampled at a minimum of 3MSPS in order to avoid overlapping aliased components. In the third case, the signal occupies the band from 1 to 2MHz, and the minimum required sampling rate for no overlapping aliased components drops back to 2MSPS. The last case shows a signal which occupies the band from 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MSPS to avoid overlapping aliased components.

This analysis can be generalized as shown in Figure 5.6. The actual minimum required sampling rate is a function of the ratio of the highest frequency component, \( f_{\text{MAX}} \), to the total signal bandwidth, \( B \). Notice for large ratios of \( f_{\text{MAX}} \) to the bandwidth, \( B \), the minimum required sampling frequency approaches \( 2B \).
MINIMUM REQUIRED SAMPLING RATE AS A FUNCTION OF THE RATIO OF THE HIGHEST FREQUENCY COMPONENT TO THE TOTAL SIGNAL BANDWIDTH

Figure 5.6

Let us consider the case of a signal which occupies a bandwidth of 1MHz and lies between 6 and 7MHz as shown in Figure 5.7. Shannon's Information Theorem states that the signal (bandwidth = 1MHz) must be sampled at least at 2MSPS in order to retain all the information (avoid overlapping aliased components). Assuming that the ADC sampling rate, $f_s$, is 2MSPS, additional sampling frequencies are generated at all integer multiples of $f_s$: $4f_s$, $6f_s$, $8f_s$, etc. The actual signal between 6 and 7MHz is aliased around each of these sampling frequency harmonics, $f_s$, $2f_s$, $3f_s$, $4f_s$, ...., hence the term harmonic sampling. Notice that any one of the aliased components is an accurate representation of the original signal (the frequency inversion which occurs for one-half of the aliased components can be removed in software). In particular, the component lying in the baseband region between dc and 1MHz is the one calculated using a Fast Fourier Transform, and is also an accurate representation of the original signal, assuming no ADC conversion errors. The FFT output tells us all the characteristics of the signal except for its original position in the frequency spectrum, which was apriori knowledge.
INTERMEDIATE FREQUENCY (IF) SIGNAL BETWEEN 6 AND 7 MHz IS ALIASED BETWEEN DC AND 1MHz BY SAMPLING AT 2MSPS

Figure 5.7

A popular application of undersampling is in digital receivers. A simplified block diagram of a traditional digital receiver using baseband sampling is shown in Figure 5.8. The mixer in the RF section of the receiver mixes the signal from the antenna with the RF frequency of the local oscillator. The desired information is contained in relatively small bandwidth of frequencies Delta f. In actual receivers, Delta f may be as high as a few megahertz. The local oscillator frequency is chosen such that the Delta f band is centered about the IF frequency at the bandpass filter output. Popular IF frequencies are generally between 10 and 100MHz. The detector then translates the Delta f frequency band down to baseband where it is filtered and processed by a baseband ADC. Actual receivers can have several stages of RF and IF processing, but the simple diagram serves to illustrate the concepts.

SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

Figure 5.8

In a receiver which uses direct IF-to-digital techniques (often called undersampling, harmonic, bandpass, or IF sampling), the IF signal is applied directly to a wide bandwidth ADC as shown in Figure 5.9. The ADC sampling rate is chosen to be at least 2 Delta f. The process of sampling the IF frequency at the proper rate causes one of the aliased components of Delta f to appear in the dc to $f_s/2$ Nyquist
bandwidth of the ADC output. DSP techniques can now be used to process the
digital baseband signal. This approach eliminates the detector and its associated
noise and distortion. There is also more flexibility in the DSP because the ADC
sampling rate can be shifted to tune the exact position of the $\Delta f$ signal within the
baseband.

The obvious problem with this approach is that the ADC must now be able to
accurately digitize signals which are well outside the dc to $f_s/2$ Nyquist bandwidth
which most ADCs were designed to handle. Special techniques are available,
however, which can extend the dynamic range of ADCs to include IF frequencies.

**SIMPLIFIED DIGITAL RECIEVER USING IF SAMPLING**

![Diagram](image)

**Figure 5.9**

Let us consider a typical example, where the IF frequency is 72.5MHz, and the
desired signal occupies a bandwidth of 4MHz ($B=4\text{MHz}$), centered on the IF
frequency (see Figure 5.10). We know from the previous discussion that the
minimum sampling rate must be greater than 8MHz, probably on the order of
10MHz in order to prevent dynamic range limitations due to aliasing. If we place the
sampling frequency at the lower band-edge of 70MHz (72.5–2.5), we will definitely
recover the aliased component of the signal in the dc to 5MHz baseband. There is,
however, no need to sample at this high rate, so we may choose any sampling
frequency 10MHz or greater which is an integer sub-multiple of 70MHz, i.e., $70\div2 =
35.000\text{MHz}$, $70\div3 = 23.333\text{MHz}$, $70\div4 = 17.500\text{MHz}$, $70\div5 = 14.000\text{MHz}$, $70\div6 =
11.667\text{MHz}$, or $70\div7 = 10.000\text{MHz}$. We will therefore choose the lowest possible
sampling rate of $10.000\text{MHz}$ ($70\div7$).
INTERMEDIATE FREQUENCY (IF) SIGNAL AT 72.5MHz (±2MHz) IS ALIASED BETWEEN DC AND 5MHz BY SAMPLING AT 10MSPS

Figure 5.10

There is an advantage in choosing a sampling frequency which a sub-multiple of the lower band-edge in that there is no frequency inversion in the baseband alias as would be the case for a sampling frequency equal to a sub-multiple of the upper band-edge. (Frequency inversion can be easily dealt with in the DSP software should it occur, so the issue is not very important).

Undersampling applications such as the one just described generally require sampling ADCs which have low distortion at the high input IF input frequency. For instance, in the example just discussed, the ADC sampling rate requirement is only 10MSPS, but low distortion is required (preferably 60 to 80dB SFDR) at the IF frequency of 72.5MHz.

A large opportunity for bandpass sampling is in digital cellular radio base stations. For systems which have RF frequencies at 900MHz, 70MHz is a popular first-IF frequency. For systems using an RF frequency of 1.8GHz, first-IF frequencies between 200 and 240MHz are often used.

In broadband receiver applications, one ADC digitizes multiple channels in the receive path. Individual channel selection and filtering is done in the digital domain. Narrowband channel characteristics such as bandwidth, passband ripple, and adjacent channel rejection can be controlled with changes to digital parameters (i.e. filter coefficients). Such flexibility is not possible when narrowband analog filters are in the receive path.

Figure 5.11 illustrates the kind of input spectrum an ADC must digitize in a multichannel design. The spectral lines represent narrowband signal inputs from a variety of signal sources at different received power levels. Signal "C" could represent a transmitter located relatively far away from the signal sources "A" and "B". However, the receiver must recover all of the signals with equal clarity. This requires that distortion from the front-end RF and IF signal processing components,
including the ADC, not exceed the minimum acceptable level required to demodulate the weakest signal of interest. Clearly, third-order intermodulation distortion generated by "A" and "B" (2B - A, and 2A - B) will distort signals C and D if the nonlinearities in the front-end are severe. Strong out-of-band signals can also introduce distortion; signal "E" in Figure 5.11 shows a large signal that is partially attenuated by the antialiasing filter. In many systems, the power level of the individual transmitters is under control of the base station. This capability helps to reduce the total dynamic range required.

**BROADBAND DIGITAL RECEIVER ADC INPUT**

![BANDPASS FILTER RESPONSE](image)

**Figure 5.11**

In broadband receiver applications (using an RF frequency of approximately 900MHz, and a first-IF frequency of 70MHz), SFDR requirements for the ADC are typically 70 to 80dBc. Signal bandwidths between 5MHz and 10MHz are common, requiring corresponding sampling rates of 10MSPS to 20MSPS.

Sampling ADCs are generally designed to process signals up to Nyquist (f_s/2) with a reasonable amount of dynamic performance. As we have seen, however, even though the input bandwidth of a sampling ADC is usually much greater than its maximum sampling rate, the SFDR and effective bit (ENOB) performance usually decreases dramatically for full scale input signals much above f_s/2. This implies that the selection criteria for ADCs used in undersampling applications is SFDR or ENOB at the IF frequency, rather than sampling rate.

The general procedure for selecting an ADC for an undersampling application is not straightforward. The signal bandwidth and its location within the frequency spectrum must be known. The bandwidth of the signal determines the minimum sampling rate required, and in order to ease the requirement on the antialiasing filter, a sampling rate of 2.5 times the signal bandwidth works well. After determining the approximate sampling frequency needed, select the ADC based on the required SFDR, S/(N+D), or ENOB at the IF frequency. This is where the dilemma usually occurs. You will find that an ADC specified for a maximum sampling rate of 10MSPS, for instance, will not have adequate SFDR at the IF frequency (72.5MHz in the example above), even though its performance is excellent up to its Nyquist frequency of 5Mhz. In order to meet the SFDR, S/(N+D), or ENOB
requirement, you will generally require an ADC having a much higher sampling rate than is actually needed.

Figure 5.12 shows the approximate SFDR versus input frequency for the AD9022/AD9023 (20MSPS), AD9026/AD9027 (31MSPS), and the AD9042 (40MSPS) series of low distortion ADCs. Notice that the AD9042 has superior SFDR performance.

**SFDR COMPARISON BETWEEN 12-BIT SAMPLING ADCs**

The AD9042 is a state-of-the-art 12-bit, 40MSPS two stage subranging ADC consisting of a 6-bit coarse ADC and a 7-bit residue ADC with one bit of overlap to correct for any DNL, INL, gain or offset errors of the coarse ADC, and offset errors in the residue path. A block diagram is shown in Figure 5.13. A proprietary gray-code architecture is used to implement the two internal ADCs. The gain alignments of the coarse and residue, likewise the subtraction DAC, rely on the statistical matching of the process. As a result, 12-bit integral and differential linearity is obtained without laser trim. The internal DAC consists of 126 interdigitated current sources. Also on the DAC reference are an additional 20 interdigitated current sources to set the coarse gain, residue gain, and full scale gain. The interdigitization removes the requirement for laser trim. The AD9042 is fabricated on a high speed dielectrically isolated complementary bipolar process. The total power dissipation is only 575mW when operating on a single +5V supply.
AD9042 12-BIT, 40MSPS ADC KEY SPECIFICATIONS

- Input Range: 1V peak-to-peak, $V_{cm} = +2.4V$
- Input Impedance: 250$\Omega$ to $V_{cm}$
- Effective Input Noise: 0.33LSBs rms
- SFDR at 20MHz Input: 80dB
- S/(N+D) at 20MHz Input = 66dB
- Digital Outputs: TTL Compatible
- Power Supply: Single +5V
- Power Dissipation: 575mW
- Fabricated on High Speed Dielectrically Isolated Complementary Bipolar Process

The outstanding performance of the AD9042 is partly due to the use of differential techniques throughout the device. The low distortion input amplifier converts the single-ended input signal into a differential one. If maximum SFDR performance is desired, the signal source should be coupled directly into the input of the AD9042 without using a buffer amplifier. Figure 5.15 shows a method using capacitive coupling.
**INPUT STRUCTURE OF AD9042 ADC IS DESIGNED TO BE DRIVEN DIRECTLY FROM 50Ω SOURCE FOR BEST SFDR**

![Diagram of AD9042 ADC input structure](image)

**Figure 5.15**

**INCREASING ADC SFDR AND ENOB USING EXTERNAL SHAS**

An external SHA can increase the SFDR and ENOB of a sampling ADC for undersampling applications if properly selected and interfaced to the ADC. The SHA must have low hold-mode distortion at the frequency of interest. In addition, the acquisition time must be short enough to operate at the required sampling frequency. Figure 5.17 shows the effects of adding a SHA to an 8-bit flash converter. The ADC is clocked at 20MSPS, and the input frequency to the ADC is 19.98MHz. The scope photo shows the “beat” frequency of 2kHz reconstructed with an 8-bit DAC. Notice that without the SHA, the ADC has non-linearities and missing codes. The addition of the SHA (properly selected and timed) greatly improves the linearity and reduces the distortion.
THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

Figure 5.16

EFFECTS OF EXTERNAL SHA ON FLASH ADC PERFORMANCE FOR $f_{\text{in}} = 19.98\text{MHz}$, $f_s = 20.00\text{MSPS}$

Figure 5.17
Most SHAs are specified for distortion when operating in the track mode. What is of real interest, however, is the signal distortion in the hold mode when the SHA is operating dynamically. The AD9100 (30MSPS) and AD9101 (125MSPS) are ultra-fast SHAs and are specified in terms of hold-mode distortion. The measurement is done using a high performance low distortion ADC (such as the AD9014 14-bit, 10MSPS) to digitize the held value of the SHA output. An FFT is performed on the ADC output, and the distortion is measured digitally. For sampling rates greater than 10MSPS, the ADC is clocked at an integer sub-multiple of the SHA sampling frequency. This causes a frequency translation in the FFT output because of undersampling, but the distortion measurement still represents that of the SHA which is operating at the higher sampling rate. The AD9100 is optimized for low distortion up to 30MSPS, while the AD9101 will provide low distortion performance up to a sampling rate of 125MSPS. The low distortion performance of these SHAs is primarily due to the architecture which differs from the classical open-loop SHA architecture shown in Figure 5.18.

**CLASSIC OPEN-LOOP SHA ARCHITECTURE**

The sampling switch in the classic open-loop architecture is not within a feedback loop, and therefore distortion is subject to the non-linearity of the switch. The AD9100/AD9101 architecture shown in Figure 5.19 utilizes switches inside the feedback loop to achieve better than 12-bit AC and DC performance. The devices are fabricated on a high speed complementary bipolar process. In the track mode, S1 applies the buffered input signal to the hold capacitor, C_H, and S2 provides negative feedback to the input buffer. In the hold mode, both switches are disconnected from the hold capacitor, and negative feedback to the input buffer is supplied by S1. This architecture provides extremely low hold-mode distortion by maintaining high loop gains at high frequency. The output buffer can be configured to provide voltage gain (AD9101), which allows the switches to operate on lower common-mode voltage, thereby giving lower overall distortion.
CLOSED-LOOP SHA ARCHITECTURE
PROVIDES LOW DISTORTION AND HIGH SPEED
(AD9100, AD9101)

Figure 5.19

The hold-mode SFDR of the AD9100 is a function of the peak-to-peak input signal level and frequency as shown in Figure 5.20. Notice the data was taken as a sampling frequency of 10MSPS for three input amplitudes. The test configuration of Figure 5.21 was used to collect the data. For each input amplitude, the gain of the op amp between the AD9100 and the AD9014 ADC was adjusted such that the signal into the AD9014 was always full scale (2V peak-to-peak). Notice that optimum SFDR was obtained with a 200mV p-p input signal. Timing between the SHA and the ADC is critical. The SHA acquisition time should be long enough to achieve the desired accuracy, but short enough to allow sufficient hold-time for the ADC front-end to settle and yield a low-distortion conversion. For the test configuration shown, the optimum performance was achieved using an acquisition time of 20ns and a hold time of 80ns. The ADC is clocked close to the end of the SHA’s hold time. Best performance in this type of application is always achieved by optimizing the timing in the actual circuit.
Figure 5.20

TEST CONFIGURATION AND TIMING FOR MEASURING AD9100 SFDR AT 10MSPS

Figure 5.21

Figure 5.22 shows the SFDR of the AD9100 superimposed on the SFDR of the AD9026/AD9027 and the AD9042 ADCs. These data indicate that the AD9100 will significantly improve the SFDR of the AD9026/AD9027 ADC at the higher input frequencies. The performance of the AD9042 indicates that SFDR improvements will only occur at input frequencies above 40MHz.
The performance of the AD9100 SHA driving the AD9026/AD9027 ADC at a sampling frequency of 10MSPS is shown in Figure 5.23. The input signal is a 200mV peak-to-peak 71.4MHz sinewave. The amplifier between the SHA and the ADC is adjusted for a gain of 10. The SFDR is 72dBc, and the SNR is 62dB.

**FFT OUTPUT FOR AD9100 SHA DRIVING AD9026 ADC:**
INPUT = 200mV p-p, G = 10, f_s = 10MSPS, f_in = 71.4MHz

Similar dynamic range improvements can be achieved with high speed flash converters at higher sampling rates with the AD9101 SHA. The architecture is
similar to the AD9100, but the output buffer amplifier is optimized for a gain of 4 (see Figure 5.24). This configuration allows the front end sampler to operate at relatively low signal amplitudes, resulting in dramatic improvement in hold-mode distortion at high input frequencies and sampling rates up to 125MSPS. The AD9101 has an input bandwidth of 350MHz and an acquisition time of 7ns to 0.1% and 11ns to 0.01%.

AD9101 125MSPS SHA

![Diagram](image)

Figure 5.24

A block diagram and a timing diagram is shown for the AD9101 driving the AD9002 8 bit flash converter at 125MSPS (Figure 5.25). The corresponding dynamic range with and without the AD9101 is shown in Figure 5.26.
AD9101 SHA DRIVING AD9002 8-BIT, 125MSPS
FLASH CONVERTER FOR IMPROVED DYNAMIC RANGE

Figure 5.25

AD9002 DYNAMIC PERFORMANCE
WITH AND WITHOUT AD9101 SHA

Figure 5.26
USE OF DITHER SIGNALS TO INCREASE ADC DYNAMIC RANGE

In the development of classical ADC quantization noise theory, the assumption is usually made that the quantization error signal is uncorrelated with the ADC input signal. If this is true, then the quantization noise appears as random noise spread uniformly over the Nyquist bandwidth, dc to \( f_s/2 \), and it has an rms value equal to \( q/\sqrt{12} \). If, however, the input signal is locked to a non-prime integer submultiple of \( f_s \), the quantization noise will no longer appear as uniformly distributed random noise, but instead will appear as harmonics of the fundamental input sinewave. This is especially true if the input is an exact even submultiple of \( f_s \). Figure 5.27 illustrates the point using FFT simulation for an ideal 12 bit ADC. The FFT record length was chosen to be 4096. The spectrum on the left shows the FFT output when the input signal is an exact even submultiple (1/32) of the sampling frequency (the frequency was chosen so that there were exactly 128 cycles per record). The SFDR is approximately 78dBc. The spectrum on the right shows the output when the input signal is such that there are exactly 127 cycles per record. The SFDR is now about 92dBc which is an improvement of 14dB. Signal-correlated quantization noise is highly undesirable in spectral analysis applications, where it becomes difficult to differentiate between real signals and system-induced spurious components, especially when searching the spectrum for the presence of low-level signals in the presence of large signals.

EFFECTS OF SAMPLING A SIGNAL WHICH IS AN EXACT EVEN SUB-MULTIPLE OF THE ADC SAMPLING FREQUENCY

\( M = 4096 \), IDEAL 12-BIT ADC SIMULATION

![Figure 5.27](image)

There are a number of ways to reduce this effect, but the easiest way is to add a small amount of broadband rms noise to the ADC input signal as shown in Figure 5.28. The rms value of this noise should be equal to about 1/2 LSB. The effect of this is to randomize the quantization noise and eliminate its possible signal-dependence. In most systems, there is usually enough random noise present on the input signal so that this happens automatically. This is especially likely when using high speed ADCs which have 12 or more bits of resolution and a relatively small input range of 2V p-p or less. The total noise at the ADC is composed of the noise of the input signal, the effective input noise of the ADC, and an additional component caused by
the effects of the sampling clock jitter. In most cases, the rms value of the total ADC input noise is greater than 1/2 LSB.

THE ADDITION OF WIDEBAND GAUSSIAN NOISE TO THE ADC INPUT RANDOMIZES QUANTIZATION NOISE AND REMOVES INPUT SIGNAL DEPENDENCE

![Diagram](image)

Figure 5.28

EFFECT OF ADC LINEARITY AND RESOLUTION ON SFDR AND NOISE IN DIGITAL SPECTRAL ANALYSIS APPLICATIONS

In order to understand the relationships between ADC resolution, noise, and Spurious Free Dynamic Range (SFDR), it is first necessary to review some of the issues relating to digital spectral analysis, specifically the FFT. The FFT takes a discrete number of time samples, M, and converts them into M/2 discrete spectral components. The spacing between the spectral lines is Delta f = f_s/M. When a full scale sine wave signal is applied to an ADC having a resolution of N bits, the theoretical rms signal to rms noise ratio is 6.02N + 1.76dB. If the quantization noise is uncorrelated with the signal, it appears as gaussian noise spread uniformly over the bandwidth dc to f_s/2. The FFT acts as a narrowband filter with a bandwidth of Delta f, and the FFT noise floor is therefore 10log_{10}(M/2) dB below the broadband quantization noise level (6.02N + 1.76dB). The FFT noise floor is pushed down by 3dB each time the FFT record length, M, is doubled (see Figure 5.29). This reduction in the noise floor is the same effect achieved by narrowing the bandwidth of an analog spectrum analyzer to a bandwidth of f_s/M.

For example, a 4096-point FFT has a noise floor which is 33dB below the theoretical broadband rms quantization noise floor of 74dB for a 12-bit ADC as shown in Figure 5.30 (where the average noise floor is about 74 + 33 = 107dB below full scale). Notice that there are random peaks and valleys around the average FFT noise floor. These
peaks (due to quantization noise, FFT artifacts, and roundoff error) limit the ideal SFDR to about 92dBc.

**RELATIONSHIP BETWEEN AVERAGE NOISE IN FFT BINS AND BROADBAND RMS QUANTIZATION NOISE LEVEL**

![Diagram of relationship between average noise in FFT bins and broadband RMS quantization noise level.](image)

**Figure 5.29**
NOISE FLOOR FOR AN IDEAL 12-BIT ADC USING 4096-POINT FFT

Figure 5.30

Approximately the same dynamic range could be achieved by reducing the resolution of the ADC to 11 bits and using a 16,384 point FFT. There is a tradeoff, however, because lower resolution ADCs tend to have quantization noise which is correlated to the input signal, thereby producing larger frequency spurs. Averaging the results of several FFTs will tend to smooth out the FFT noise floor, but does nothing to reduce the average noise floor.

Using more bits improves the SFDR only if the ADC AC linearity improves with the additional bits. For instance, there would be little advantage in using a 14-bit ADC which has only 12-bit linearity. The extra bits would only serve to slightly reduce the overall noise floor, but the improvement in SFDR would be only marginal.

FUTURE TRENDS IN UNDERSAMPLING ADCs

Future ADCs specifically designed for undersampling applications will incorporate the previously discussed techniques in a single-chip designs. These ADCs will be characterized by their wide SFDR at input frequencies extending well above the Nyquist limit, f_s/2. The basic architecture of the digital IF receiver is shown in Figure 5.31. The addition of a low-distortion PGA under DSP control increases the dynamic range of the system. IF frequencies associated with 900MHz digital cellular base stations are typically around 70MHz with bandwidths between 5 and 10MHz. SFDR requirements are between 70 and 80dBc. On the other hand, 1.8GHZ digital receivers typically have IF frequencies between 200 and 240MHz with bandwidths of 1MHz. SFDR requirements are typically 50dBc.
Figure 5.31

The bandpass sigma-delta architecture offers interesting possibilities in this area. Traditional sigma-delta ADCs contain integrators, which are lowpass filters. They have passbands which extend from DC, and the quantization noise is pushed up into the higher frequencies. At present, all commercially available sigma-delta ADCs are of this type (although some which are intended for use in audio or telecommunications contain bandpass filters to eliminate any DC response).

There is no particular reason why the filters of the sigma-delta modulator should be lowpass filters, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a sigma-delta ADC with bandpass filters as shown in Figure 5.32, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the passband (see Figure 5.33). If the digital filter is then programmed to have its passband in this noise-free region, we have a sigma-delta ADC with a bandpass, rather than a lowpass characteristic.
The theory is straightforward, but the development of a sigma-delta ADC is expensive, and there is no universal agreement on ideal characteristics for such a bandpass sigma-delta ADC, so developing such a converter from scratch to verify the theory would be unlikely to yield a commercial product. Researchers at Analog Devices and the University of Toronto (See References 16, 17, and 18) have therefore modified a commercial baseband (audio) sigma-delta ADC chip by rewiring its integrators as switched capacitor bandpass filters and reprogramming its digital
filter and decimator. This has provided a fast, and comparatively inexpensive, proof of the concept, but at the expense of relative low Effective Bits (11-bits), the result of less than ideal bandpass filters. Nevertheless the results are extremely encouraging and open the way to the design of purpose-built bandpass sigma-delta ADC chips for specific ASIC applications, especially, but not exclusively, radio receivers.

The overall performance characteristics of the experimental ADC are shown in Figure 5.34. The device was designed to digitize the popular radio IF frequency of 455kHz.

### SUMMARY OF RESULTS FOR EXPERIMENTAL BANDPASS SIGMA-DELTA ADC

- Center Frequency: 455kHz
- Bandwidth: 10kHz
- Sampling Rate: 1.852MSPS
- Oversampling Ratio: 91
- SNR in Specified Band: 65dB
- Supply: ±5V, Power: 750mW
- Process: 3μm CMOS, Active Area: 1.8 x 3.4 mm

![Figure 5.34](image_url)

In the future it may be possible to have such bandpass sigma-delta ADCs with user-programmable digital filter coefficients, so that the passband of a receiver could be modified during operation in response to the characteristics of the signal (and the interference!) being received. Such a function is very attractive, but difficult to implement, since it would involve loading, and storing, several hundreds or even thousands of 16-22 bit filter coefficients, and would considerably increase the size, and cost, of the converter.

A feature which could be added comparatively easily to a sigma-delta ADC is a more complex digital filter with separate reference (I) and quadrature (Q) outputs. Such a feature would be most valuable in many types of radio receivers.

Technology exists today which should allow the bandpass sigma-delta architecture to achieve 16-bit resolution, SFDR of 70 to 80dBc, and an effective throughput rate of 10 to 20MSPS (input sampling rate = 100MSPS, corresponding to an oversampling ratio of 5 to 10). This would allow 40MHz IF with a 2MHz bandwidth to be digitized directly.
CHARACTERISTICS OF A BANDPASS SIGMA-DELTA ADC DESIGN FOR IF-SAMPLING

- IF Frequency: 40 to 70MHz
- Signal Bandwidth: 2MHz
- Input Sampling Rate: 100MSPS
- Output Data Rate: 10 to 20MSPS
- Process: BiCMOS

Figure 5.35

EFFECTS OF SAMPLING CLOCK JITTER IN UNDERSAMPLING APPLICATIONS

The effects of sampling clock jitter on Signal-to-Noise Ratio (SNR) and Effective Bit (ENOB) performance discussed in Section 3 are even more dramatic in undersampling applications because of the higher input signal frequencies. Figure 5.36 shows the relationship between sampling clock jitter and SNR previously presented.

Consider the case where the IF frequency is 70MHz, and 12-bit dynamic range is required (70 to 80dB). From Figure 5.36, the rms sampling clock jitter required to maintain this SNR is approximately 1ps rms. This assumes an ideal ADC with no internal aperture jitter. ADC aperture jitter combines with the sampling clock jitter in an rms manner to further degrade the SNR.

SNR DUE TO SAMPLING CLOCK JITTER ($t_j$)

![SNR vs. Fullscale Sinewave Input Frequency](image)

Figure 5.36
The implications of this analysis are extremely important in undersampling applications. The ADC aperture jitter must be minimal, and the sampling clock generated from a low phase-noise quartz crystal oscillator. Furthermore, the oscillator should use discrete bipolar and FET devices in the circuits recommended by the crystal manufacturers. The popular oscillator design which uses a resistor, one or more logic gates, a quartz crystal, and a couple of capacitors should never be used! For very high frequency clocks, a surface acoustic wave (SAW) oscillator is preferable.

**SAMPLING CLOCK OSCILLATORS**

![Sampling Clock Oscillators Diagram](image)

The sampling clock should be isolated as much as possible from the noise present in the digital parts of the system. There should be few or no logic gates in the sampling clock path, as a single ECL gate has approximately 4ps rms timing jitter. The sampling clock generation circuitry should be on separate chips, perhaps with separately decoupled power supplies, from the remainder of the digital system, and the sampling clock signal lines should not be located where they can pick up digital noise from the rest of the system. All sampling clock circuitry should be grounded and decoupled to the analog ground plane, as would be the case for a critical analog component.

Of course, the sampling clock is itself a digital signal. It has as much potential for causing noise in the analog part of the system as any other digital signal. We therefore see that a sampling clock is very inconvenient, as it must be isolated from both the analog and digital parts of the system.

Because the sampling clock jitter is wideband and therefore creates wideband random noise, digital filtering can be used to reduce its effects in a system. In the case of an FFT, however, doubling the FFT record length reduces the noise floor by only 3dB.

This discussion illustrates the basic fact that undersampling systems have fundamental limitations with respect to their ability to process wide dynamic range broadband signals, and system tradeoffs between broadband and narrowband approaches must ultimately be made in the design of such systems.
SAMPLING CLOCK NOISE

- Low phase-noise crystal (or SAW) oscillators mandatory in high frequency undersampling applications

- Ground and decouple sampling clock circuitry to the Analog Ground Plane!

- Route sampling clock away from digital and analog signals

- Digital filtering techniques can be used to reduce the effects of sampling clock phase noise

- Sampling clock noise can ultimately dictate the tradeoffs between broadband and narrowband digital receivers

Figure 5.38
REFERENCES


SECTION 6

MULTICHANNEL APPLICATIONS

- Data Acquisition System Considerations
- Multiplexing
- Filtering Considerations for Data Acquisition Systems
- SHA and ADC Settling Time Requirements in Multiplexed Applications
- Complete Data Acquisition Systems on a Chip
- Multiplexing into Sigma-Delta ADCs
- Simultaneous Sampling Systems
- Data Distribution Systems using Multiple DACs
SECTION 6

MULTICHANNEL APPLICATIONS
Walt Kester, Wes Freeman

DATA ACQUISITION SYSTEM CONFIGURATIONS

There are many applications for data acquisition systems in measurement and process control. All data acquisition applications involve digitizing analog signals for analysis using ADCs. In a measurement application, the ADC is followed by a digital processor which performs the required data analysis. In a process control application, the process controller generates feedback signals which typically must be converted back into analog form using a DAC.

Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term data acquisition generally refers to multi-channel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as data distribution.

Figure 6.1 shows a data acquisition/distribution process control system where each channel has its own dedicated ADC and DAC. An alternative configuration is shown in Figure 6.2, where analog multiplexers and demultiplexers are used with a single ADC and DAC. In most cases, especially where there are many channels, this configuration provides an economical alternative.
There are many tradeoffs involved in designing a data acquisition system. Issues such as filtering, amplification, multiplexing, demultiplexing, sampling frequency, and partitioning must be resolved.

**MULTIPLEXING**

Multiplexing is a fundamental part of a data acquisition system. Multiplexers and switches are examined in more detail in Reference 1, but a fundamental understanding is required to design a data acquisition system. A simplified diagram of an analog multiplexer is shown in Figure 6.3. The number of input channels typically ranges from 4 to 16, and the devices are generally fabricated on CMOS processes. Some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs must be grounded or severe loss of system accuracy may result. The key specifications are switching time, on-resistance, on-resistance modulation, and off-channel isolation (crosstalk). Multiplexer switching time ranges from about 50ns to over 1µs, on-resistance from 25ohms to several hundred ohms, and off-channel isolation from 50 to 90dB. The use of trench isolation has eliminated latch-up in multiplexers while yielding improvements in speed at low supply voltages.
SIMPPLIFIED DIAGRAM OF A TYPICAL ANALOG MULTIPLEXER

Figure 6.3

MULTIPLEXER KEY SPECIFICATIONS

- Switching Time: 50ns to >1μs
- On-Resistance: 25Ω to hundreds of Ω’s
- On-Resistance Modulation (Ron change with signal level)
- Off-Channel Isolation: 50 to 90 dB
- Overvoltage Protection

Figure 6.4
WHAT’S NEW IN MULTIPLEXERS?

- **Trench Isolation** gives high speed, latch-up protection, and low-voltage operation

- **ADG511, ADG512, ADG513**: +3.3V, +5V, ±5V specified
  - $R_{on} < 50\,\Omega$ @ ±5V
  - **Switching Time**: <200ns @ ±5V

- **ADG411, ADG412, ADG413**: ±15V, +12V specified
  - $R_{on} < 35\,\Omega$
  - ±15V **Switching Time**: <150ns @ ±15V

- **ADG508F, ADG509F, ADG528F**: ±15V specified
  - $R_{on} < 300\,\Omega$
  - **Switching Time**: <250ns
  - Fault-Protection on Inputs and Outputs

**Figure 6.5**

Multiplexer on-resistance is generally slightly dependent on the signal level (often called $R_{on}$ modulation). This will cause signal distortion if the multiplexer must drive a load resistance, therefore the multiplexer output should therefore be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC - but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer. A detailed analysis of multiplexers can be found in Reference 1, Section 8, or Reference 2, Section 2.

An M-channel multiplexed data acquisition system is shown in Figure 6.6. The multiplexer output drives a PGA whose gain can be adjusted on a per-channel basis depending on the channel signal level. This ensures that all channels utilize the full dynamic range of the ADC. The PGA gain is changed at the same time as the multiplexer is switched to a new channel. The ADC *Convert Command* is applied after the multiplexer and the PGA have settled to the required accuracy (1LSB). The maximum sampling frequency (when switching between channels) is limited by the multiplexer switching time $t_{mux}$, the PGA settling time $t_{pga}$, and the ADC conversion time $t_{conv}$ as shown in the formula.
In a multiplexed system it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the other. When the multiplexer switches between these channels its output is a fullscale step voltage. All elements in the signal path must settle to the required accuracy (1LSB) before the conversion is made. The effect of inadequate settling is dc crosstalk between channels.

The SAR ADC chosen in this application has no internal SHA (similar to the industry-standard AD574-series), and therefore the input signal must be held constant (within 1LSB) during the conversion time in order to prevent encoding errors. This defines the maximum rate-of-change of the input signal:

\[ \frac{dv}{dt}_{\text{max}} \leq \frac{1 \text{ LSB}}{t_{\text{conv}}} \]

The amplitude of a fullscale sinewave input signal is equal to \((2^N)/2\), or \(2^{(N-1)}\), and its maximum rate-of-change is

\[ \frac{dv}{dt}_{\text{max}} = 2\pi f_{\text{max}} \cdot 2^{N-1} = \pi f_{\text{max}} \cdot 2^N \]

Setting the two equations equal, and solving for \(f_{\text{max}}\),

\[ f_{\text{max}} \leq \frac{1}{\pi \cdot 2^N t_{\text{conv}}} \]

For example, if the ADC conversion time is 20\(\mu\text{sec}\) (corresponding to a maximum sampling rate of slightly less than 50kSPS), and the resolution is 12-bits, then the
The maximum channel input signal frequency is limited to 4Hz. This may be adequate if the signals are DC, but the lack of a SHA function severely limits the ability to process dynamic signals.

Adding a SHA function to the ADC as shown in Figure 6.7 allows processing of much faster signals with almost no increase in system complexity, since sampling ADCs such as the AD1674 have the SHA function on-chip.

**THE ADDITION OF A SHA FUNCTION TO THE ADC ALLOWS PROCESSING OF DYNAMIC INPUT SIGNALS**

![Figure 6.7](image1)

![Figure 6.8](image2)

The timing is adjusted such that the multiplexer and the PGA are switched immediately following the acquisition time of the SHA. If the combined multiplexer and PGA settling time is less than the ADC conversion time (see Figure 6.8), then the maximum sampling frequency of the system is given by:
\[
f_s \leq \frac{1}{t_{\text{acq}} + t_{\text{conv}}}
\]

The AD1674 has a conversion time of 9\(\mu\)s, an acquisition time of 1\(\mu\)s to 12-bits, and a sampling rate of 100kSPS is possible, if all the channels are addressed. The per-channel sampling rate is obtained by dividing the ADC sampling rate by M.

**FILTERING CONSIDERATIONS IN DATA ACQUISITION SYSTEMS**

Filtering in data acquisition systems not only prevents aliasing of unwanted signals but also reduces noise by limiting bandwidth. In a multiplexed system, there are basically two places to put filters: in each channel, and at the multiplexer output.

**FILTERING IN A DATA ACQUISITION SYSTEM**

The filter at the input of each channel is used to prevent aliasing of signals which fall outside the Nyquist bandwidth. The per-channel sampling rate (assuming each channel is sampled at the same rate) is \(f_s/M\), and the corresponding Nyquist frequency is \(f_s/2M\). The filter should provide sufficient attenuation at \(f_s/2M\) to prevent dynamic range limitations due to aliasing.

A second filter can be placed in the signal path between the multiplexer output and the ADC, usually between the PGA and the SHA. The cutoff frequency of this filter must be carefully chosen because of its impact on settling time. In a multiplexed system such as shown in Figure 6.7, there can be a fullscale step voltage change at the multiplexer output when it is switched between channels. This occurs if the signal on one channel is positive fullscale, and the signal on the adjacent channel is negative fullscale. From the timing diagram shown in Figure 6.8, the signal from the filter has essentially the entire conversion period \((1/f_s)\) to settle from the step voltage. The signal should settle to within 1LSB of the final value in order not to introduce a significant error. The settling time requirement therefore places a lower limit on the filter’s cutoff frequency. The single-pole filter settling time required to maintain a given accuracy is shown in Figure 6.10. The settling time requirement is
expressed in terms of the filter time constant and also the ratio of the filter cutoff frequency, \( f_{c2} \), to the ADC sampling frequency, \( f_s \).

**SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY**

<table>
<thead>
<tr>
<th>RESOLUTION, # OF BITS</th>
<th>LSB (%FS)</th>
<th># OF TIME CONSTANTS</th>
<th>( f_{c2}/f_s )</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>1.563</td>
<td>4.16</td>
<td>0.67</td>
</tr>
<tr>
<td>8</td>
<td>0.391</td>
<td>5.55</td>
<td>0.89</td>
</tr>
<tr>
<td>10</td>
<td>0.0977</td>
<td>6.93</td>
<td>1.11</td>
</tr>
<tr>
<td>12</td>
<td>0.0244</td>
<td>8.32</td>
<td>1.32</td>
</tr>
<tr>
<td>14</td>
<td>0.0061</td>
<td>9.70</td>
<td>1.55</td>
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<td>0.00038</td>
<td>12.48</td>
<td>2.00</td>
</tr>
<tr>
<td>20</td>
<td>0.000095</td>
<td>13.88</td>
<td>2.22</td>
</tr>
<tr>
<td>22</td>
<td>0.000024</td>
<td>15.25</td>
<td>2.44</td>
</tr>
</tbody>
</table>

**Figure 6.10**

As an example, assume that the ADC is a 12-bit one sampling at 100kSPS. From the table in Figure 6.10, 8.32 time constants are required for the filter to settle to 12-bit accuracy, and

\[
\frac{f_{c2}}{f_s} \geq 132, \text{ or } f_{c2} \geq 132\text{kSPS}.
\]

While this filter will help prevent wideband noise from entering the SHA, *it does not provide the same function as the antialiasing filters at the input of each channel.*

The above analysis assumes that the multiplexer/PGA combined settling time is significantly less than the filter settling time. If this is not the case, then the filter cutoff frequency must be larger, and in most cases it should be left out entirely in favor of per-channel filters.

**SHA AND ADC SETTLING TIME REQUIREMENTS IN MULTIPLEXED APPLICATIONS**

We have discussed the importance of the fullscale settling time of the multiplexer/PGA/filter combination, but what is equally important is the ability of the ADC to acquire the final value of the step voltage input signal to the required accuracy. Failure of any link in the signal chain to settle will result in dc crosstalk between adjacent channels and loss of accuracy. If the data acquisition system uses a separate SHA and ADC, then the key specification to examine is the SHA *acquisition time*, which is usually specified as a the amount of time required to acquire a fullscale input signal to 0.1% accuracy (10-bits) or 0.01% accuracy (13-
bits). In most cases, both 0.1% and 0.01% times are specified. If the SHA acquisition time is not specified for 0.01% accuracy or better, it should not be used in a 12-bit multiplexed application.

If the ADC is a sampling one (with internal SHA), the SHA acquisition time required to achieve a level of accuracy may still be specified, as in the case of the AD1674 (1µs to 12-bit accuracy). SHA acquisition time and accuracy are not directly specified for some sampling ADCs, so the transient response specification should be examined. The transient response of the ADC (settling time to within 1 LSB for a fullscale step input) must be less the 1/fs, where f_s is the ADC sampling rate. This often ignored specification may become the weakest link in the signal chain. In some cases neither the SHA acquisition time to specified accuracy nor the transient response specification may appear on the data sheet for the particular ADC, in which case it is probably not acceptable for multiplexed applications. Because of the difficulty in measuring and achieving better than 12-bit settling times using discrete components, the accuracy of most multiplexed data acquisition systems is limited to 12-bits. Designing multiplexed systems with greater accuracy is extremely difficult, and using a single ADC per channel should be strongly considered at higher resolutions.

SHA AND ADC CONSIDERATIONS IN MULTIPLEXED DATA ACQUISITION SYSTEMS

- Examine SHA Acquisition Time Specification to Required Accuracy:
  - 0.1% = 10-bits
  - 0.01% = 13-bits
- If Sampling ADC, SHA Acquisition Time may not be given, so examine Transient Response Specification
- Inadequate Settling Results in Loss of Accuracy and Causes DC Crosstalk Between Channels
- Multiplexing at greater than 12-bits Accuracy, or at Video Speeds is Extremely Difficult!

Figure 6.11

COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data
acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self-calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels, a SHA, an internal voltage reference, and a fast 12-bit ADC. Input scaling allows up to ±10V inputs when operating on a single +5V supply. Its block diagram is shown in Figure 6.12, and key specifications are summarized in Figure 6.13. Both AC and DC parameters are fully specified, simplifying the preparation of an error budget, and three types are available with three different standard input ranges:

<table>
<thead>
<tr>
<th>Type</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD7890-10</td>
<td>±10 V</td>
</tr>
<tr>
<td>AD7890-5</td>
<td>0 to 5V</td>
</tr>
<tr>
<td>AD7890-2</td>
<td>0 to +2.5V</td>
</tr>
</tbody>
</table>

![AD7890 Block Diagram](image)

**Figure 6.12**
AD7890 SPECIFICATIONS

- ADC Conversion Time: \( 5.9\mu s \)
- SHA Acquisition Time: \( 2\mu s \)
- 117kSPS Throughput Rate (Includes 0.6\mu s Overhead)

AC and DC Specifications

- Single +5V Operation
- Low Power Drain:
  - Operational: 30mW
  - Power Down Mode: 1mW

- Standard Input Ranges
  - AD7890 - 10: \( \pm 10V \)
  - AD7890 - 5: 0 to +5V
  - AD7890 - 2: 0 to +2.5V

Figure 6.13

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the CONVST pin.

With the serial clock rate at its maximum of 10MHz, the achievable throughput rate for the AD7890 is 5.9\mu s (conversion time) plus 0.6\mu s (six serial clocks of internal overhead) plus 2\mu s (acquisition time). This results in a minimum throughput time of 8.5\mu s (equivalent to a throughput rate of 117kSPS). The AD7890 draws 30mW from a +5V supply.

The entire family of AD789X 12-bit data acquisition ADCs is shown in Figure 6.14. The AD7890 and AD7891 are complete 8-channel data acquisition systems, while the AD7892, AD7893, and AD7896 are designed for use on a single channel, or with an external multiplexer.
The AD785X 12-bit low power data acquisition ADCs have been designed and fully specified for either +3V or +5V operation. This family includes parallel and serial single and 8-channel versions. The devices have self or system calibration modes for offset, gain, and the internal SAR DAC.

**Figure 6.14**

**AD785X SERIES OF 3V / 5V 12-BIT ADCs**

As was discussed in Section 3, the digital filter is an integral part of a sigma-delta ADC. When the input to a sigma-delta ADC changes by a large step, the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not inherently so, but the time taken to change channels can be inconvenient.

As an example, the AD7710-family of ADCs contains an on-chip multiplexer (see Figure 6.16), and the digital filter (frequency response shown in Figure 6.17)
requires three conversion cycles (300ms at a 10Hz throughput rate) to settle. It is thus possible to multiplex sigma-delta converters, provided adequate time is allowed for the internal digital filter to settle.

THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE

Figure 6.16

AD7710 DIGITAL FILTER FREQUENCY RESPONSE

- Response Follows a $\text{sinc}^3 = \left(\frac{\sin x}{x}\right)^3$
- First Notch Frequency is Programmable and given by:
  \[ f_{\text{notch}} = \frac{f_{\text{clk}in}}{512} \left(\frac{1}{\text{Decimal Value of Digital Code}}\right) \]
- For $f_{\text{clk}in} = 10\text{MHz}$, $9.76\text{Hz} \leq f_{\text{notch}} \leq 1.028\text{kHz}$

Figure 6.17
THE RATE OF CONVERSION AND SETTLING TIME DEPENDS ON THE FILTER SETTING

Figure 6.18

In the case of the AD771X-series, four conversions must take place after a channel change before the output data is again valid (Figure 6.18). The SYNC input pin resets the digital filter and, if it is used, data is valid on the third output afterwards, saving one conversion cycle. When the internal multiplexer is switched, the SYNC is automatically operated.

If sigma-delta ADCs are used in multi-channel applications, consider using one sigma-delta ADC per channel as shown in Figure 6.19. This eliminates the requirement for an analog multiplexer but requires that the outputs be synchronized in simultaneous sampling applications. Although the inputs are sampled at the same instant at a rate Kf_S, the decimated output frequency, f_S, is generally derived internally in each ADC by dividing the input sampling frequency by K (the oversampling rate). The output data must therefore be synchronized by the same clock at a frequency f_S.
Products such as the AD7716 include multiple sigma-delta ADCs in a single IC, and provide the synchronization automatically. The AD7716 is a quad sigma-delta ADC with up to 22-bit resolution and an over-sampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 6.20 and some of its key features in Figure 6.21. The device does not have a "start conversion" control input, but samples continuously. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by data written to the DAS. The output register is updated at a rate which depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.
AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES

- Up to 22-Bit Resolution, 4 Input Channels
- \(\Sigma\Delta\) Architecture, 570kSPS Oversampling Rate
- On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz
- Serial Input / Output Interface
- \(\pm 5\)V Power Supply Operation
- Low Power: 50mW

**SIMULTANEOUS SAMPLING SYSTEMS**

There are certain applications where it is desirable to sample a number of channels simultaneously such as in-phase and quadrature (I and Q) signal processing. A typical configuration is shown in Figure 6.22. Each channel requires its own filter and SHA. Each SHA is simultaneously placed in the *hold* mode by a common command signal. During the input SHAs' hold time the multiplexer is sequentially switched from channel to channel, and the single non-sampling ADC is used to digitize the signal on each channel. The maximum ADC sampling rate is the reciprocal of the sum of the multiplexer settling time, \(t_{\text{mux}}\), and the ADC conversion time, \(t_{\text{conv}}\).
The maximum per-channel sampling frequency is determined by $M$, $t_{\text{mux}}$, $t_{\text{conv}}$, and the acquisition time of the simultaneous SHAs, $t_{\text{acq1}}$.

$$f_{s1} \leq \frac{1}{t_{\text{acq1}} + M(t_{\text{mux}} + t_{\text{conv}})}$$


SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING NON-SAMPLING ADC

If a sampling ADC is used to perform the conversion (see Figure 6.23), the acquisition time of the second SHA, $t_{\text{acq2}}$, must be considered in determining the maximum ADC sampling rate, $f_{s2}$. The multiplexer should be switched to the next channel after the single SHA goes into the hold mode. If the multiplexer settling time is less than the ADC conversion time, then the maximum ADC sampling rate $f_{s2}$ is the reciprocal of the sum of the SHA acquisition time and the ADC conversion time.

$$f_{s2} \leq \frac{1}{t_{\text{acq2}} + t_{\text{conv}}}$$

The maximum input sampling frequency is less than this value divided by $M$, where $M$ is the number of channels. Additional timing overhead ($t_{\text{acq1}}$) is required for the simultaneous SHAs to acquire the signals.

$$f_{s1} < \frac{1}{t_{\text{acq1}} + M(t_{\text{conv}} + t_{\text{acq2}})}$$

---

Figure 6.22
In many industrial and process control applications, multiple programmable voltage sources are required. Traditionally, these applications have required a large number of components, but recent product developments have greatly reduced the parts count without compromising performance.

**DATA DISTRIBUTION SYSTEM USING MULTIPLE DACs**

- Many systems require multiple, programmable voltages
  - Automatic Test Equipment (ATE)
  - Robotics
  - Industrial Automation
  - System Calibration
  - Ultrasound/Sonar Power Gain and Receiver Level

Multiple voltage outputs can either be derived by demultiplexing the output of a single DAC or by employing multiple DACs. These two approaches are shown in Figure 6.25. In the demultiplexed circuit, one DAC feeds the inputs of several sample-and-hold amplifiers (SHA). The equivalent digital value for the analog output is applied to the DAC, and the appropriate SHA is selected. After the DAC settling time and SHA acquisition time requirements have been met, the SHA can be deselected and the next channel updated. Once a SHA is deselected, the output voltage will begin to droop at a rate specified for the SHA. Thus, the SHA must be refreshed before the output voltage droop exceeds the required accuracy (typically 1/2 LSB).
OPTIONS FOR ANALOG DATA DISTRIBUTION

The multiple DAC application is straightforward. One DAC is provided for each channel, and an address decoder simply selects the appropriate DAC. No refresh is required.

The DAC plus SHA system evolved because, in the past, DACs were more expensive than SHAs. This situation was particularly true for DACs with resolution above 8 bits. In addition, multiple-SHAs with on-chip hold capacitors reduced the parts count, printed circuit board area, and cost of demultiplexed DAC systems. Finally, the demultiplexed DAC only requires one calibration step, since the same DAC provides the output voltage for each of the output channels. Of course, single-calibration is only valid if the SHA does not introduce unacceptable errors. For example, the SMP08 is an 8-channel SHA which exhibits a 10mV maximum offset voltage and is accurate to 1/2 LSB when demultiplexing an 8-bit, 5V full-scale DAC.

WHY DEMULTIPLEX A SINGLE DAC?

- Cost of DAC > Cost of SHA
- Multichannel SHAs (e.g. SMP-08/SMP-18) Reduce Parts Count
- Only One Calibration Required

A representative 16-channel, 8-bit demultiplexed data distribution system is shown in Figure 6.27. The DAC8228 produces a voltage output which is applied to the input of 16 SHAs. The DAC digital value is written into the DAC8228 at the same time as the channel address is presented to the SHA. After the SHA’s acquisition time requirement has been satisfied, the next channel can be refreshed. The SMP08’s acquisition time to 0.1% is 7µs, so the maximum data transfer rate is the reciprocal of the acquisition time, or 140kHz.
Once a SHA channel is deselected, the input bias current of the amplifier begins to discharge the hold capacitor. The rate at which the capacitor voltage changes is specified on the SHA data sheet as the droop rate. With a maximum droop rate of 20mV/s, the SMP08 can maintain 8-bit accuracy (1/2 LSB at 5V full scale) provided refreshing occurs once each 500ms.

The SMP08 is a complete, single-chip 8-channel SHA, which incorporates analog switches, hold capacitors, amplifiers, and address decoders. Each SMP08 replaces 17 components (8 SHAs, 8 hold capacitors, and one decoder). Even with this level of integration, however, the complete data distribution circuit still requires six components.

Operation of the demultiplexed DAC is shown in Figure 6.28. With the DAC output at 5V, the system refreshes CH0 once each second. The upper trace is the address decode output which goes low to select CH0. The lower trace is the output of CH0's SHA. While the address input is low, the DAC's output is connected to the input of CH0's SHA. When the address input goes high, the SMP08 maintains less than 1/4 LSB error for one second. Thus, the droop rate of this particular SMP08 is about 2mV/sec. The photo also shows a 1mV hold step when switching from sample to hold mode.
At first glance, demultiplexed DAC systems may appear to be more cost-effective than multiple DACs. However, several factors combine to reduce the system cost when a multiple DAC is used (Figure 6.29). For example, advances in integrated circuit fabrication, trimming and testing have combined to improve yields and reduce costs. Process improvements produce transistors and resistors with better matching, which reduces trimming requirements. At the same time, improvements in laser trimming and testing permit more accurate matching of multiple devices on one die. While these advances also have an effect on the costs of demultiplexed systems, the economics of IC fabrication are such that the impact of improvements is relatively greater on multiple DAC devices. As a result of these improvements, multiple DACs are very cost competitive with demultiplexed systems on a per-channel basis.
WHY USE A MULTIPLE-DAC SOLUTION?

- Cost
  - Laser Trimming Aids Matching
  - Lower Parts Count
  - Reduced Design Time

- Additional System Features
  - Less Microcontroller Overhead
  - Faster Update Rate
  - Synchronized Outputs
  - Power-On Reset
  - Read-Back Capability
  - Serial Interface

Figure 6.29

Another advantage of the multiple-DAC system is reduced parts count. While cost estimates may vary, the advantages of eliminating components in a design cannot be ignored. Among these advantages are reduced pin count, printed circuit board area, inventory, incoming inspection, and purchasing transactions.

Reducing design time also contributes to cost savings. From a design engineering point of view, design time is both a critical and a very visible factor in the "time-to-market" equation. Reducing parts count can have a major impact on design time by reducing device evaluation time, interface timing analyses, error budget analyses, printed circuit board layout, etc.

The real advantages of the single-chip multiple DAC, however, lie in the features that are difficult or impossible to add with a demultiplexed circuit. These advantages include:

1. No refresh cycle is required. As previously mentioned, the demultiplexed DAC must constantly be refreshed. The minimum time between refresh cycles is set by the required system accuracy (typically 1/2 LSB), SHA droop rate, and LSB voltage value. Specifically,

   \[
   \text{Minimum Refresh Time} = \frac{V_{FS}/2}{2^N \times \text{Droop Rate}}
   \]

   where \( V_{FS} \) = DAC full scale voltage and
   \( N \) = DAC resolution in bits.

   Constantly refreshing a demultiplexed DAC puts a software burden on the system. In particular, notice that the refresh time is halved for each additional bit of resolution. For example, if the DAC resolution is increased from 8-bits to 12-bits the
DACs must be refreshed 16 times more often. Software burden vs. hardware savings tradeoffs must be evaluated carefully in high resolution systems.

2. **Faster data update rates are possible.** In addition to requiring constant refresh, the rate at which the multiplexed DAC can be updated is limited by the sequential architecture of the system. Thus, the acquisition time of the SHA is multiplied by the number of channels. For the circuit of Figure 6.27, the best-case time for updating all 16 DAC values, assuming a 7µs SHA acquisition time, will be:

$$t_s = 16 \cdot 7\mu s = 112\mu s$$

Multiple DACs, on the other hand, can usually be treated as memory or input/output locations, and updated at or near the maximum cycle time of the microcontroller. Consecutive DACs can be loaded with data while previously-loaded DACs are settling to their final values. Since the digital transfer rate is usually faster than the settling time of the DAC, the multiple-DAC system update rate is much faster than the demultiplexed DAC rate.

3. **Multiple DACs can offer synchronized outputs.** Servo, ATE, and other systems can benefit from multiple outputs which change simultaneously. Many multiple DACs, such as the quad 8-bit AD7225 and octal 12-bit AD7568, are double-buffered. Data can be loaded into storage latches sequentially, then transferred simultaneously to the DAC latches when a separate “load” pin is brought low. For higher throughput, new data can be loaded into the storage latches as soon as the “load” pin returns high. In this case, the new data is loaded during the settling time of the DACs, so the throughput rate is maximized.

4. **Multiple DACs usually have a power-on reset feature.** Many systems must assume a known state upon power-up. For example, a programmable power supply should not output random voltages when turned on. Several DACs, such as the quad 12-bit DAC8412/DAC8413 and octal 8-bit DAC8800, provide a reset feature which sets all of the DACs to a known state. In most cases, the DAC output is reset to zero. The DAC8412, however, will reset to mid-scale. This feature provides a zero-volt output at reset when the DAC is configured for a bipolar output.

5. **Some multiple DACs’ registers feature data readback.** On some multiple DACs, the data bus is actually bi-directional, and the value written into the DAC register can also be read back by the controller. This feature provides the opportunity for hardware and software error checking. Since the DAC values do not have to be saved by the controller, additional data storage is also available for minimum-memory microcomputer applications.

6. **To save real estate and parts count, some multiple DACs use serial data interfaces.** Only two or three pins are required, at both the controller and the DAC, to transfer data. Creating a serial data interface for a demultiplexed-DAC system requires several additional packages to decode the serial address, even if a serial-input DAC is specified. Dramatic reductions in pin count can be obtained when a multiple DAC with serial input is specified. For example, the DAC8420 provides four, 12-bit voltage output DACs in one 16-pin package.
A serial data interface is inherently slower than a parallel interface. While this is usually a problem only in high speed systems, the slower serial data rate does exacerbate the demultiplexed-DAC’s refresh requirements.

A two chip solution to the data distribution challenge is shown in Figure 6.30. The AD8600 is a multiple-channel DAC which combines 32 registers, 16 DACs, 16 voltage output buffers, control logic, and an address decoder in a single 44-pin package.

![A 16-CHANNEL 8-BIT DATA DISTRIBUTION SYSTEM USING A 16-CHANNEL DAC](image)

Interfacing to the AD8600 is easy. The DACs are simply treated as 16 memory or I/O locations. Updating the value of any DAC is merely a matter of writing the DAC value, via an 8-bit data bus, to the appropriate address. If desired, data can be written into the input registers without affecting the DAC values. When the LOAD input is pulled low, all DAC outputs will change simultaneously. Holding LOAD low causes the output of each DAC to change as soon as the WRITE command occurs.

This 16-channel, single chip DAC reduces parts count by 66% over the demultiplexed DAC solution. Inventory and assembly costs, printed circuit board area, and design time are all reduced. Refreshing the DAC values is not required, so software overhead is eliminated.

When evaluated solely on the cost of components, the demultiplexed single DAC approach is about 40% less expensive than the multiple DAC. On a system cost basis, however, the advantages of the multiple DAC make it the cost as well as the performance winner. A comparison of the two approaches is shown in Figure 6.31. The cost advantages of the DAC8300 solution include:
COMPARING REPRESENTATIVE 16-CHANNEL, 8-BIT DATA DISTRIBUTION SYSTEMS

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>SINGLE DEMULTIPLEXED DAC</th>
<th>MULTIPLE DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Time</td>
<td>Moderate</td>
<td>Low</td>
</tr>
<tr>
<td>Refresh Required</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Refresh Ripple at Output</td>
<td>Dependent on Refresh Rate</td>
<td>None</td>
</tr>
<tr>
<td>Synchronized Outputs</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Time Required to Change All 16 DACs</td>
<td>112 µs</td>
<td>3.3 µs</td>
</tr>
<tr>
<td>Power-On Reset</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Read-Back Capability</td>
<td>No</td>
<td>Yes (Available on some)</td>
</tr>
<tr>
<td>Serial Data Interface</td>
<td>Additional Components</td>
<td>Yes, on Some DACs</td>
</tr>
<tr>
<td>Parts Count</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PC Board Holes (Total Number of Pins)</td>
<td>74</td>
<td>52</td>
</tr>
</tbody>
</table>

**Figure 6.31**

1. **Reduced design time.** All of the DAC system specifications are defined in the multiple DAC data sheet. The demultiplexed DAC, on the other hand, requires analysis of the DC and AC parameters of both the DAC and SHA, as well as the relationship between these parameters. (For example, must the DAC settling time be added to the SHA acquisition time, or, since the DAC settling time is only 2µs compared to 7µs for the SHA, can the DAC settling time be ignored? Updating each channel in 7µs instead of 9µs reduces refresh overhead by about 20%, but this is only valid if system specifications are met. Clearly, prototype evaluation is required).

2. **Parts count is reduced by 66%**. As previously mentioned, costs for purchasing, inventory and assembly are reduced.

3. **The number of PC board holes (that is, the pin count) is reduced.** The number of holes that are required in the PC board is another measure of assembly cost. On this basis, the multiple DAC wins by about 30%.

4. **No refresh is required.** This fact eliminates the software required to provide timing for the demultiplexed DAC, and may also free up the use of a timer on the microcontroller.

Although the cost savings listed above are significant, the multiple DAC’s improvements to system performance are even more important in most applications. The system improvements include:

1. **Reduced output ripple.** The demultiplexed DAC output will always have ripple, caused by the droop rate of the SHA.

2. **Faster update rate.** The delay time imposed by the SHA acquisition time is eliminated, so the AD8600 circuit can load new DAC values in as little as 80ns. To update 16 DACs, including an 80ns load pulse to change all DAC outputs simultaneously, and allowing 2µs for DAC settling, requires:
\[ t_s = (16 + 1) \cdot 80 \text{ns} + 2 \mu\text{s} = 3.3 \mu\text{s}. \]

The demultiplexed DAC, as was shown previously, is limited by the fact that the acquisition time of the SHA is multiplied by the sequential architecture of the system. The multiple DAC has reduced the refresh time from 112µs to only 3.3µs. In applications such as automatic test equipment, the effects of a 3300% improvement in test value update time are significant. The demultiplexed DAC circuit can be improved somewhat by specifying faster SHAs, but the increased droop rate of a faster SHA will demand that refresh be performed even more frequently. The increased refresh may offset the speed advantage of the faster SHA.

3. *Simultaneous DAC output changes.* With double-buffered data latches, each of the DAC values can be loaded sequentially, but the outputs will change simultaneously. If desired, of course, any of the DACs can be updated individually.

4. *A DAC reset input.* At system power up, or during power fault recovery, setting the reset input to a logic low will force all DAC registers into the zero state. This will asynchronously place zero-volts on all of the DAC outputs.

5. *Data readback.* The DAC has a bi-directional data bus, so that the value written into the DAC register can also be read back by the controller. This feature provides the opportunity for hardware and software error checking and can be especially useful during system debugging. Since the DAC values do not have to be saved in memory by the controller, an additional 16 bytes of data storage is also available for minimum-memory microcomputer applications.

Multiple DACs are offered in a wide variety of configurations, resolution, digital interface, and analog output. For example, dual, quad, and octal versions of both 8-bit and 12-bit devices are available. Serial data interfaces are also available, for reduced pin count. A 1994 selection guide (Reference 5) from Analog Devices contains 12 multiple DAC products which have a serial data interface.

Many multiple DACs are used in automatic calibration or system nulling applications. A typical device for these tasks is the AD8842, an octal 8-bit TrimDAC® (Figure 6.32). This device includes a serial data input for DAC data and address, eight DAC registers, and eight voltage-output DACs.
This device introduces a capability which is impossible with a demultiplexed DAC: the ability to have different reference voltages for each DAC channel. The output voltage of each channel of the AD8842 is simply:

$$V_{OUT} = V_{IN} \cdot \left( \frac{D}{128} - 1 \right)$$

where D is a representation of the DAC input value (that is, 0 to 255 for an 8-bit DAC). The value of $V_{IN}$ can be either positive or negative, DC or AC, allowing each DAC a 4-quadrant multiplying capability. Since $V_{IN}$ can be an AC signal, the DACs can also be used as a programmable gain control for signals up to 50kHz. $V_{IN}$, the analog input, exhibits a fixed input resistance of about 20kohms, so driving it, either from a DC voltage reference or from an AC source, is easy.

The AD8842 is an example of the reduction in pin count which is possible when a serial data interface is used. It combines 8 voltage output DACs, under 3-wire serial interface and an asynchronous preset input, into a single 24-pin DIP or SOIC package. To update any DAC, the DAC output value and address are shifted into the serial input register. A logic LOW on the LD input then transfers the data to the appropriate DAC register. The last bit of the serial input shift register is also available on the serial data output, so that multiple AD8842s can be daisy-chained without additional logic. Although the digital data can be loaded at an 8MHz rate, each DAC output requires 5.4µs to settle to ±1 LSB.

Other key features of the AD8842 are shown in Figure 6.33. The preset (PR) input can be used to force the outputs of all the DACs to 0V when power is first applied, or after a power fault. Placing a logic low on PR will force a value of 128 base10 (80
base16) into all of the DAC registers. As can be seen from the output voltage equation shown in Figure 6.32, a DAC value of 128 base 10 produces a 0V output.

**AD8842 KEY FEATURES**

- Eight Individual Channels
- 3-Wire Serial Data Input, 8MHz Loading Rate
- Asynchronous Reset Input
- 50kHz, 4-Quadrant Multiplexing Bandwidth
- Replaces 8 Potentiometers
- Constant 20kΩ Input Resistance
- ±4V Output Swing
- Low Power: 95mW on ±5V Supplies
- 24-pin Narrow DIP or SO Package

*Figure 6.33*

The AD8842 TrimDAC® can also replace 8 potentiometers in voltage nulling applications. Unlike a trimming potentiometer, however, the TrimDAC® can generate both positive and negative voltages from a positive reference voltage. This is a significant advantage in many applications, because the nulling voltage can be derived from a very stable system reference voltage. Obtaining a bipolar nulling voltage with a potentiometer normally requires either providing two separate positive and negative reference voltages, or connecting one end of the pot to the negative power supply. Since power supplies are typically noisy and poorly regulated when compared to the system reference voltage, performance will be degraded if the power supply must be used.

The effect of a serial interface on pin count becomes even more evident as the DAC resolution increases. For example, the AD8522 squeezes two 12-bit DACs, a 2.5V reference, a double-buffered serial input, and two reset control inputs into a single 14-pin package (Figure 6.34). A companion part, the AD8582, has similar features but requires 24 pins because it has a parallel interface.
The AD8522’s 2.5V reference is available on the VREF pin to provide a reference for other data acquisition portions of the system or for ratiometric applications. The reference output can also be used to create a virtual ground for applications where a quasi-bipolar output is desired. The VREF pin cannot, however, be used as a reference input.

As with the AD8842 octal DAC, both AD8522 DAC registers can be asynchronously forced to a half-scale value (2048 base 10 or 800 base 16). This action sets a 0V reading for quasi-bipolar applications. Both registers of the AD8522 can also be reset to a "000" value, which provides a 0V reset for unipolar applications. Other key features of the AD8522 are shown in Figure 6.35.

**AD8522 KEY FEATURES**

- Space-Saving SOIC-14 Package, only 1.5mm Height!
- Low Power: 10mW max
- No External Components, No Adjustments Necessary
- +5V Operation Guaranteed Down to 4.5V Minimum
- 4.095V Full Scale (1mV/LSB), Fully Trimmed
- Buffered Rail-to-Rail Voltage Outputs
- 2.5 V VREF Output Pin - Useful for establishing virtual ground in bipolar applications
- Midscale or Zero-Scale Present
- Double-Buffered 3-Wire Serial Data Input
- Software and Hardware A/B DAC Select
The AD8522 introduces two new concepts to the multi-channel data distribution discussion. The first new concept is the complete DAC (Figure 6.36). All of the systems mentioned previously have required a separate external reference, which had to be adjusted to set the DAC's full scale output voltage. The AD8522, on the other hand, has an on-chip bandgap reference which is laser-trimmed during production to provide a full scale output voltage of 4.095V (that is, 1mV/LSB). Since the voltage reference, DAC, and voltage output amplifiers are on a single chip, the entire DAC system specification is contained in the AD8522's data sheet specifications. This eliminates the necessity of evaluating several separate devices, as well as calculating the error contributions of each device, and further demonstrates the significant reduction in design time which results from reducing package count. In addition, system cost is reduced and reliability is improved because the calibration operation is eliminated.

**EQUIVALENT SCHEMATIC OF AD8522 ANALOG SECTION**

![Equivalent Schematic of AD8522 Analog Section](image)

Figure 6.36

The other concept which has not been discussed previously is low-voltage, single supply operation. It is at this point that demultiplexed DAC systems rapidly become impractical. One effect of a low supply voltage is that the value of the least significant bit must be reduced. For single +5V operation, the practical limit on full scale voltage at 12-bits is typically 4.096V. This yields an LSB value of 1mV for a 12-bit DAC, which means that the total SHA error budget, including offset voltage, droop rate and hold step, must not exceed ±500µV in order to limit errors to 1/2 LSB.

Improving the droop rate and hold step errors of a multi-channel SHA is difficult because of the limited size of the on-chip capacitors. As the value of the hold capacitors increase, die size and cost rise rapidly. Adding individual SHAs with external hold capacitors is possible, but rapidly increases the component count. Again, the multi-channel DAC is a superior solution.

Another requirement for single-supply, low voltage operation is rail-to-rail operation. Single-supply bipolar amplifiers, using common-emitter output stages, are limited in some low voltage applications because the saturation voltage of the output transistors limits output voltage swing. The AD8522 employs P-channel and
N-channel MOSFETs (Figure 6.37) to provide wide output voltage swing while operating from a single +5 V supply. The output of this type of stage (at a supply rail) looks like the on-resistance of the P or N-channel FET connected to the rail. Obviously, this on-resistance begins to limit the output swing as the output load current is increased.

**AD8522 RAIL-TO-RAIL OUTPUT PERFORMANCE
YIELDS 5mA WITH 60mA SHORT CIRCUIT CURRENT**

![Figure 6.37](image)

The effect of a serial interface on pin count is demonstrated by comparing the AD8522 with the similar AD8582. The latter part has a 12-bit parallel interface, and requires 24 pins versus 14 pins for the serial data version.

**AD8582 COMPLETE DUAL 12-BIT SINGLE +5V SUPPLY DAC**

![Figure 6.38](image)

One significant advantage of the parallel interface is, of course, higher speed. The parallel device can update both 12-bit DACs in 100ns. The serial data version, on the other hand, requires 32 clock cycles to enter the data for two DACs. With a maximum clock frequency of 14MHz, this results in a data update period of 2.2μs.
The parallel-data version also includes complete dual-rank data latches, so that both DACs can be updated simultaneously (Figure 6.39).

**AD8582 KEY FEATURES**

- Complete Dual 12-bit DAC
- No External Components
- Single +5 Operation
- 1mV/bit with 4.095V Full Scale
- True Voltage Output, ±5mA Drive
- Parallel Input Register with Fast 30ns Chip Select
- Double-Buffered for Simultaneous A and B Output Update
- Reset Pin Forces Output to Zero Volts or half Scale, Depending on MSB Pin
- Low Power: 5mW

Figure 6.39

The logical extension of a serial data interface and low voltage CMOS technology is expressed in Figure 6.40. While not a multi-channel device, the AD8300 does pack a complete 12-bit voltage output DAC into a single 8-pin package. No external components are required, except for supply bypass capacitors. Since it is capable of operating from a single 3V supply, this device is ideal for battery-powered applications.

**A 12-BIT, +3V DAC SYSTEM BASED ON AD8300**

Figure 6.40
The AD8300 has only one analog pin, which is the DAC's voltage output. With only one analog pin, the AD8300 is an ideal device for designers whose experience is mainly digital. All analog circuitry, except for the analog voltage output pin, is transparent to the user. Double-buffered data latches prevent the DAC output from changing while new data is being shifted into the AD8300.

**Figure 6.41**

The AD8300 is laser-trimmed during production, so no calibration or other adjustments are required. The DAC value is simply shifted into the serial data input, and the analog output responds with a pre-trimmed value of:

\[ V_{OUT} = D \cdot 0.5mV, \]

where D is a decimal number which represents the DAC input value (that is, 0 to 4095). The full-scale output voltage is 2.0475V, which is appropriate for the minimum supply voltage of 2.7V. The DAC output can be asynchronously set to 0V with the CLR input, if a power-on reset is required.
KEY FEATURES OF THE AD8300 DAC

- Complete Voltage Output 12-bit DAC
- Single +3V Operation
- No External Components
- 2.0475V Full Scale Output (0.5mV/bit)
- 6μs Output Settling Time
- Serial Data Input
- Asynchronous Clear Input
- Low Power; 3.6mW
- PCMCIA-Compatible SO-8 Package (1.5mm package height)

Figure 6.42

The data distribution systems discussed so far have illustrated the tradeoffs between demultiplexing a single DAC and using a single chip, multiple-channel DAC. Both of these concepts assume that the system being designed requires several analog voltages in close physical proximity to each other. The design considerations change, however, for systems where different circuit elements are not physically close. Analog signal traces should be kept as short as possible to reduce error sources such as leakage and noise pickup. Digital signals have more noise immunity than analog signals, so the rule of thumb is to locate the DAC as close to its associated analog circuitry as possible.

A complete DAC with serial input can utilize its small size to place the analog voltages near the circuits they control with minimal impact on overall PC board area. Two AD8300s, for example, have a total of only 16 pins. This is only two pins more than the previously-discussed dual-12-bit DAC, yet the two single DACs can be located directly adjacent to subsequent circuits (Figure 6.43). This eliminates long PC board traces (for the analog signal) and reduces noise pickup. Multiple AD8300s can be accessed with one serial data bus, and the outputs of the DACs can change either synchronously or asynchronously.
REMOTE, MULTI-CHANNEL DATA DISTRIBUTION

Figure 6.43
REFERENCES


SECTION 7

OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

- Amplifier Input Stage Overvoltage
- Amplifier Output Voltage Phase Reversal
- Understanding and Protecting Integrated Circuits from Electrostatic Discharge (ESD)
SECTION 7

OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

Adolfo Garcia, Wes Freeman

One of the most commonly asked applications questions is: “What happens if external voltages are applied to an analog integrated circuit with the supplies turned off?” This question describes situations that can take on many different forms: from lightning strikes on cables which propagate very high transient voltages into signal conditioning circuits, to walking across a carpet and then touching a printed circuit board full of sensitive precision circuits. Regardless of the situation, the general issue is the effect of overvoltage stress (and, in some cases, abuse) on analog integrated circuits. The discussion which follows will be limited in general to operational amplifiers, because it is these devices that most often interface to the outside world. The principles developed here can and should be applied to all analog integrated circuits which are required to condition or digitize analog waveforms. These devices include (but are not limited to) instrumentation amplifiers, analog comparators, sample-and-hold amplifiers, analog switches and multiplexers, and analog-to-digital converters.

AMPLIFIER INPUT STAGE OVERVOLTAGE

In real world signal conditioning, sensors are often used in hostile environments where faults can and do occur. When these faults take place, signal conditioning circuitry can be exposed to large voltages which exceed the power supplies. The likelihood for damage is quite high, even though the components’ power supplies may be turned on. Published specifications for operational amplifier absolute maximum ratings state that applied input signal levels should never exceed the power supplies by more than 0.3V or, in some devices, 0.7V. Exceeding these levels exposes amplifier input stages to potentially destructive fault currents which flow through internal metal traces and parasitic p-n junctions to the supplies. Without some type of current limiting, unprotected input differential pairs (BJTs or FETs) can be destroyed in a matter of microseconds. There are, however, some devices with built-in circuitry that can provide protection beyond the supply voltages, but in general, absolute maximum ratings must still be observed.
INPUT STAGE OVERVOLTAGE

■ INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS
  (Usually Specified With Respect to Supply Voltages)

■ A Common Specification Requires the Input Signal $|V_s| \leq 0.3V$

■ Input Voltage Should be Held Near Zero in the Absence of Supplies

■ Input Stage Conduction Current Needs to be Limited (Rule of Thumb: $\leq 5mA$)

■ Avoid Reverse Bias Junction Breakdown in Input Stage Base-Emitter Junctions

■ Differential and Common-Mode Ratings may Differ

■ No Two Amplifiers are exactly the Same

■ Some Op Amps Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still be Observed

Figure 7.1

Although more recent vintage operational amplifiers designed for single-supply or rail-to-rail operation are now including information with regard to input stage overvoltage effects, there are very many amplifiers available today without such information provided by the manufacturer. In those cases, the circuit designer using these components must ascertain the input stage current-voltage characteristic of the device in question before steps can be taken to protect it. All amplifiers will conduct current to the positive/negative supply, provided the applied input voltage exceeds some internal threshold. This threshold is device dependent, and can range from 0.7V to 30V, depending on the internal construction of the input stage. Regardless of the threshold level, externally generated fault currents should be limited to no more than $\pm 5mA$.

Many factors contribute to the current-voltage characteristic of an amplifier's input stage: internal differential clamping diodes, current-limiting series resistances, substrate potential connections, and differential input stage topologies (BJTs or FETs). Input protection diodes used as differential input clamps are typically constructed from the base-emitter junctions of NPN transistors. These diodes usually form a parasitic p-n-junction to the negative supply when the applied input voltage exceeds the negative supply. Current-limiting series resistances used in the input stages of operational amplifiers can be fabricated from three types of material: n- or p-type diffusions, polysilicon, or thin-films (SiCr, for example). Polysilicon and thin-film resistors are fabricated over thin layers of oxide which provide an insulating barrier to the substrate; as such, they do not exhibit any parasitic p-n junctions to either supply. Diffused resistors, on the other hand, exhibit p-n
junctions to the supplies because they are constructed from either p- or n-type diffusion regions. The substrate potential of the amplifier is the most critical component, for it will determine the sensitivity of an amplifier's input current-voltage characteristic to supply voltage.

The configuration of the amplifier's input stage also plays a large role in the current-voltage characteristic of the amplifier. Input differential pairs of operational amplifiers are constructed from either bipolar transistors (NPN or PNP) or field-effect transistors (junction or MOS, N- or P-channel). While the bipolar input differential pairs do not have any direct path to either supply, FET differential pairs do. For example, an n-channel JFET forms a parasitic p-n junction between its backgate and the p-substrate that energizes when $V_{IN} + 0.7V < V_{NEG}$. As mentioned previously, many manufacturers of analog integrated circuits do not provide any details with regard to the behavior of the device's input structure. Either simplified schematics are not provided or, if they are shown, the behavior of the input stage under an overvoltage condition is omitted. Therefore, other measures must be taken in order to identify the conduction paths.

A standard transistor curve tracer can be configured to determine the current-voltage characteristic of any amplifier regardless of input circuit topology. As shown in Figure 7.2, both amplifier supply pins are connected to ground, and the collector output drive is connected to one of the amplifier's inputs. The curve tracer applies a DC ramp voltage and measures the current flowing through the input stage. In the event that a transistor curve tracer is not available, a DC voltage source and a multimeter can be substituted for the curve tracer. A 10kohm resistor should be used between the DC voltage source and the amplifier input for additional protection. Ammeter readings from the multimeter at each applied DC voltage will yield the same result as that produced by the curve tracer. Although either input can be tested (both inputs should), it is recommended that the unused input is left open; otherwise, additional junctions could come into play and would complicate matters further. Evaluations of current feedback amplifier input stages are more difficult because of the lack of symmetry between the inputs. As a result, both inputs should be characterized for their individual current-voltage characteristics.
Once the input current-voltage characteristic has been determined for the device in question, the next step is to determine the minimum level of resistance required to limit fault currents to ±5mA. Equation 7.1 illustrates the computation for $R_S$ when the input overvoltage level is known:

$$R_S = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5 \text{ mA}} \quad \text{Eq. 7.1}$$

The worst case condition for overvoltage would be when the power supplies are initially turned off or disconnected. In this case, $V_{SUPPLY}$ is equal to zero. For example, if the input overvoltage could reach 100V under some type of fault condition, then the external resistor should be no smaller than 20kohms. Most operational amplifier applications only require protection at one input; however, there are a few configurations (difference amplifiers, for example) where both inputs can be subjected to overvoltage and both must be protected. The need for protection on both inputs is much more common with instrumentation amplifiers.
OVERVOLTAGE EFFECTS

- Junctions may be **Forward Biased** if the Current is Limited
- In General a Safe Current Limit is 5mA
- **Reverse Bias** Junction Breakdown is Damaging Regardless of the Current Level
- When in Doubt, Protect with External Diodes and Series Resistances
- Curve Tracers Can be Used to Check the Overvoltage Characteristics of a Device
- Simplified Equivalent Circuits in Data Sheets do not tell the Entire Story!!!

Figure 7.3

AMPLIFIER OUTPUT VOLTAGE PHASE REVERSAL

Some operational amplifiers exhibit output voltage phase reversal when one or both of their inputs exceeds their input common-mode voltage range. Phase reversal is usually associated with JFET (n- or p-channel) input amplifiers, but some bipolar devices (especially single-supply amplifiers operating as unity-gain followers) may also be susceptible. In the vast majority of applications, output voltage phase reversal does not harm the amplifier nor the circuit in which the amplifier is used. Although a number of operational amplifiers suffer from phase reversal, it is rarely a problem in system design. However, in servo loop applications, this effect can be quite hazardous. Fortunately, this is only a temporary condition. Once the amplifier’s inputs return to within its normal operating common-mode range, output voltage phase reversal ceases. It may still be necessary to consult the amplifier manufacturer, since phase reversal information rarely appears on device data sheets. Summarized as follows is a list of recent vintage Analog Devices amplifier products that are now including output voltage phase reversal characterization/commentary:

<table>
<thead>
<tr>
<th>Single-Supply/Rail-to-Rail</th>
<th>Dual Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP295/OP495</td>
<td>OP282/OP482</td>
</tr>
<tr>
<td>OP113/OP213/OP413</td>
<td>OP285</td>
</tr>
<tr>
<td>OP183/OP283</td>
<td>OP467</td>
</tr>
<tr>
<td>OP292/OP492</td>
<td>OP176</td>
</tr>
<tr>
<td>OP191/OP291/OP491</td>
<td>BUF04</td>
</tr>
<tr>
<td>OP279</td>
<td></td>
</tr>
<tr>
<td>AD820/AD822/AD824</td>
<td></td>
</tr>
<tr>
<td>OP193/OP293/OP493</td>
<td></td>
</tr>
</tbody>
</table>
In BiFET operational amplifiers, phase reversal may be prevented by adding an appropriate resistance in series with the amplifier’s input to limit the current. Bipolar input devices can be protected by using a Schottky diode to clamp the input to within a few hundred millivolts of the negative rail. For a complete description of the output voltage phase reversal effect, please consult Reference 1.

**BEWARE OF AMPLIFIER OUTPUT PHASE REVERSAL**

- Sometimes Occurs in FET and Bipolar Input (Especially Single-Supply) Op Amps when Input Exceeds Common Mode Range
- Does Not Harm Amplifier, but may be Disastrous in Servo Systems!
- Not Usually Specified on Data Sheet, so Amplifier Must be Checked
- Easily Prevented:
  
  **BiFETs:**
  
  Add Appropriate Input Series Resistance (Determined Empirically, Unless Provided in Data Sheet)
  
  **Bipolars:**
  
  Use Schottky Diode Clamps to the Supply Rails.

Figure 7.4

Rail-to-rail operational amplifiers present a special class of problems to the integrated circuit designer, because these types of devices should not exhibit any abnormal behavior throughout the entire input common-mode range. In fact, it is desirable that devices used in these applications also not exhibit any abnormal behavior if the applied input voltages exceed the power supply range. One of the more recent vintage rail-to-rail input/output operational amplifiers, the OPX91 family (the OP191, the OP291, and the OP491), includes additional components that prevent overvoltage and damage to the device. As shown in Figure 7.5, the input stage of the OPX91 devices use six diodes and two resistors to clamp the input terminals to each other and to the supplies. D1 and D2 are base-emitter NPN diodes which are used to protect the bases of Q1-Q2 and Q3-Q4 against avalanche breakdown when the applied differential input voltage to the device exceeds 0.7V. Diodes D3-D6 are diodes formed from substrate PNP transistors that clamp the applied input voltages on the OPX91 to the supply rails.
A CLOSER LOOK AT THE OP-X91 INPUT STAGE REVEALS ADDITIONAL DEVICES

Figure 7.5

An interesting benefit from using substrate PNP s as clamp diodes is that their collectors are connected to the negative supply; thus, when the applied input voltage exceeds either supply rail, the diodes energize, and the fault currents are diverted directly to the supply and not through or into the device’s input stage. There are also 5kohm resistors in series with each of the inputs to the OPX91 to limit the fault current through D1 and D2 when the differential input voltage exceeds 0.7V. Note that these 5kohm resistors are p-type diffusions placed inside an n-well, which is then connected to the positive supply. When the applied input voltage exceeds the positive supply, some of the fault current generated is also diverted to VPOS and away from the input stage. As a result of these measures, the input overvoltage characteristic of the OPX91 is well behaved as shown in Figure 7.6. Note that the combination of the 5kohm resistors and clamp diodes safely limits the input current to less than 2mA, even when the inputs of the device exceed the supply rails by 10V.
As an added safety feature, an additional pair of diodes is used in the input stage across Q3 and Q4 to prevent subsequent stages internal to the OPX91 from collapsing (that is, forced into cutoff). If these stages were forced into cutoff, then the amplifier would undergo output voltage phase reversal when the inputs exceeded the positive input common mode voltage. An illustration of the diodes’ effectiveness is shown in Figure 7.7. Here, the OPX91 family can safely handle a 20Vp-p input signal on ±5V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. With these amplifiers, no external clamping diodes are required.
For those amplifiers where external protection is clearly required against both overvoltage abuse and output phase reversal, a common technique is to use a series resistance, $R_s$, to limit fault current, and Schottky diodes to clamp the input signal to the supplies, as shown in Figure 7.8.
Figure 7.8

The external input series resistance, \( R_S \), will be provided by the manufacturer of the amplifier, or determined empirically by the user with the method previously shown in Figure 7.2 and Eq. 7.1. More often than not, the value of this resistor will provide enough protection against output voltage phase reversal, as well as limiting the fault current through the Schottky diodes.

It is evident that whenever resistance is added in series with an amplifier's input, its offset and noise performance will be affected. The effects of this series resistance on circuit noise can be calculated using the following equation.

\[
E_{n,\text{total}} = \sqrt{\left(e_{n,\text{op amp}}\right)^2 + \left(e_{n,R_S}\right)^2 + \left(R_S \cdot i_{n,\text{op amp}}\right)^2}
\]

The thermal noise of the resistor, the voltage noise due to amplifier noise current flowing through the resistor, and the input noise voltage of the amplifier are added together (in root-sum-square manner, since the noise voltages are uncorrelated) to determine the total input noise and may be compared with the input voltage noise in the absence of the protection resistor.

A protection resistor in series with an amplifier input will also produce a voltage drop due to the amplifier bias current flowing through it. This drop appears as an increase in the circuit offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal, a resistor in series with each input will tend to balance the effect and reduce the error. The effects of this additional series resistance on the circuit's overall offset voltage can be calculated:
\[ V_{os(\text{total})} = V_{os} + I_b R_s \]

For the case where \( R_{FB} = R_s \) or where the source impedance levels are balanced, then the total circuit offset voltage can be expressed as:

\[ V_{os(\text{total})} = V_{os} + I_{os} R_s \]

To limit the additional noise of \( R_{FB} \), it can be shunted with a capacitor.

When using external clamp diodes to protect operational amplifier inputs, the effects of diode junction capacitance and leakage current should be evaluated in the application. Diode junction capacitance and \( R_s \) will add an additional pole in the signal path, and diode leakage currents will double for every 10\(^\circ\)C rise in ambient temperature. Therefore, low leakage diodes should be used such that, at the highest ambient temperature for the application, the total diode leakage current is less than one-tenth of the input bias current for the device at that temperature. Another issue with regard to the use of Schottky diodes is the change in their forward voltage drop as a function of temperature. These diodes do not, in fact, limit the signal to ±0.3V at all ambient temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is true if over-voltage is only possible at turn-on, when the diodes and the op amp will always be at the same temperature. If the op amp is warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature.

**UNDERSTANDING AND PROTECTING INTEGRATED CIRCUITS FROM ELECTROSTATIC DISCHARGE (ESD)**

_Wes Freeman_

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures which protect against ESD damage also increase input leakage.

The keys to eliminating ESD damage are: (1) awareness of the sources of ESD voltages, and (2) understanding the simple handling steps that will discharge potential voltages safely.

The basic definitions relating to ESD are given in Figure 7.9. Notice that the _ESD Failure Threshold_ level relates to any of the IC data sheet limits, and not simply to a _catastrophic failure_ of the device. Also, the limits apply to each pin of the IC, not just to the input and output pins.
ESD DEFINITIONS

- ESD (Electrostatic Discharge):
  - A single fast, high current transfer of electrostatic charge.
    - Direct contact between two objects at different potentials.
    - A high electrostatic field between two objects when they are close in proximity.

- ESD Failure Threshold:
  - The highest voltage level at which all pins on a device can be subjected to ESD zaps without failing any 25°C data sheet limits

Figure 7.9

The generation of static electricity caused by rubbing two substances together is called the triboelectric effect. Static charge can be generated either by dissimilar materials (for example, rubber-soled shoes moving across a rug) or by separating similar materials (for example, pulling transparent tape off of a roll).

A wide variety of common human activities can create high electrostatic charge. Some examples are given in Figure 7.10. The values shown will occur with a fairly high relative humidity. Low humidity, such as can occur indoors during cold weather, can generate voltages 10 times (or more) greater than the values shown.
EXAMPLES OF ELECTROSTATIC CHARGE GENERATION

- Person walks across a typical carpet.
  - 1000-1500V generated

- Person walks across a typical vinyl floor.
  - 150 - 250V generated

- Person handles instructions protected by clear plastic covers.
  - 400 - 600V generated

- Person handles polyethylene bags.
  - 1000 - 1200V generated

- Person pours polyurethane foam into a box.
  - 1200 - 1500V generated

- An IC slides down a grounded handler chute.
  - 50 - 500V generated

- An IC slides down an open conductive shipping tube.
  - 25 - 250V generated

Note:
Above values can occur in a high (≈60%) RH environment. For low RH (≈30%), generated voltages can be >10 times those listed above!

Figure 7.10

In an effort to standardize the testing and classification of integrated circuits for ESD robustness, ESD models have been developed (Figure 7.11). These models attempt to simulate the source of ESD voltage. The assumptions underlying the three commonly-used models are different, so results are not directly comparable.

MODELING ELECTRONIC POTENTIAL

- Three Models:
  1. Human Body Model (HBM)
  2. Machine Model (MM)
  3. Charged Device Model (CDM)

- Model Correlation:
  - Low - Assumptions are Different

Figure 7.11

The most-often encountered ESD model is the Human Body Model (HBM). This model simulates the approximate resistance and capacitance of a human body with a simple RC network. The capacitor is charged through a high voltage power supply (HVPS) and then discharged (using a high voltage switch) through a series resistor.
The RC values for different individuals will, of course, vary. However, the HBM has been standardized by MIL-STD-883 Method 3015 Electrostatic Discharge Sensitivity Classification, which specifies R-C combinations of 1.5kohm and 100pF. (R, C, and L values for all three ESD models are shown in Figure 7.12.)

ESD MODELS APPLICABLE TO ICs

- **Human Body Model (HBM)**
  
  Simulates the discharge event that occurs when a person charged to either a positive or negative potential touches an IC at different potential.

  \[
  \text{RLC: } R = 1.5k\Omega, \quad L = 0n\text{H}, \quad C = 100p\text{F}
  \]

- **Machine Model (MM)**
  
  Non-real-world Japanese model based on worst-case HBM.

  \[
  \text{RLC: } R = 0\Omega, \quad L = 500n\text{H}, \quad C = 200p\text{F}
  \]

- **Charged Device Model (CDM)**
  
  Simulates the discharge that occurs when a pin on an IC, charged to either a positive or negative potential, contacts a conductive surface at a different (usually ground) potential.

  \[
  \text{RLC: } R = 1\Omega, \quad L = 0n\text{H}, \quad C = 1 - 20p\text{F}
  \]

Figure 7.12

The Machine Model (MM) is a worst-case Human Body Model. Rather than using an average value for resistance and capacitance of the human body, the MM assumes a worst-case value of 200pF and 0ohms. The 0ohm output resistance of the MM is also intended to simulate the discharge from a charged conductive object (for example, a charged DUT socket on an automatic test system) to an IC pin, which is how the Machine Model earned its name. However, the MM does not simulate many known real-world ESD events. Rather, it models the ESD event resulting from an ideal voltage source (in other words, with no resistance in the discharge path). EIAJ Specification ED-4701 Test Method C-111 Condition A and ESD Association Specification S5.2 provide guidelines for MM testing.

The Charged Device Model (CDM) originated at AT&T. This model differs from the HBM and the MM, in that the source of the ESD energy is the IC itself. The CDM assumes that the integrated circuit die, bond wires, and lead frame are charged to some potential (usually positive with respect to ground). One or more of the IC pins then contacts ground, and the stored charge rapidly discharges through the leadframe and bond wires. Typical examples of triboelectric charging followed by a CDM discharge include:
1. An IC slides down a handler chute and then a corner pin contacts a grounded stop bar.

2. An IC slides down an open conductive shipping tube and then a corner pin contacts a conductive surface.

The basic concept of the CDM is different than the HBM and MM in two ways. First, the CDM simulates a charged IC discharging to ground, while the HBM and MM both simulate a charged source discharging into the IC. Thus, current flows out of the IC during CDM testing, and into the IC during HBM and MM testing. The second difference is that the capacitor in the CDM is the capacitance of the package, while the HBM and MM use a fixed external capacitor.

Unlike the HBM and MM, CDM ESD thresholds may vary for the same die in different packages. This occurs because the device under test (DUT) capacitance is a function of the package. For example, the capacitance of an 8-pin package is different than the capacitance of a 14-pin package. CDM capacitance values can vary from about 1 to 20pF. The device capacitance is discharged through a 1ohm resistor.

Schematic representations of the three models are shown in Figure 7.13. Notice that C1 in the HBM and MM are external capacitors, while CPKG in the CDM is the internal capacitance of the DUT.

The HBM discharge waveform is a predictable unipolar RC pulse, while the MM discharge shows ringing because of the parasitic inductance in the discharge path (typically 500nH). Ideally, the CDM waveform is also a single unipolar pulse, but the parasitic inductance in series with the 1ohm resistor slows the rise time and introduces some ringing.

---

**SCHEMATIC REPRESENTATION OF ESD MODELS AND TYPICAL DISCHARGE WAVEFORMS**

![Schematic Diagram](image)

**Figure 7.13**
The significant features of each ESD model are summarized in Figure 7.14. The peak currents shown for each model are based on a test voltage of 400V. Peak current is lowest for the HBM because of the relatively high discharge resistance. The CDM discharge has low energy because device capacitance is only in the range of 1pF to 20pF, but peak current is high. The MM has the highest energy discharge, because it has the highest capacitance value (Power = 0.5 CV^2).

**COMPARISON OF HBM, MM, AND CDM ESD MODELS**

<table>
<thead>
<tr>
<th>MODEL</th>
<th>HBM</th>
<th>MM</th>
<th>SOCKETED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulate</td>
<td>Human Body</td>
<td>Machine</td>
<td>Charged Device</td>
</tr>
<tr>
<td>Real World?</td>
<td>Yes</td>
<td>Generally</td>
<td>No</td>
</tr>
<tr>
<td>RCD</td>
<td>1.5kΩ, 100pF</td>
<td>20, 200pF</td>
<td>10, 100pF</td>
</tr>
<tr>
<td>Rise Time</td>
<td>&lt;10ns (8-20ns typ)</td>
<td>14ns**</td>
<td>430ns**</td>
</tr>
<tr>
<td>Ipeak at 400V</td>
<td>0.37A</td>
<td>5.8A*</td>
<td>2.1A**</td>
</tr>
<tr>
<td>Energy</td>
<td>Moderate</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Package</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Figure 7.14 compares 400V discharge waveforms of the CDM, MM, and HBM, with the same current and time scales.

---

*These values per ESD Association Std. 5.2.
**EIAJ Std. ED-4701 Method C-111 includes no waveform specifications.
These values are for the direct charging (socketed) method.
The CDM waveform corresponds to the shortest known real-world ESD event. The waveform has a rise time of <1ns, with the total duration of the CDM event only about 2ns. The CDM waveform is essentially unipolar, although some ringing occurs at the end of the pulse that results in small negative-going peaks. The very short duration of the overall CDM event results in an overall discharge of relatively low energy, but peak current is high.

The MM waveform consists of both positive- and negative-going sinusoidal peaks, with a resonance frequency of 10MHz to 15MHz. The initial MM peak has a typical rise time of 14ns, and the total pulse duration is about 150ns. The multiple high current, moderate duration peaks of the MM result in an overall discharge energy that is by far the highest of the three models for a given test voltage.

The risetime for the unipolar HBM waveform is typically 6-9ns, and the waveform decays exponentially towards 0V with a fall time of approximately 150ns. (Method 3015 requires a rise time of <10ns and a delay time of 150ns ± 20ns, with decay time defined as the time for the waveform to drop from 100% to 36.8% of peak current). The peak current for the HBM is 400V/1500ohms, or 0.267A, which is much lower than is produced by 400V CDM and MM events. However, the relatively long duration of the total HBM event still results in an overall discharge of moderately high energy.

As previously noted, the MM waveform is bipolar while HBM and CDM waveforms are primarily unipolar. However, HBM and CDM testing is done with both positive and negative polarity pulses. Thus all three models stress the IC in both directions.
MIL-STD-883 Method 3015 classifies ICs for ESD failure threshold. The classification limits, shown in Figure 7.16, are derived using the HBM shown in Figure 7.13. Method 3015 also mandates a marking method to denote the ESD classification. All military grade Class 1 and 2 devices have their packages marked with one or two “Delta” symbols, respectively, while class 3 devices (with a failure threshold >4kV) do not have any ESD marking. Commercial and industrial grade IC packages may not be marked with any ESD classification symbol.

### CLASSIFYING AND MARKING ICs FOR ESD PER MIL-883C, METHOD 3015

<table>
<thead>
<tr>
<th>HBM ESD CLASS</th>
<th>FAILURE THRESHOLD</th>
<th>MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>&lt;2kV</td>
<td>Δ</td>
</tr>
<tr>
<td>2</td>
<td>2kV - &lt;4kV</td>
<td>Δ Δ</td>
</tr>
<tr>
<td>3</td>
<td>&gt;4kV</td>
<td>None</td>
</tr>
</tbody>
</table>

Note: Commercial and Industrial Grade ICs are not marked for ESD

Figure 7.16

Notice that the Class 1 limit includes all devices which do not pass a 2kV threshold. However, a Class 1 rating does not imply that all devices within that class will pass 1,999V. In any event, the emphasis must be placed on eliminating ESD exposure, not on attempting to decide how much ESD exposure is ‘safe.’

A detailed discussion of IC failure mechanisms is beyond the scope of this seminar, but some typical ESD effects are shown in Figure 7.17.

### UNDERSTANDING ESD DAMAGE

- **ESD Failure Mechanisms:**
  - Dielectric or junction damage
  - Surface charge accumulation
  - Conductor fusing.

- **ESD Damage Can Cause:**
  - Increased leakage
  - Reduced performance
  - Functional failures of ICs.

- **ESD Damage is often Cumulative:**
  - For example, each ESD “zap” may increase junction damage until, finally, the device fails.

Figure 7.17
For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is prevention. There is no way to undo ESD damage, or to compensate for its effects.

THE MOST IMPORTANT THING TO REMEMBER ABOUT ESD DAMAGE

- ESD DAMAGE CANNOT BE “CURED”!
- Circuits cannot be tweaked, nulled, adjusted, etc., to compensate for ESD damage.

ESD DAMAGE MUST BE PREVENTED!

Figure 7.18

Since ESD damage can not be undone, the only cure is prevention. Luckily, prevention is a simple two-step process. The first step is recognizing ESD-sensitive products, and the second step is understanding how to handle these products.

PREVENTING ESD DAMAGE TO ICs

Two key elements in protecting circuits from ESD damage are:

- Recognizing ESD-sensitive products
- Always handling ESD-sensitive products at a grounded workstation.

Figure 7.19

All static sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or in antistatic tubes. Either way, the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as is shown in Figure 7.20, which outlines the appropriate handling procedures.
Once ESD-sensitive devices are identified, protection is easy. Obviously, keeping ICs in their original protective packaging as long as possible is the first step. The second step is to discharge potential ESD sources before damage to the IC can occur. The HBM capacitance is only 100pF, so discharging a potentially dangerous voltage can be done quickly and safely through a high impedance. Even with a source resistance of 10Megohms, the 100pF will be discharged in less than 100milliseconds.

The key component required for safe ESD handling is a workbench with a static-dissipative surface, as shown in Figure 7.21. This surface is connected to ground through a 1Megohm resistor, which dissipates static charge while protecting the user from electrical shock hazards caused by ground faults. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with a discharge resistor.
Notice that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, the CDM assumes that a high peak current will flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the surface shown in Figure 7.21, however, the peak current is not high enough to damage the device.

A conductive wrist strap is also recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape off of packages, will not cause damage to ICs. Again, a 1Megohm resistor, from the wrist strap to ground, is required for safety.

When building prototype breadboards or assembling PC boards which contain ESD-sensitive devices, all passive components should be inserted and soldered before the ICs. This procedure minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy (Figure 7.22)
ANALOG DEVICES’ COMMITMENT

- Analog Devices is committed to helping our customers prevent ESD damage by:
  - Building products with the highest level of ESD protection commensurate with performance requirements
  - Protecting products from ESD during shipment
  - Helping customers to avoid ESD exposure during manufacture

Figure 7.22

A complete ESD protection plan, however, requires more than building-ESD protection into ICs. Users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures (Figure 7.23).

ESD PROTECTION REQUIRES A PARTNERSHIP BETWEEN THE IC SUPPLIER AND THE CUSTOMER

ANALOG DEVICES:

- Circuit Design and Fabrication -
  ↓ Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.
- Pack and Ship -
  ↓ Pack in static dissipative material. Mark packages with ESD warning.

CUSTOMERS:

- Incoming Inspection -
  ↓ Inspect at grounded workstation. Minimize handling.
- Inventory Control -
  ↓ Store in original ESD-safe packaging. Minimize Handling.
- Manufacturing -
  ↓ Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.
- Pack and Ship -
  ↓ Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 7.23
The **ESD Protection Manual** is available from Analog Devices’ literature department. This manual provides additional information on static-dissipative work surfaces, packaging materials, protective clothing, ESD training, and other subjects.

**ESD PROTECTION MANUAL**

Contact Analog Devices’ literature department for a copy of the ESD Prevention Manual, which has further information on:

- Handling Instructions
- Packaging
- Static-Safe Facilities
- Other ESD Issues

Figure 7.24
REFERENCES


SECTION 8

DISTORTION MEASUREMENTS

■ High Speed Op Amp Distortion
■ High Frequency Two-Tone Generation
■ Using Spectrum Analyzers in High Frequency Low Distortion Measurements
■ Measuring ADC Distortion using FFTs
■ FFT Testing
■ Troubleshooting the FFT Output
■ Analyzing the FFT Output
SECTION 8

DISTORTION MEASUREMENTS

HIGH SPEED OP AMP DISTORTION

Walt Kester

Dynamic range of an op amp may be defined in several ways. The most common ways are to specify Harmonic Distortion, Total Harmonic Distortion (THD), or Total Harmonic Distortion Plus Noise (THD + N).

Harmonic distortion is measured by applying a spectrally pure sinewave to an op amp in a defined circuit configuration and observing the output spectrum. The amount of distortion present in the output is usually a function of several parameters: the small- and large-signal nonlinearity of the amplifier being tested, the amplitude and frequency of the input signal, the load applied to the output of the amplifier, the amplifier’s power supply voltage, printed circuit board layout, grounding, power supply decoupling, etc. Therefore, any distortion specification is relatively meaningless unless the exact test conditions are specified.

Harmonic distortion may be measured by looking at the output spectrum on a spectrum analyzer and observing the values of the second, third, fourth, etc., harmonics with respect to the amplitude of the fundamental signal. The value is usually expressed as a ratio in %, ppm, dB, or dBC. For instance, 0.0015% distortion corresponds to 15ppm, or –96.5dBC. The unit "dBC" simply means that the harmonic’s level is so many dB below the value of the "carrier" frequency, i.e., the fundamental.

Harmonic distortion may be expressed individually for each component (usually only the second and third are specified), or they all may be combined in a root-sum-square (RSS) fashion to give the Total Harmonic Distortion (THD). The distortion component which makes up Total Harmonic Distortion is usually calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included. This is because the RSS process causes the higher-order terms to have negligible effect on the THD, if they are 3 to 5 times smaller than the largest harmonic. For example,

\[ \sqrt{0.10^2 + 0.03^2} = \sqrt{0.0109} = 0.104 \approx 0.1 \]
DEFINITIONS OF THD AND THD + N

- $V_s = \text{Signal Amplitude (rms Volts)}$
- $V_2 = \text{Second Harmonic Amplitude (rms Volts)}$
- $V_n = \text{n-th Harmonic Amplitude (rms Volts)}$
- $V_{\text{noise}} = \text{rms value of noise over measurement bandwidth}$

\[
\text{THD + N} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2 + V_{\text{noise}}^2}}{V_s}
\]

\[
\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_s}
\]

Figure 8.1

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In audio applications, the bandwidth is normally chosen to be around 100kHz. In narrow-band applications, the level of the noise may be reduced by filtering. On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range. It should be evident that the THD+N approximately equals THD if the rms noise over the measurement bandwidth is several times less than the THD, or even the worst harmonic. It is worth noting that if you know only the THD, you can calculate the THD+N fairly accurately using the amplifier's voltage- and current-noise specifications. (Thermal noise associated with the source resistance and the feedback network may also need to be computed). But if the rms noise level is significantly higher than the level of the harmonics, and you are only given the THD+N specification, you cannot compute the THD.

Special equipment is often used in audio applications for a more sensitive measurement of the noise and distortion. This is done by first using a bandstop filter to remove the fundamental signal (this is to prevent overdrive distortion in the measuring instrument). The total rms value of all the other frequency components (harmonics and noise) is then measured over an appropriate bandwidth. The ratio to the fundamental is the THD+N specification.

Audio frequency amplifiers (such as the OP-275) are optimized for low noise and low distortion within the audio bandwidth (20Hz to 20kHz). In audio applications, total harmonic distortion plus noise (THD+N) is usually measured with specialized equipment, such as the Audio Precision System One. The output signal amplitude is measured at a given frequency (e.g., 1kHz); then the fundamental signal is removed with a bandstop filter, and the system measures the rms value of the remaining frequency components, which contain both harmonics and noise. The noise and harmonics are measured over a bandwidth that will include the highest harmonics,
usually about 100kHz. The measurement is swept over the frequency range for various conditions.

THD+N results for the OP-275 are plotted in Figure 8.2 as a function of frequency. The signal level is 3V rms, and the amplifier is connected as a unity-gain follower. The data is shown for three load conditions: 600ohm, 2kohm, and 10kohm. Notice that a THD+N value of 0.0008% corresponds to 8ppm, or –102dBc. The input voltage noise of the OP-275 is typically 6nV/rtHz @ 1kHz, and integrated over an 80kHz noise bandwidth, yields an rms noise level of 1.7µV rms. For a 3V rms signal level, the corresponding signal-to-noise ratio is 125dB. Because the THD is considerably greater than the noise level, the THD component is the primary contributor. Multiple plots with variable bandwidths can be used to help separate noise and distortion.

**THD + N FOR THE OP -275 OVER 100kHz BANDWIDTH IS DOMINATED BY DISTORTION**

![THD + N plot](image)

*Figure 8.2*

Now, consider the AD797, a low noise amplifier (1nV/rtHz) where measurement equipment distortion, and not the amplifier distortion, limits the measurement. The THD specification for the AD797 is 120dBc @ 20kHz, and a plot is shown in Figure 8.3. The distortion is at the limits of measurement of available equipment, and the actual amplifier noise is even lower by 20dB. The measurement was made with a spectrum analyzer by first filtering out the fundamental sinewave frequency ahead of the analyzer. This is to prevent overdrive distortion in the spectrum analyzer. The first five harmonics were then measured and combined in an RSS fashion to get the THD figure. The legend on the graph indicates that the measurement equipment "floor" is about 120dBc; hence at frequencies below 10kHz, the THD may be even less.
THD OF THE AD797 OP AMP SHOWS MEASUREMENT LIMIT AT -120dBc, WHILE AMPLIFIER NOISE FLOOR IS AT -140dBc (1nV/\sqrt{Hz} INTEGRATED OVER 100kHz BANDWIDTH)

Figure 8.3

To calculate the AD797 noise, multiply the voltage noise spectral density (1nV/\sqrt{Hz}) by the square root of the measurement bandwidth to yield the device’s rms noise floor. For a 100kHz bandwidth, the noise floor is 316nV rms, corresponding to a signal-to-noise ratio of about 140dB for a 3V rms output signal.

Rather than simply examining the THD produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones. As shown in Figure 8.4, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies, \( f_1 \) and \( f_2 \), to a nonlinear device. The second order products located at \( f_2 + f_1 \) and \( f_2 - f_1 \) are located far away from the two tones, and may be removed by filtering. The third order products located at \( 2f_1 + f_2 \) and \( 2f_2 + f_1 \) may likewise be filtered. The third order products located at \( 2f_1 - f_2 \) and \( 2f_2 - f_1 \), however, are close to the original tones, and filtering them is difficult. Third order IMD products are especially troublesome in multi-channel communications systems where the channel separation is constant across the frequency band.
Intermodulation distortion products are of special interest in the RF area, and a major concern in the design of radio receivers. Third-order IMD products can mask out small signals in the presence of larger ones. Third order IMD is often specified in terms of the third order intercept point as shown in Figure 8.5. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. If the system non-linearity is approximated by a power series expansion, the second-order IMD amplitudes increase 2dB for every 1dB of signal increase. Similarly, the third-order IMD amplitudes increase 3dB for every 1dB of signal increase. With a low level two-tone input signal, and two data points, draw the second and third order IMD lines as are shown in Figure 8.5, because one point and a slope determine each straight line.

Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress. But the second and third-order intercept lines may be extended to intersect the extension of the output signal line. These intersections are called the second- and third order intercept points, respectively. The values are usually referenced to the output power of the device expressed in dBm. Another parameter which may be of interest is the 1dB compression point. This is the point at which the output signal is compressed by 1dB from the ideal input/output transfer function. This point is also shown in Figure 8.5.
Knowing the third order intercept point allows calculation of the approximate level of the third-order IMD products as a function of output signal level. Figure 8.6 shows the third order intercept value as a function of frequency for the AD9622 voltage feedback amplifier.
Assume the op amp output signal is 5MHz and 2V peak-to-peak into a 100ohm load (50ohm source and load termination). The voltage into the 50ohm load is therefore 1V peak-to-peak, corresponding to +4dBm. The value of the third order intercept at 5MHz is 36dBm. The difference between +36dBm and +4dBm is 32dB. This value is then multiplied by 2 to yield 64dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be –64dBc (dB below carrier frequency), or at a level of –60dBm. Figure 8.7 shows the graphical analysis for this example.
USING THE THIRD ORDER INTERCEPT POINT TO CALCULATE IMD PRODUCT FOR THE AD9622 OP AMP

Figure 8.7

HIGH FREQUENCY TWO-TONE GENERATION

Generating test signals with the spectral purity required to make low distortion high frequency measurements is a challenging task. A test setup for generating a single tone is shown in Figure 8.8. The sinewave oscillator should have low phase noise (e.g., Marconi 2382), especially if the device under test is an ADC, where phase noise increases the ADC noise floor. The output of the oscillator is passed through a bandpass (or lowpass) filter which removes any harmonics present in the oscillator output. The distortion should be 6dB lower than the desired accuracy of the measurement. The 6dB attenuator isolates the DUT from the output of the filter. The impedance at each interface should be maintained at 50ohms for best performance (75ohm components can be used, but 50ohm attenuators and filters are generally more readily available). The termination resistor, RT, is selected so that the parallel combination of RT and the input impedance of the DUT is 50ohms.

LOW DISTORTION SINGLE-TONE GENERATOR

Figure 8.8
Before performing the actual distortion measurement, the oscillator output should be set to the correct frequency and amplitude. Measure the distortion at the output of the attenuator with the DUT replaced by a 50ohm termination resistor (generally the 50ohm input of a spectrum analyzer. Next, replace the 50ohm load with \( R_T \) and the DUT. Measure the distortion at the DUT input a second time. This allows non-linear DUT loads to be identified. Non-linear DUT loads (such as flash ADCs with signal-dependent input capacitance, or switched-capacitor CMOS ADCs) can introduce distortion at the DUT input.

Generating two tones suitable for IMD measurements is even more difficult. A low-distortion two-tone generator is shown in Figure 8.9. Two bandpass (or lowpass) filters are required as shown. Harmonic suppression of each filter must be better than the desired measurement accuracy by at least 6dB. A 6dB attenuator at the output of each filter serves to isolate the filter outputs from each other and prevent possible cross-modulation. The outputs of the attenuators are combined in a passive 50ohm combining network, and the combiner drives the DUT. The oscillator outputs are set to the required level, and the IMD of the final output of the combiner is measured. The measurement should be made with a single termination resistor, and again with the DUT connected to identify non-linear loads.

**LOW DISTORTION TOW TONE GENERATOR**

![Diagram of a low distortion two-tone generator.](image)

**Figure 8.9**

**USING SPECTRUM ANALYZERS IN HIGH FREQUENCY LOW DISTORTION MEASUREMENTS**

Analog spectrum analyzers are most often used to measure amplifier distortion. Most have 50ohm inputs, therefore an isolation resistor between the device under test (DUT) and the analyzer is required to simulate DUT loads greater than 50ohms. After adjusting the spectrum analyzer for bandwidth, sweep rate, and sensitivity, check it carefully for input overdrive. The simplest method is to use the variable attenuator to introduce 10dB of attenuation in the analyzer input path. Both the signal and any harmonics should be attenuated by a fixed amount (10dB, for instance) as observed on the screen of the spectrum analyzer. If the harmonics are attenuated by more than 10dB, then the input amplifier of the analyzer is introducing distortion, and the sensitivity should be reduced. Many analyzers have a
button on the front panel for introducing a known amount of attenuation when checking for overdrive.

**MEASURING AMPLIFIER DISTORTION REQUIRES CARE TO PREVENT ANALYZER OVERDRIVE**

![Diagram](image)

**Figure 8.10**

Another method to minimize sensitivity to overdrive is shown in Figure 8.11. The amplitude of the fundamental signal is first measured with the notch filter switched out. The harmonics are measured with the notch filter switched in. The insertion loss of the notch filter, $X_{dB}$, must be added to the measured level of the harmonics.
NOTCH FILTER REMOVES THE FUNDAMENTAL SIGNAL TO MINIMIZE ANALYZER OVERDRIVE

Figure 8.11

MEASURING ADC DISTORTION USING FFTS

The speed of personal computers and the availability of suitable software now makes DSP bench testing of high speed ADCs relatively easy. A block diagram of a typical DSP PC-based test system is shown in Figure 8.12. In order to perform any DSP testing, the first requirement is a high speed buffer memory of sufficient width and depth. High speed logic analyzers make a convenient memory and eliminate the need for designing special hardware. The HP1663A is a 100MHz logic analyzer which has a simple IEEE-488 output port for easy interfacing to a personal computer. The analyzer can be configured as either a 16-bit wide by 8k deep, or a 32-bit wide by 4k deep memory. This is more than sufficient to test a high speed ADC at sample rates up to 100MHz. For higher sample rates, faster logic analyzers are available, but are fairly costly. An alternative to using a high speed logic analyzer is to operate the ADC at the desired sample rate, but only clock the final output register at an even sub-multiple of the sample clock frequency. This is sometimes called decimation and is useful for relaxing memory requirements. If an FFT is performed on the decimated output data, the fundamental input signal and its associated harmonics will be present, but translated in frequency. Simple algorithms can be used to find the locations of the signal and its harmonics provided the original signal frequency is known.
A SIMPLE PC-BASED TEST SYSTEM

Figure 8.12

**FFT TESTING**

Easy to use mathematical software packages, such as Mathcad™ (available from MathSoft, Inc., 201 Broadway, Cambridge MA, 02139) are available to perform fast FFTs on most 486-based PCs. The use of a co-processor allows a 4096-point FFT to run in a few seconds on a 75MHz,486 PC. The entire system will run under the Windows environment and provide graphical displays of the FFT output spectrum. It can be programmed to perform SNR, S/(N+D), THD, IMD, and SFDR computations. A simple QuickBasic program transfers the data stored in the logic analyzer into a file in the PC via the IEEE-488 port (Reference 3, Section 16).

Properly understanding of FFT fundamentals is necessary in order to achieve meaningful results. The first step is to determine the number of samples, M, in the FFT record length. In order for the FFT to run properly, M must be a power of 2. The value of M determines the frequency *bin width*, Delta f = f_s/M. The larger M, the more frequency resolution. Figure 8.13 shows the relationship between the average noise floor of the FFT with respect to the broadband quantization noise level. Each time M is doubled, the average noise in the Delta f bandwidth decreases by 3dB. Larger values of M also tend to give more repeatable results from run to run (see Figure 8.13).
M values of 512 (for 8-bit ADCs), 2048 (for 10-bit ADCs), and 4096 (for 12-bit ADCs) have proven to give good accuracy and repeatability. For extremely wide dynamic range applications (such as spectral analysis) $M=8192$ may be desirable. It should be noted that averaging the results of several FFTs will tend to smooth out the noise floor, but will not change the average value of the floor.

In order to obtain spectrally pure results, the FFT data window must contain an exact integral number of sinewave cycles as shown in Figure 8.14. These frequency ratios must be precisely observed to prevent end-point discontinuity. In addition, it is desirable that the number of sinewave cycles contained within the data window be a prime number. This method of FFT testing is referred to as coherent testing because two locked frequency synthesizers are used to insure the proper ratio (coherence) between the sampling clock and the sinewave frequency. The requirements for coherent sampling are summarized in Figure 8.15.
FFT OF SINEWAVE HAVING INTEGRAL NUMBER OF CYCLES IN WINDOW

Figure 8.14

REQUIREMENTS FOR COHERENT SAMPLING

- \( f_s \) = Sampling Rate
- \( f_{in} \) = Input Sinewave Frequency
- \( M \) = Number of Samples in Record (Integer Power of 2)
- \( M_c \) = Prime Integer Number of Cycles of Sinewave During Record (Makes All Samples Unique)
- Make \( f_{in} / f_s = M_c / M \)

Figure 8.15

Making the number of cycles within the record a prime number ensures a unique set of sample points within the data window. An even number of cycles within the record length will cause the quantization noise energy to be concentrated in the harmonics of the fundamental (causing a decrease in SFDR) rather than being randomly distributed over the Nyquist bandwidth. Figure 8.16 shows a 4096-point FFT output for a theoretically perfect 12-bit sinewave. The spectrum on the left was made with exactly 128 samples within the record length, corresponding to a frequency which is 1/32 times \( f_s \). The SFDR is 78dB. The spectrum on the right was made with exactly 127 samples within the record, and the SFDR increases to 92dB.
Coherent FFT testing ensures that the fundamental signal occupies one discrete line in the output spectrum. Any leakage or smearing into adjacent bins is the result of aperture jitter, phase jitter on the sampling clock, or other unwanted noise due to improper layout, grounding, or decoupling.

If the ratio between the sampling clock and the sinewave frequency is such that there is an endpoint discontinuity in the data (shown in Figure 8.17), then spectral leakage will occur. The discontinuities are equivalent to multiplying the sinewave by a rectangular windowing pulse which has a $\sin(x)/x$ frequency response. The discontinuities in the time domain result in leakage or smearing in the frequency domain, because many spectral terms are needed to fit the discontinuity. Because of the endpoint discontinuity, the FFT spectral response shows the main lobe of the sinewave being smeared, and a large number of associated sidelobes which have the basic characteristics of the rectangular time pulse. This leakage must be minimized using a technique called windowing (or weighting) in order to obtain usable results in non-coherent tests.
This situation is exactly what occurs in real-world spectral analysis applications where the exact frequencies being sampled are unknown and uncontrollable. Sidelobe leakage is reduced by choosing a windowing (or weighting) function other than the rectangular window. The input time samples are multiplied by an appropriate windowing function which brings the signal to zero at the edges of the window. The selection of an appropriate windowing function is primarily a tradeoff between main-lobe spreading and sidelobe rolloff.

The time-domain and frequency-domain characteristics of a simple windowing function (the Hanning Window) are shown in Figure 8.18. A comparison of the frequency response of the Hanning window and the more sophisticated Minimum 4-Term Blackman-Harris window is given in Figures 8.19 and 8.20. For general ADC testing with non-coherent input frequencies, the Hanning window will give satisfactory results. For critical spectral analysis or two-tone IMD testing, the Minimum 4-Term Blackman-Harris window is the better choice because of the increase in spectral resolution.
TIME AND FREQUENCY REPRESENTATION OF THE HANNING WINDOW

\[ W_n = 0.5 \cdot 0.5 \cos \frac{2\pi n}{M} \]

\[ \Delta t = \frac{1}{f_s} \]

\[ T = M \Delta t \]

Figure 8.18

FREQUENCY RESPONSE OF THE HANNING WINDOW

\[ W_n = 0.5 \cdot 0.5 \cos \frac{2\pi n}{M} \]

HANNING WINDOW, \( M = 1024 \)

Figure 8.19
The addition of a windowing function to the FFT software involves first calculating the proper coefficient for each time sample within the record. These values are then stored in a memory file. Each time sample is multiplied by its appropriate weighting coefficient before performing the actual FFT. The software routine is easy to implement in QuickBasic.

When analyzing the FFT output resulting from windowing the input data samples, care must be exercised in determining the energy in the fundamental signal and the energy in the various spurious components. For example, sidelobe energy from the fundamental signal should not be included in the rms noise measurement. Consider the case of the Hanning Window function being used to test a 12-bit ADC with a theoretical SNR of 74dB. The sidelobe attenuation of the Hanning Window is as follows:

<table>
<thead>
<tr>
<th>Bins From Fundamental</th>
<th>Sidelobe Attenuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>32dB</td>
</tr>
<tr>
<td>5.0</td>
<td>50dB</td>
</tr>
<tr>
<td>10.0</td>
<td>68dB</td>
</tr>
<tr>
<td>20.0</td>
<td>86dB</td>
</tr>
</tbody>
</table>

Therefore, in calculating the rms value of the fundamental signal, you should include at least 20 samples on either side of the fundamental as well as the fundamental itself.

If other weighting functions are used, their particular sidelobe characteristics must be known in order to accurately calculate signal and noise levels.
A typical Mathcad™ FFT output plot is shown in Figure 8.21 for the AD9022 12-bit, 20MSPS ADC using the Hanning Window and a record length of 4096.

![MATHCAD™ 4096 POINT FFT OUTPUTS FOR AD9022 12-BIT, 20 MSPS ADC (HANNING WEIGHTING)](image)

**Figure 8.21**

The actual QuickBasic routine for transferring the HP analyzer’s data to a DOS file in the PC as well as the Mathcad™ routine are given in Reference 3, Section 16.

**TROUBLESHOOTING THE FFT OUTPUT**

Erroneous results are often obtained the first time an FFT test setup is put together. The most common error is improper timing of the latch strobe to the buffer memory. The HP1663A logic analyzer accepts parallel data and a clock signal. It has an internal DAC which may be used to examine a record of time samples. Large glitches on the stored waveform probably indicate that the timing of the latch strobe with respect to the data should be changed.

After ensuring correct timing, the FFT routine should produce a reasonable spectral output. If there are large values of harmonics, the input signal may be overdriving the ADC at one or both ends of the range. After bringing the signal within the ADC range (usually about 1dB below fullscale), excess harmonic content becomes more difficult to isolate.

Make sure that the sinewave input to the ADC is spectrally pure. Bandpass filters are usually required to clean up the output of most high frequency oscillators, especially if wide dynamic range is expected.

After ensuring the spectral purity of the ADC input, make sure the data output lines are not coupling to either the sampling clock or to the ADC analog input. Remember that the glitches produced on the digital lines are signal-dependent and will therefore contribute to harmonic distortion if they couple into either one of these two lines. As has been discussed previously, noise or digital modulation on the sampling clock can also produce harmonic distortion in the FFT output. The use of an evaluation board with separate sampling clock and analog input connectors will usually prevent this. The special ribbon cable used with the logic analyzer to capture
the ADC output data has a controlled impedance and should not cause performance degradation.

In addition to the above hardware checks, the FFT software should be verified by applying a theoretically perfect quantized sinewave to the FFT and comparing the results to theoretical SNR, etc. This is easy to do using the "roundoff" function available in most math packages. The effects of windowing non-coherent inputs should also be examined before running actual ADC tests.

In performing calculations with the FFT output, the term at dc and $f_s/2$ should be omitted from any calculations, as they can produce erroneous results. Input frequencies which are integer submultiples of the sampling clock can also produce artificially large harmonics.

**TROUBLESHOOTING THE FFT OUTPUT**

- **Excess harmonic distortion:**
  - Distortion on input signal
  - Signal outside ADC input range
  - Digital runs coupling into analog input or sampling clock
  - Poor layout, decoupling, and grounding
  - Buffer memory not clocked at correct time
  - Analog input frequency locked to integer submultiple of sampling clock

- **Excess noise floor:**
  - Noise or phase jitter on input signal
  - Noise or phase jitter on sampling clock
  - Poor layout, decoupling, and grounding
  - Eliminate dc and $f_s/2$ FFT components from calculations

**Figure 8.22**

**ANALYZING THE FFT OUTPUT**

Once the FFT output is obtained, it can be analyzed in a number of ways, similar to that of the display on an analog spectrum analyzer. The spurious free dynamic range (SFDR) is the ratio of the fundamental signal to the worst frequency spur. Total harmonic distortion (THD) is obtained by taking the ratio of the signal to the rms value of the first several harmonics (and then taking the logarithm of the ratio). Because of aliasing, however, locating the harmonics in the frequency spectrum can be difficult. For instance, if a 3MHz signal is sampled at 10MSPS, the second harmonic (6MHz) actually appears in the FFT output at 4MHz (10MHz – 6MHz). The third harmonic (9MHz) appears at 1MHz (10MHz – 9MHz). The fourth harmonic (12MHz) appears at 2MHz (12MHz – 10MHz). Software routines to perform these calculations are easily written.
Two tone intermodulation distortion can be measured by applying two spectrally pure tones to the ADC using the circuit previously shown in Figure 8.9. The concept of second- or third-order intercept point has little meaning when testing ADCs for two reasons. First, the ADC acts as a hard limiter for out-of-range signals, while an amplifier soft limits. Second, as the amplitude of the tones is reduced, the value of the signal-related frequency spurs tends to become somewhat constant because of the discontinuous nature of the ADC transfer function. A "hard distortion" floor is reached beyond which further reduction in signal amplitude has little effect on the spur levels.

Finally, signal-to-noise plus distortion (S/N+D) can be calculated by taking the ratio of the rms signal amplitude to the rms value of all other spectral components (excluding dc and f_s/2). From the S/N+D value, the effective number of bits (ENOB) can be calculated. In some applications, the value of S/N+D without the harmonics included is of interest.

Because of the statistical nature of the FFT analysis, there will be some variability in the output from run to run under identical test conditions. The data can be stabilized by averaging the results of several FFT runs. This will not lower the average noise floor of the FFT, but will reduce the variation in the results.

**ANALYZING THE FFT OUTPUT**

- Single-to-Noise including Distortion: S/(N+D)
- Effective Number of Bits: (ENOB)
- Signal-to-Noise without distortion: SNR
- Spurious Free Dynamic Range: SFDR
- Harmonic Distortion
- Total Harmonic Distortion: THD
- THD + Noise (Same as S/N + D)
- Two-Tone Intermodulation Distortion

*Figure 8.23*
REFERENCES


SECTION 9

HARDWARE DESIGN TECHNIQUES

- Prototyping Analog Circuits
- Evaluation Boards
- Noise Reduction and Filtering for Switching Power Supplies
- Low Dropout References and Regulators
- EMI/RFI Considerations
- Sensors and Cable Shielding
While there is no doubt that computer analysis is one of the most valuable tools that the analog designer has acquired in the last decade or so, there is equally no doubt that analog circuit models are not perfect and must be verified with hardware. If the initial test circuit or "breadboard" is not correctly constructed, it may suffer from malfunctions which are not the fault of the design but of the physical structure of the breadboard itself. This section considers the art of successful breadboarding of high performance analog circuits.

Real electronic circuits contain many "components" which were not present in the circuit diagram, but which are there because of the physical properties of conductors, circuit boards, IC packages, etc. These components are difficult, if not impossible, to incorporate into computer modeling software, and yet they have substantial effects on circuit performance at high resolutions, or high frequencies, or both.

It is therefore inadvisable to use SPICE modeling or similar software to predict the ultimate performance of such high performance analog circuits. After modeling is complete, the performance must be verified by experiment.

This is not to say that SPICE modeling is valueless - far from it. Most modern high performance analog circuits could never have been developed without the aid of SPICE and similar programs, but it must be remembered that such simulations are only as good as the models used, and these models are not perfect. We have seen the effects of parasitic components arising from the conductors, insulators and components on the PCB, but it is also necessary to appreciate that the models used within SPICE simulations are not perfect models.

Consider an operational amplifier. It contains some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the diffusions in the op-amp chip. This is the model that the designer will have used to evaluate the device during his design. In simulations, such a model will behave very like the actual op-amp, but not exactly.
**SPICE MODELING**

- SPICE modeling is a powerful tool for predicting the performance of analog circuits.
- Analog Devices provides macromodels for over 450 ICs

**HOWEVER**

- Models omit real-life effects
- No model can simulate all the parasitic effects of discrete components and a PCB layout

**THEREFORE**

- Prototypes must be built and proven before production.

Figure 9.1

However, this model is not published, as it contains too much information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing such models of a number of op-amps to reach a useful result. For these, and other reasons, the SPICE models of analog circuits published by manufacturers or software companies are "macro" models, which simulate the major features of the component, but lack some of the fine detail. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally.

The basic principle of a breadboard is that it is a temporary structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial breadboarding systems, but almost all of them are designed to facilitate the breadboarding of digital systems, where noise immunities are hundreds of millivolts or more. (We shall discuss the exception to this generality later.) Non copper-clad Matrix board (Vectorboard, etc.), wire-wrap, and plug-in breadboard systems (Bimboard, etc.) are, without exception, unsuitable for high performance or high frequency analog breadboarding. They have too high resistance, inductance, and capacitance. Even the use of standard IC sockets is inadvisable.

**PRACTICAL BREADBOARDING TECHNIQUES**

The most practical technique for analog breadboarding uses a copper-clad board as a ground plane. The ground pins of the components are soldered directly to the plane and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Ideally the layout should be similar to the layout to be used on the final PCB. This approach is often referred to as "deadbug" because the ICs are often mounted upside down with their
leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 9.2 shows a hand-wired breadboard based around two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120ohms, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not taken, however, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

"DEADBUG" PROTOTYPE TECHNIQUE

![Figure 9.2](image)

Pieces of copper-clad may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with connections through holes) with the board itself providing screening. In this case, the board will need legs to protect the components on the underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Robert A. Pease of National Semiconductor (Reference 1) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless the technique is very practical and widely used because the circuit may so easily be modified.
Another "deadbug" prototype is shown in Figure 9.3. The board is single-sided copper clad with holes pre-drilled on 0.1" centers. Power busses are at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board.

"DEADBUG" PROTOTYPE USING PRE-DRILLED SINGLE-SIDED COPPER-CLAD BOARD

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each hole used for a via must be drilled out so as to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

IC sockets can degrade the performance of high speed or high precision analog ICs. Even "low-profile" sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used, an IC socket made of individual "pin sockets" (sometimes called "cage jacks") mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively).
PIN SOCKETS (CAGE JACKS) HAVE MINIMUM PARASITIC RESISTANCE, INDUCTANCE AND CAPACITANCE

There is a commercial breadboarding system which has most of the advantages of "bird's nest over a ground plane, or deadbug" (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" [Reference 2].

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. They are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50ohms, 60ohms, 75ohms or 100ohms) when mounted on the ground plane, and a variety of pads for mounting various other components. A few of the many types of Solder-Mount building-block components are shown in Figure 9.5.
The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Figure 9.6 shows an example of a 2.5GHz phase-locked-loop prototype built with Solder-Mount. This is a high speed circuit, but the technique is equally suitable for the construction of high resolution low frequency analog circuitry. A particularly convenient feature of Solder-Mount at VHF is the ease with which it is possible to make a transmission line.
"SOLDER-MOUNT" PROTOTYPE

If a conductor runs over a ground plane it forms a microstrip transmission line. Solder-Mount has strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50ohms, 60ohms, 75ohms, and 100ohms). These strips may be used as transmission lines, for impedance matching, or simply as power buses. (Glass fiber/epoxy PCB is somewhat lossy at VHF and UHF, but the losses will probably be tolerable if microstrip runs are short.)

Both the "deadbug" and the "Solder-Mount" breadboarding techniques become tedious for complex circuits. Larger circuits are often better prototyped using more formal layout techniques.

An approach to prototyping more complex analog circuits is to actually lay out a double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections. Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their approximate position, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques (Reference 3) to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape (Reference 4). These systems produce single and double-sided circuit boards directly by drilling all holes and using a milling technique to remove copper and create insulation paths and finally, the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there
is no "plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils.

An example of such a prototype board is shown in Figure 9.7. This is a "daughter" board designed to interface an AD9562 Dual Pulse-Width Modulator in a 44-pin PLCC package to a "mother" board. The leads are on 50 mil centers, and the traces are approximately 25 mils wide.

"MILLED" PROTOTYPE PC BOARD

Figure 9.7

Multilayer PC boards do not easily lend themselves to standard prototyping techniques. One side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.
SUCCESSFUL PROTOTYPING

- Always use a ground plane for precision or high frequency circuits
- Minimize parasitic resistance, capacitance, and inductance
- If sockets are required, use “pin sockets” (“cage jacks”)
- Pay equal attention to signal routing, component placement, grounding, and decoupling in both the prototype and the final design

Popular prototyping techniques:
- Freehand “deadbug” using point-to-point wiring
- “Solder-Mount”
- Milled PC board from CAD layout
- Multilayer boards: Double-sided with additional point-to-point wiring

Figure 9.8

EVALUATION BOARDS

Manufacturer’s evaluation boards provide a convenient way of evaluating high-performance ICs without the need for constructing labor-intensive prototype boards. Analog Devices provides evaluation boards for almost all new high speed and precision products. The boards are designed with good layout, grounding, and decoupling techniques. They are completely tested, and artwork (including PG tape) is available to customers.

Because of the popularity of dual precision op amps in 8-pin DIPs, a universal evaluation board has been developed (see Figure 9.9). This board makes extensive use of pin sockets to allow resistors or jumpers to configure the two op amps in just about any conceivable feedback, input/output, and load condition. The inputs and outputs are convenient right-angle BNC connectors. Because of the use of sockets and the less-than-compact layout, this board is not useful for op amps having gain-bandwidth products much greater than 10MHz.
A schematic of the AD8001 800MHz 50mW current feedback op amp evaluation board for the 8-lead SOIC package is shown in Figure 9.10. The board is designed for a non-inverting gain of 2. (Boards for inverting and non-inverting modes are available for both the 8-lead SOIC and the DIP package).

Decoupling on both the + and – supplies consists of 1000pF and 0.01µF surface mount chip ceramic capacitors in addition to a 10µF/25V surface mount tantalum electrolytic. The top view of the PC board is shown in Figure 9.10, and the bottom view in Figure 9.12.
AD8001AR (SOIC) 800MHz OP AMP: NON-INVERTING MODE EVALUATION BOARD SCHEMATIC

Figure 9.10

AD8001AR (SOIC) EVALUATION BOARD - TOP VIEW

Figure 9.11
Figure 9.12 (bottom side of board) shows the surface mount resistors and capacitors. Notice that the ceramic chip capacitors are mounted as close as possible to the power pins as possible. The input and output runs are 50ohm transmission lines. The input from the SMA connector is terminated in a 50ohm chip resistor at the op amp, and the output has a 50ohm source termination for driving a 50ohm cable through the output SMA connector.

All resistors are surface mount film resistors. Notice that the ground plane is etched away from the area immediately surrounding the inputs of the op amp to minimize stray capacitance.

Slightly different resistor values are required to achieve optimum performance in the SOIC and the DIP packages (see Figure 9.13), because the SOIC package has slightly lower parasitic capacitance and inductance than the DIP. The criteria for selection of the components was maximum 0.1dB bandwidth.
ADC evaluation boards include more support circuitry than op amp boards. An example is the AD7714 (22-bit precision measurement sigma-delta ADC) evaluation board (see Figure 9.14 for a simplified block diagram). Included on the evaluation board are an AD780 precision reference, a 2.4576MHz crystal and digital buffers to buffer the signal to and from the edge connectors.

Interfacing to this board is provided either through a 36-Way Centronics connector or through a 9-Way D-type connector. The Centronics connector is intended for connection to the printer port of a PC. External sockets are provided for the analog inputs, an external reference input option, and an external master clock option.

Included in the evaluation board package is a PC-compatible DOS-based disk which contains software for controlling and evaluating the performance of the AD7714 using the printer port. There are two files on the disk, an executable file, and a "readme" text file which gives details of the functions available in the executable
program. The evaluation software is run by running the executable file. The program provides a number of different menu-type screens, each screen containing several function options.

The first menu gives options on the type of PC being used. The next menu in the sequence is the Main Menu which contains various options. These allow reading from the AD7714 Data Register, configuration of the Communications Register, file options (read and write data to files), noise analysis, printer port setup, and resetting the AD7714.

The Noise Menu allows the user to get statistical results from the data, to plot the raw data, plot a histogram of the data on the screen, or perform a rolling average of the data. A photograph of the AD7714 evaluation board is shown in Figure 9.15. Notice the parallel printer connector on the left and the use of low-profile sockets for convenience. It should be noted that although the use of sockets is discouraged, any sockets used on evaluation boards have been proven to cause minimal performance degradation.

AD7714 EVALUATION BOARD PHOTO

![AD7714 Evaluation Board](image)

Figure 9.15

Evaluation boards for high speed sampling ADCs contain the required support circuitry for proper evaluation of the converter. Figure 9.16 shows a block diagram of the AD9026 (12-bit, 31MSPS) evaluation board. The analog input is connected directly to the ADC input via an SMA connector. The sampling clock (Encode Input) is conditioned by the low-jitter high-speed AD9698 dual comparator. The parallel digital outputs of the AD9026 are buffered by latches which drive the output connector as well as the AD9713 12-bit DAC. The DAC output is connected to an output SMA connector.
The output connector is designed for convenient interfacing to an external buffer memory or to a logic analyzer input (a very convenient high speed buffer memory). The top side of the board is shown in Figure 9.17. The board is a 3-layer board consisting of one ground plane (outer layer), one power/signal plane (inner layer), and an additional signal plane (outer layer). Pin sockets are used to mount the AD9026. Figure 9.18 shows the bottom side of the board and the surface mounted AD9698 SOIC comparator and the AD9713B PLCC DAC.
Figure 9.18
REFERENCES: PROTOTYPING AND EVALUATION BOARDS


Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

3. Schematic Capture and Layout Software:

   PADS Software, INC, 165 Forest St., Marlboro, MA, 01752

   ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121

4. Prototype Board Cutters:

   LPKF CAD/CAM Systems, Inc., 1800 NW 169th Place, Beaverton, OR, 97006

   T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341
Noise Reduction and Filtering for Switching Power Supplies

Walt Jung and John McDonald

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. There are several good reasons for their popularity, including high efficiency, low temperature rise, small size, and light weight.

Switching power supplies, or more simply switchers, a category including switching regulators and switching converters, are by their nature efficient. Often this can be above 90%, and as a result, these power supply types use less power and generate less heat than do equivalent linear supplies.

A switcher can be as much as one third the size and weight of a linear supply delivering the same voltage and current. Switching frequencies can range from 20kHz to 1MHz, and as a result, relatively small components can be used in their design.

In spite of these benefits, switchers have their drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, and occurs as both conducted and radiated noise, and unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the voltage spikes will contain frequency components extending easily to 100MHz or more.

Because of wide variation in the noise output characteristics of commercial switchers, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the peak (or p-p) amplitudes of the switching spikes, with the output loading of your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in external filtering networks.
SWITCHING POWER SUPPLY CHARACTERISTICS

ADVANTAGES:
- Efficient
- Small Size, Light Weight
- Low Operating Temperature Rise
- Isolation from Line Transients
- Wide Input/Output Range

DISADVANTAGES:
- Noise: LF, HF, Electric Field, Magnetic Field Conducted, Radiated
- DC regulation and accuracy can be poor

Figure 9.19

This section discusses filter techniques for rendering a noisy switcher output analog ready, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. These techniques include characterization of switcher output noise, identification of the frequency range of interference produced by the switching power supply, evaluation of passive components commonly used in external power supply filters, and the design and construction of a switching power supply filter. The filter solutions presented are generally applicable to all power supply types incorporating a switch element in their energy path. This includes various DC-DC converters, as well as the 5V PC type supply used in the example.

A TYPICAL 5V, 150W PC SWITCHING POWER SUPPLY

Figure 9.20
A typical 5V PC type switcher is shown in Figure 9.20, and typifies the style. A display of the 5V power buss of an operating desktop PC (Dell Dimension XPS P-90) using a similar (but not identical) supply is shown in Figure 9.21. The unfiltered output shown from this switcher exhibits a ~60mV p-p transient component at an 80kHz (roughly) switching frequency, as seen in the (A) left photo with the 5µs time base. The expanded scale photo for the same operating conditions of (B) right shows the detail of the switching glitches on a 100ns time base. The fast voltage spikes produce significant harmonics well into the high MHz range.

**OUTPUT OF 5V PC SWITCHING POWER SUPPLY (UNFILTERED)**

![Output Photos](image)

**Figure 9.21**

It is clear that this switcher is not analog ready, just as it is shown. Since many analog ICs show degraded power supply rejection at frequencies above a few kHz, some filtering is necessary. This will be particularly true for use with low power op amps, which can show PSRR degradation above a few hundred Hz. In general, all op amps, voltage references, DACs, and ADCs require clean supplies to meet their design accuracy. Switcher noise can prevent this happening, if left unchecked.

Before offering techniques to reduce switcher noise, a brief examination of switching supply architectures is helpful, and two popular ones are shown in Figure 9.22. Higher efficiency designs use a pulse width modulation technique for voltage regulation, while lower efficiency, lower noise designs use linear post regulators.
BASIC SWITCHING POWER SUPPLY TOPOLOGY

Figure 9.22

The raw AC line voltage is first rectified and filtered to a high DC level, then converted to a 30kHz (or higher) frequency square wave, which drives a transformer. The signal is again rectified, and filtered at the transformer output. Some switchers may use a linear regulator to form the final output voltage, as in the upper diagram. Others use pulse width regulation techniques to control the duty cycle of the transformer drive (lower diagram). Although more efficient, this results in more noise at the output than linear post-regulation.

It is important to understand that noise is generated in every stage of the switcher. The first stage AC line rectification creates current spikes, which produce line-related harmonic noise. In the inverter stage, fast pulse edges generate harmonics extending well beyond 5MHz. Furthermore, the parasitic capacitance within the primary and secondary windings of the transformer provide an additional path through which high-frequency noise can corrupt the DC output voltage. Finally, high-frequency noise is also generated by both rectifier stages.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a source, a path, and a receptor [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. From this array of general noise immunity approaches, this section focuses on reducing switching power supply noise with external post filters.
Before designing a switching supply filter, it is helpful to determine whether or not the supply noise is actually affecting the circuit performance. If critical node voltages in the circuit have transients synchronous with the switcher’s operating frequency, then the supply is the likely culprit. A highly recommended method for determining if the supply is the noise source is to temporarily operate the circuit from a clean linear power supply or battery. If the interfering noise level drops dramatically, the switcher is guilty as charged. Note that lowering the power supply noise level may also help identify other noise sources which were masked by the higher switcher noise. Once the noise source is quantified and its path (radiated or conducted) identified, the process of reducing or eliminating it can begin.

Tools which can be used to combat switcher noise are highlighted by Figure 9.24. These tools differ in their electrical characteristics as well as their practicality towards noise reduction. For this reason they are listed roughly in a suggested order of priorities. Of the tools, inductance and capacitance are the most powerful filtering elements, and can also be the most cost-effective and small in size.
Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of practical, effective power supply filters. There are generally three classes of capacitors useful in filters in the 10kHz-100MHz frequency range suitable for switchers. These are broadly distinguished by their generic dielectric types; electrolytic, film, and ceramic. These dielectrics can in turn be further subdivided as discussed below. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 9.25. Background and tutorial information on capacitors can be found in Reference 2 and many vendor catalogs.

**CAPACITOR SELECTION**

<table>
<thead>
<tr>
<th></th>
<th>Aluminum Electrolytic (General Purpose)</th>
<th>Aluminum Electrolytic (Switching Type)</th>
<th>Tantalum Electrolytic</th>
<th>Polyester (Stacked Film)</th>
<th>Ceramic (Multilayer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>100 μF (1)</td>
<td>120 μF (1)</td>
<td>100 μF (1)</td>
<td>1 μF</td>
<td>0.1 μF</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>25 V</td>
<td>25 V</td>
<td>20 V</td>
<td>400 V</td>
<td>50 V</td>
</tr>
<tr>
<td>ESR</td>
<td>0.6 Ω @ 100 kHz</td>
<td>0.18 Ω @ 100 kHz</td>
<td>0.12 Ω @ 100 kHz</td>
<td>0.11 Ω @ 1 MHz</td>
<td>0.12 Ω @ 1 MHz</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>≥ 100 kHz</td>
<td>≥ 500 kHz</td>
<td>≥ 1 MHz</td>
<td>≥ 10 MHz</td>
<td>≥ 1 GHz</td>
</tr>
</tbody>
</table>

(1) Types shown in Figure 9.26 data
(2) Upper frequency limit is strongly size and package dependent

**Figure 9.25**

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance of the capacitor switches from a capacitive to inductive
characteristic. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used, and all capacitor types discussed here are available in surface mount packages, which are preferable for high speed uses.

The electrolytic family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes general purpose aluminum electrolytic types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They have relatively high leakage currents (this can be tens of µA, but is strongly dependent upon specific family design, electrical size and voltage rating vs. applied voltage). However, this is not likely to be a major factor for basic filtering applications.

Also included in the electrolytic family are tantalum types, which are generally limited to voltages of 100V or less, with capacitance of 500µF or less[Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do the general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the switching type, which is designed and specified for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This type of capacitor competes directly with the tantalum type in high frequency filtering applications, and has the advantage of a much broader range of available values.

More recently, high performance aluminum electrolytic capacitors using an organic semiconductor electrolyte have appeared [Reference 5]. These OS-CON families of capacitors feature appreciably lower ESR and higher frequency range than do the other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad ranges of values and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10µF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10milliohms or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.
Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the stacked-film type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see type “V” of Reference 4, plus Reference 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the very high frequencies, stacked film types only should be considered. Some manufacturers are also supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability in values up to several µF in the high-K dielectric formulations of X7R and Z5U, at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). The NP0 types are limited in available values to 0.1µF or less, with 0.01µF representing a more practical upper limit.

Multilayer ceramic “chip caps” are increasingly popular for bypassing and filtering at 10MHz or more, because their very low inductance design allows near optimum RF bypassing. In smaller values, ceramic chip caps have an operating frequency range to 1GHz. For these and other capacitors for high frequency applications, a useful value can be ensured by selecting a value which has a self-resonant frequency above the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in general purpose, tantalum and switching type electrolytics, a broad series resonance region is noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, which is nominally equal to the capacitor’s ESR at that frequency. In an example below, this low Q resonance is noted to encompass quite a wide frequency range, several octaves in fact. Contrasted to the very high Q sharp resonances of film and ceramic caps, this low Q behavior can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where a high level of ESR is critical, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.
Figure 9.26 illustrates the high frequency impedance characteristics of a number of electrolytic capacitor types, using nominal 100µF/20V samples. In these plots, the impedance, |Z|, vs. frequency over the 20Hz-200kHz range is displayed using a high resolution 4-terminal setup [Reference 8]. Shown in this display are performance samples for a 100µF/25V general purpose aluminum unit (top curve @ right), a 120µF/25V HFQ unit (next curve down @ right), a 100µF/20V tantalum bead type (next curve down @ right), and a 100µF/20V OS-CON unit (lowest curve @ right). While the HFQ and tantalum samples are close in 100kHz impedance, the general purpose unit is about 4 times worse. The OS-CON unit is nearly an order of magnitude lower in 100kHz impedance than the tantalum and switching electrolytic types.

As noted above, all real capacitors have parasitic elements which limit their performance. As an insight into why the impedance curves of Figure 9.26 appear the way they do, a (simplified) model for a 100µF/20V tantalum capacitor is shown in Figure 9.27.
The electrical network representing this capacitor is shown, and it models the ESR and ESL components with simple R and L elements, plus a 1megohm shunt resistance. While this simple model ignores temperature and dielectric absorption effects which occur in the real capacitor, it is still sufficient for this discussion.

When driven with a constant level of AC current swept from 10Hz to 100MHz, the voltage across this capacitor model is proportional to its net impedance, which is shown in Figure 9.28.
At low frequencies the net impedance is almost purely capacitive, as noted by the 100Hz impedance of 15.9ohms. At the bottom of this “bathtub” curve, the net impedance is determined by ESR, which is shown to be 0.12ohms at 125kHz. Above about 1MHz this capacitor becomes inductive, and impedance is dominated by the effect of ESL. While this particular combination of capacitor characteristics have been chosen purposely to correspond to the tantalum sample used with Figure 9.26, it is also true that all electrolytics will display impedance curves which are similar in general shape. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style). The simulation curve of Figure 9.28 can be considered as an extension of the 100µF/20V tantalum capacitor curve from Figure 9.26.

Ferrites (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful for decoupling in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites becomes resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 9.29 summarize a number ferrite characteristics.
CHARACTERISTICS OF FERRITES

- Good for frequencies above 25kHz
- Many sizes and shapes available including leaded “resistor style”
- Ferrite impedance at high frequencies is primarily resistive – Ideal for HF filtering
- Low DC loss: Resistance of wire passing through ferrite is very low
- High saturation current
- Low cost

**Figure 9.29**

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). The most simple form is the bead of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the stage being decoupled. Alternately, the leaded ferrite bead is the same bead, mounted by adhesive on a length of wire, and used simply as a component (Reference 11 typifies these two styles). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount bead styles are also available.

FERRITE IMPEDANCE DEPENDS ON

- Material
- Permeability
- Frequency
- Number of Turns
- Size
- Shape
- Temperature
- Field Strength (generated by current flowing through wire)

**Figure 9.30**

Recently, PSpice ferrite models for Fair-Rite materials have become available that allow ferrite impedance to be estimated [Reference 12]. The models of Fair-Rite materials #43 and #73 can be downloaded from the MicroSim bulletin board (714-830-1550). These models have been designed to match measured impedances rather than theoretical impedances.
A ferrite’s impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. A spectrum analyzer is useful here. Second, the expected temperature range of the filter should be known, because ferrite impedance varies with temperature. Third, the DC bias current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should ultimately lead to the selection of the proper ferrite.

**CHOOSING THE RIGHT FERRITE DEPENDS ON**

- Source of Interference
- Interference Frequency Range
- Impedance Required at Interference Frequency
- Environmental Conditions:
  - Temperature, AC and DC Field Strength,
  - Size / Space Available
- Don’t fail to Test the Design -------

**EXPERIMENT! EXPERIMENT!**

Figure 9.31

Maintaining high power supply efficiency requires the intelligent limiting of series resistors and linear post regulators in the switching supply's output. However, small resistors (generally less than 10ohms) can be used in applications where load currents are low and load regulation is not highly critical.

Higher performance linear post regulators can provide 60dB and more of power supply rejection up to 100kHz, for example see the designs of [Reference 8]. When used with effective input filtering, their PSRR can be extended above 1MHz or higher. Linear post regulation will generally result in a net efficiency decrease, which can be serious if the regulator requires several volts of headroom. The PSRR vs. frequency performance of a linear post regulator should also be carefully considered. For example, some low dropout linear regulators offer very little power supply rejection at frequencies above a few kHz, a performance fact of life which must be traded off against the efficiency advantages of the <100mV level dropouts they can boast.

Using the component selection choices mentioned above, low and high frequency band filters can be designed to smooth the noisy switcher's DC output so as to produce an analog ready 5V supply. It is most practical to do this over two (and sometimes more) stages, with each stage optimized for a range of frequencies. One basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to about 10MHz. This larger filter is used as a card entry filter providing broadband filtering for all analog power entering the PC board. Thereafter, smaller
and more simple local filter stages can be used to provide very high frequency
decoupling, right at the power pins of the individual ICs.

Figure 9.32 illustrates a card entry filter suitable for use with switching supplies. Because of the low rolloff point of 1.5kHz and mV level DC errors, it will be effective for a wide variety of filter applications just as it is shown. This filter is a single stage LC low-pass filter covering the 1kHz to 1MHz range, using carefully chosen parts. Because of component losses, it begins to lose effectiveness above a few MHz, but is still able to achieve an attenuation approaching 60dB at 1MHz.

The key to low DC losses is the use of input choke, L1, a ferrite-core unit selected for a low DC resistance (DCR) of <0.25ohms at the 100µH inductance. The prototype was tested with an axial lead type 5250 choke, but the radial style 6000-101K should give comparable results [Reference 13]. Both chokes have a low inductance shift due to the 300mA load current. The low DCR allows the 300mA to be passed with no more than 75mV of DC error at full load. Alternately, resistive filtering might be used in place of L1, but the basic tradeoff here is that load current capacity will be compromised for comparable DC errors. For example, a 1ohm resistor with a 75mV DC allowable error can pass only a 75mA current.

C1, a 100µF/20V tantalum type, provides the bulk of the capacitive filtering, shunted by a 1µF multilayer ceramic. The remaining part of the filter is R1, a damping resistor used to control resonant peaks.

"CARD-ENTRY" SWITCHING SUPPLY FILTER

Figure 9.32

Figure 9.33 shows the frequency response of this filter, both in terms of a SPICE simulation as well as lab measurements. There is good agreement between the simulation and the measurements for the common range below 1MHz. Measurements were not made above 1MHz, since higher frequencies are attenuated by second stage localized high frequency filters.
This filter has some potential pitfalls, and one of them is the control of resonances. If the LCR circuit formed does not have sufficiently high resistance at the resonant frequency, amplitude peaking will result. This peaking can be minimized with resistance at two locations: in series with $L_1$, or in series with $C_1+C_2$. Obviously, limited resistance is usable in series with $L_1$, as this increases the DC errors. Thus the use of the $C_1+C_2$ series damping resistor $R_1$, which should not be eliminated. The 1ohm value used actually provides a slightly underdamped response, with peaking on the order of 1dB. An alternate value of 1.5ohms can also be used for less peaking, if this is desired, but the tradeoff here is that the attenuation below 1MHz will then suffer.

Note that if the damping resistor were to be eliminated or an excessively low value used, it is possible that a transient at the frequency of $L_1-(C_1+C_2)$ resonance could cause the filter to ring, actually exacerbating whatever peak amplitude occurs at the input. Of course, keeping the basic filter corner frequency well below the lowest commonly used switcher frequency of 20kHz also helps to minimize this possibility. A side benefit of $R_1$ is that it buffers variations in parasitic resistance in $L_1$ and $C_1$, by making them smaller percentage of the total resistance, and thus less likely to effect overall performance. For wide temperature applications however, temperature changes of the filter characteristics will still need consideration.

![OUTPUT RESPONSE OF “CARD-ENTRY” FILTER](image)

**Figure 9.33**

Because of the high sensitivity to source series resistance of this filter, measuring its frequency response is not a trivial task. The low output impedance high current unity gain buffer of Figure 9.34 was used for the data of Figure 9.33. Note that the filter presents a load of ~1ohms to the source at resonance, so the buffer drive level is kept less than 100mV RMS, to prevent buffer current limiting.
A local high frequency filter which can be used in conjunction with the card entry filter is shown in Figure 9.35. This simple filter can be considered an option, one which is exercised dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It is composed of Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, which provides a resistance of more than 80ohms at 10MHz, increasing to over 100ohms at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a 0.1μF ceramic unit shown.

Both the card entry filter and the local high frequency decoupling filters are designed to filter differential-mode noise only. They use components commonly available off the shelf from national distributors [Reference 14].
The following is a list of switching power supply filter layout and construction guidelines which will help guarantee that the filter does the best job possible:

(1) Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low inductance change at the rated DC current, as well as low DCR.

(2) Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.

(3) Use short leads or leadless components, to minimize lead inductance. This will minimize the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred.

(4) Use a large-area ground plane for minimum impedance.

(5) Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not absolutely necessary, it does instill confidence in a design when correlation is achieved (see Reference 15).

The discussion of switching power supplies so far has focused on filtering the output of the supply. This assumes that the incoming AC power is relatively clean, an assumption not always valid. However, the AC power can also be an EMI path, both entering and exiting the equipment. To remove this path and reduce emissions caused by the switching power supply and other circuits in the instrument, a power line filter is required. Remember that the AC line power can be lethal! Do not experiment without proper equipment and training!

All components used in power line filters should be UL approved, and the best way to provide this for your equipment is to specify only a complete, packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors, which are integral to many line filters. This is the best way to do this function, as this automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.
POWER LINE FILTERING IS ALSO IMPORTANT

Commercial power line filters, such as the one shown schematically in Figure 9.37, can be quite effective in reducing noise. AC power-line noise is generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines.

TYPICAL COMMERCIAL POWER LINE FILTER

Common-mode noise is dominant at frequencies over 1MHz and is generally introduced into the AC lines through capacitive coupling. Ferrites provide effective filtering of the high frequency common-mode noise when used as common-mode chokes. For example, to create an effective common-mode choke, a few turns of the input power leads can be wound around a large ferrite. This provides a simple and effective solution for common-mode noise, but is ineffective against differential-mode noise. Differential-mode noise can be minimized by using proper LC filtering.
techniques as described earlier in this section, using proper UL approved across-the-line rated components. A power-line filter must be designed to minimize both common- and differential-mode noise to keep EMI from entering and leaving the system.

**POWER LINE NOISE MODES**

- **Common Mode:**
  - Dominates above 1MHz, Primarily Capacitive Coupled
  - 2200 to 4700pF typical shunt capacitor values
  - 0.5 to 10mH typical series ferrite values

- **Differential Mode:**
  - Dominates below 1MHz
  - 0.1 to 2.2µF typical shunt capacitor values
  - Molyperm or powdered iron inductors, 100 to 200µH, typical series values

*Figure 9.38*

Notice the common-mode choke formed by the inductors on both sides of the filter in Figure 9.37. These inductors have a dual role, because they are also part of the differential-mode LC filters. This filter, using multiple stages, is an example of a higher quality type.

As noted, the AC power line filter should be in good electrical contact with the chassis of the instrument. Furthermore, connecting the AC power line directly into the power line filter reduces the possibility of EMI entering or exiting the instrument. If this is not possible, routing the filter AC input power lines close to the chassis and twisting them will help minimize loop areas and minimize LF magnetic coupling.

The power supply filter should be located as close as possible to the switching power supply; i.e., in commercial units it is always integral to the supply. Many switching power supplies have steel enclosures which can be used for electric and LF magnetic shielding (however, the enclosure must be connected to chassis ground to act as a Faraday shield).

If digital circuitry is present, the digital power pick-off point should occur *before* the switching power supply filter. This minimizes the digital noise in the output of the switching supply filter, plus minimizes any potential DC error form the higher currents.
POWER LINE FILTER PLACEMENT IS IMPORTANT

Figure 9.39
REFERENCES: NOISE REDUCTION AND FILTERING FOR SWITCHING POWER SUPPLIES


4. Type HFQ Aluminum Electrolytic Capacitor and type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

5. OS-CON Aluminum Electrolytic Capacitor 93/94 Technical Book, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, (501) 633-6634.


10. Fair-Rite Linear Ferrites Catalog, Fair-Rite Products, Box J, Wallkill, NY, 12886, (914) 895-2055.

11. Type EXCEL leaded ferrite bead EMI filter, and type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.


14. DIGI-KEY, PO Box 677, Thief River Falls, MN, 56701-0677, (800) 344-4539.

15. Tantalum Electrolytic Capacitor SPICE Models, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.
LOW DROPOUT REFERENCES AND REGULATORS

Walt Jung

Many circuits require stable regulated voltages relatively close in potential to an unregulated source. An example would be a linear post regulator for a switching power supply, where voltage loss is critical. This low dropout type of regulator is readily implemented with a rail-rail output op amp. The wide output swing and low saturation voltage enables outputs to come within a fraction of a volt of the source for medium current (<30mA) loads, such as reference applications. For higher output currents, the rail-rail voltage swing feature allows direct drive to low saturation voltage pass devices, such as power PNPs or P-channel MOSFETs. Op amps which work from 3V up with the rail-rail features are most suitable here, providing power economy and maximum flexibility.

BASIC REFERENCES IN LOW POWER SYSTEMS

Among the many problems in making stable DC voltage references work from 5V and lower supplies are quiescent power consumption, overall efficiency, the ability to operate down to 3V, low input/output (dropout) capability, and minimum noise output. Because such low voltage supplies can’t support 6V zeners, these low voltage references must necessarily be bandgap based-- a 1.2V potential.

One difficulty is simply to get a reference circuit which works well at 3V inputs, conditions which dictate a lower voltage reference diode. A workhorse circuit solution is the reference and appropriate low power scaling buffer shown in Figure 9.40. Here a low current 1.2V diode is used for D1, the 1.235V AD589. Resistor R1 sets the current, chosen for 50µA at the minimum supply of 2.7V. Obviously, loading on the unbuffered diode must be minimized at the VREF node.

RAIL-RAIL OUTPUT OP AMPS ALLOW GREATEST FLEXIBILITY IN LOW DROPOUT REFERENCES

Figure 9.40
The amplifier U1 both buffers and optionally scales up the 1.2V reference, allowing higher source/sink currents. A higher op amp quiescent current is expended in doing this, and is a basic design tradeoff of this approach. This current can range from 150-300µA/channel with the OP295/495 and OP191/291/491 series for U1, 620µA/channel using an AD820/822/824 section, or in the range of 1000-2000µA/channel with the OP284 and OP279. The former two series are most useful for very light loads (<2mA), while the latter three series provide device dependent outputs up to 50mA. All devices are simply used in the circuit as shown, and their key specs are summarized in Figure 9.41.

**OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS**

<table>
<thead>
<tr>
<th>Device*</th>
<th>Iq/channel mA</th>
<th>Vsat(+), V(min @ mA)</th>
<th>Vsat(-), V(max @ mA)</th>
<th>Isc, mA (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP193/293/493</td>
<td>0.017</td>
<td>4.20 @ 1</td>
<td>0.280 @ 1 (typ)</td>
<td>± 8</td>
</tr>
<tr>
<td>OP255/495 (max)</td>
<td>0.150</td>
<td>4.50 @ 1</td>
<td>0.110 @ 1</td>
<td>± 11</td>
</tr>
<tr>
<td>OP191/291/491</td>
<td>0.300</td>
<td>4.80 @ 2.5</td>
<td>0.075 @ 2.5</td>
<td>± 8.75</td>
</tr>
<tr>
<td>AD820/822</td>
<td>0.620</td>
<td>4.89 @ 2</td>
<td>0.055 @ 2</td>
<td>± 15</td>
</tr>
<tr>
<td>OP284/484 (max)</td>
<td>1.250</td>
<td>4.95 @ 2.5</td>
<td>0.125 @ 2.5</td>
<td>± 7.5</td>
</tr>
<tr>
<td>OP279</td>
<td>2.000</td>
<td>4.80 @ 10</td>
<td>0.075 @ 10</td>
<td>± 45</td>
</tr>
</tbody>
</table>

*Typical device specifications @ Vs = +5V, Ta = 25°C, unless otherwise noted.

**Figure 9.41**

In Figure 9.40, without gain scaling resistors R2-R3, V_{OUT} is simply 1.235V. With the resistors, V_{OUT} can be anywhere between the rails, due to the rail-rail output swing of the op amps mentioned above. With rail-rail devices, this buffered reference is inherently "low dropout", allowing a +4.5V reference output on a +5V supply, for example. The general expression for V_{OUT} is shown in the figure, where “V_{REF}” is the reference voltage, in this case 1.235V.

Amplifier standby current can be optionally reduced to below 20µA if an amplifier from the OP193/293/493 series is used. This will be at the expense of current drive and positive rail saturation, but does provide the lowest possible quiescent current when necessary. All devices operate from voltages down to 3V (except the OP279, which operates at 5V).

Power conservation can be a critical issue with references, as can output DC precision. For such applications, simple one-package fixed voltage references which simply “drop in” with minimal external circuitry and deliver high accuracy are most attractive. Two unique features of the three terminal REF19X bandgap reference family are low power, and shutdown capability. The series allows fixed outputs from 2.048-5V to be controlled between ON and OFF, via a TTL/CMOS power control input. It provides precision reference quality for those popular voltages shown in Figure 9.42.
The REF19X family can be used as a simple three terminal fixed reference as per the table by tying pins 2 and 3 together, or as an ON/OFF controlled device, by programming pin 3 as noted. In addition to the shutdown capacity, the distinguishing functional features are a low dropout of 0.5V at 10mA, and a low current drain for both quiescent and shutdown states, 45 and 15µA (max.), respectively. For example, working from inputs in the range of 6.3 to 15V, a REF195 used as shown drives 5V loads at up to 30mA, with grade dependent tolerances of ±2 to ±5mV, and max TCs of 5 to 25ppm/°C. Other devices in the series provide comparable accuracy specifications, and all have low dropout features.

To maximize DC accuracy in this circuit, the output of U1 should be connected directly to the load with short heavy traces, to minimize IR drops. The common terminal (pin 4) is less critical due to lower current in this leg.

**LOW DROPOUT REGULATORS**

By adding a boost transistor to the basic rail-rail output low dropout reference of Figure 9.40, output currents of 100mA or more are possible, while still retaining features of low standby current and low dropout voltage. Figure 9.43 shows a low dropout regulator with 800µA standby current, suitable for a variety of outputs at current levels of 100mA.
The 100mA output is achieved with a controlled gain bipolar power transistor for pass device Q1, an MJE170. Maximum output current control is provided by limiting base drive to Q1 with series resistor R3. This limits the base current to about 2mA, so the max HFE of Q1 then allows no more than 500mA, thus limiting Q1’s short circuit dissipation to safe levels.

Overall, the circuit operates as a follower with gain, as was true in the case of Figure 9.40, so VOUT has a similar output expression. The circuit is adapted for different voltages simply by programming R1 via the table. Dropout with a 100mA load is about 200mV, thus a 5V output is maintained for inputs above 5.2V (see table), and VOUT levels down to 3V are possible. Step load response of this circuit is quite good, and transient error is only a few mVp-p for a 30-100mA load change. This is achieved with low ESR switching type capacitors at C1-C2, but the circuit also works with conventional electrolytics (with higher transient errors).

If desired, lowest output noise with the AD820 is reached by including the optional reference noise filter, R5-C3. Lower current op amps can also be used for lower standby current, but with larger transient errors due to reduced bandwidth.

While the 30mA rated output current of the REF19X series is higher than most reference ICs, it can be boosted to much higher levels if desired, with the addition of a PNP transistor, as shown in Figure 9.44. This circuit uses full time current limiting for protection of pass transistor shorts.
In this circuit the supply current of reference U1 flows in R1-R2, developing a base drive for pass device Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100-200mA loads, U1 is never required to furnish more than a few mA, and this factor minimizes temperature related drift. Short circuit protection is provided by Q2, which clamps drive to Q1 at about 300mA of load current. With separation of control/power functions, DC stability is optimum, allowing best advantage of premium grade REF19X devices for U1. Of course, load management should still be exercised. A short, heavy, low resistance conductor should be used from U1-6 to the VOUT sense point “S”, where the collector of Q1 connects to the load.

Because of the current limiting, dropout voltage is raised about 1.1V over that of the REF19X devices. However, overall dropout typically is still low enough to allow operation of a 5 to 3.3V regulator/reference using the 3.3V REF-196 for U1, with a Vs of 4.5V and a load current of 150mA.

The heat sink requirements of Q1 depend upon the maximum power. With Vs = 5V and a 300mA current limit, the worst case dissipation of Q1 is 1.5W, less than the TO-220 package 2W limit. If TO-39 or TO-5 packaged devices such as the 2N4033 are used, the current limit should be reduced to keep maximum dissipation below the package rating, by raising R4. A tantalum output capacitor is used at C1 for its low ESR, and the higher value is required for stability. Capacitor C2 provides input bypassing, and can be a ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are in order. To enable shutdown control, the connection to U1-2 and U1-3 is broken at “X”, and diode D1 allows a CMOS control source to drive U1-3 for ON/OFF control. Startup from shutdown is not as clean under heavy load as it is with the basic REF19X series stand-alone, and can require several milliseconds
under load. Nevertheless, it is still effective, and can fully control 150mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

By combining a REF19X series reference IC with a rail-rail output op amp, the best of both worlds is realized performance-wise (see Figure 9.45). The REF19X basic reference provides a stable low TC voltage source with low current drain, while the rail-rail output op amp provides high output current with both sink/source load capability.

30mA OUTPUT CURRENT REGULATOR/REFERENCE

![Figure 9.45](image)

The low dropout performance of this circuit is provided by stage U2, 1/2 of an OP279 connected as a follower/buffer for the V\textsubscript{OUT2} as produced by U1. The low voltage saturation characteristic of the OP279 allows up to 30 mA of load current in the illustrated use, a 5V to 3.3V converter. In this application the stable 3.3V from U1 is applied to U2 through a noise filter, R1-C1. U2 replicates the U1 voltage within a few mV, but at a higher current output at V\textsubscript{OUT1}. It also has ability to both sink and source output current(s), unlike most IC references. R2 and C2 in the feedback path of U2 provide bias compensation for lowest DC error and additional noise filtering.

To scale V\textsubscript{OUT2} to another (higher) output level, the optional resistor R3 (shown dotted) is added, causing the new V\textsubscript{OUT1} to become:

\[
V_{\text{OUT1}} = V_{\text{OUT2}} \left[ 1 + \frac{R2}{R3} \right]
\]

As an example, for a V\textsubscript{OUT1} = 4.5V, and V\textsubscript{OUT2} = 2.5V from a REF192, the gain required of U2 is 1.8 times, so R3 and R2 would be chosen for a ratio of 1.25/1, or 22.5kohm/18kohm. Note that for the lowest V\textsubscript{OUT1} DC error, R2 || R3 should be
maintained equal to R1 (as here), and the R2-R3 resistors should be stable, close
tolerance metal film types.

Performance of the circuit is good in both AC and DC senses, with the measured DC
output change for a 30mA load change under 1mV, equivalent to an output
impedance of <0.03ohm. The transient performance for a step change of 0-10mA of
load current is determined largely by the R5-C5 output network. With the values
shown, the transient is about 10mV peak, and settles to within 2mV in 8μs, for
either polarity. Further reduction in transient amplitude is possible by reducing R5
and possibly increasing C3, but this should be verified by experiment to minimize
excessive ringing with some capacitor types. Load current step changes smaller than
10mA will of course show less transient error.

The circuit can be used either as shown as a 5 to 3.3V reference/regulator, or it can
also be used with ON/OFF control. By driving pin 3 of U1 with a logic control signal
as noted, the output is switched ON/OFF. Note that when ON/OFF control is used,
resistor R4 must be used with U1, to speed ON-OFF switching.

As noted, the “low dropout” style of regulator is readily implemented with a rail-rail
output op amps such as those of Figure 9.41, as their wide output swing allows easy
drive to a low saturation voltage pass device. Further, it is most useful when the op
amp has a rail-rail input feature, as this allows high-side current sensing, for
positive rail current limiting. Typical applications are voltages developed from a 3-
9V range system sources, or anywhere where low dropout performance is required
for power efficiency. The 4.5V case here works from 5V nominal sources, with worst-
case levels down to 4.6V or less.

Figure 9.46 shows such a regulator using an OP284 plus a low R_{ds(on)} P-channel
MOSFET pass device. Low dropout performance is provided by Q1, with a rating of
0.11ohm with a gate drive of 2.7V. This relatively low gate drive allows operation on
supplies as low as 3V without compromise to overall performance.
The circuit’s main voltage control loop operation is provided by U1B, half of the OP284. This voltage control amplifier amplifies the 2.5V reference voltage produced by U2, a REF192. The regulated output voltage $V_{OUT}$ is then of the same form as noted in the previous circuit.

Note that for the lowest $V_{OUT}$ DC error, $R_2 || R_3$ should be maintained equal to $R_1$ (as here), and the $R_2$-$R_3$ resistors should be stable, close tolerance metal film types. The table suggests $R_1$-$R_3$ values for popular output voltages. In general, $V_{OUT}$ can be anywhere between $V_{OUT_2}$ and the 12V maximum rating of Q1.

While the low voltage saturation characteristic of Q1 is part of the low dropout key, the other advantage is a low and accurate current-sense comparison. Here, this is provided by current sense amplifier U1A, which is provided a 20mV reference from the 1.235V AD589 reference diode D2 and the $R_7$-$R_8$ divider. When the product of the output current and $R_s$ match this threshold, current control is activated, and U1A drives Q1’s gate via D1. Overall circuit operation is then under current mode control, with a current limit $I_{limit}$ defined as:

$$I_{limit} = \left[ \frac{V_{R(D2)}}{R_s} \right] \left[ \frac{R_7}{R_7 + R_8} \right]$$

Obviously the comparison voltage should be small, since it becomes a significant portion of the overall dropout voltage. Here, the 20mV value used is higher than the typical offset of the OP284, but still reasonably low as a percentage of $V_{OUT}$ (<0.5%). For other $I_{limit}$ levels, sense resistor $R_s$ should be set along with $R_7$-$R_8$, to maintain this threshold voltage between 20 and 50mV.

For a 4.5V output version, measured DC output change for a 225mA load change was on the order of a few µV, while the dropout voltage at this same current level...
was about 30mV. The current limit as shown is 400mA, allowing operation at levels up to 300mA or more. While the Q1 device can support currents of several amperes, a practical current rating takes into account the SO-8 device’s 2.5W 25°C dissipation. A short-circuit current of 400mA at an input level of 5V will cause a 2W dissipation in Q1, so other input conditions should be considered carefully in terms of Q1’s potential overheating. If higher powered devices are used for Q1, the circuit will support outputs of tens of amperes as well as the higher $V_{OUT}$ levels noted above.

The circuit can be used either as shown for a standard low dropout regulator, or it can also be used with ON/OFF control. Note that when the output is OFF in this circuit, it is still active (i.e., not an open circuit). This is because the OFF state simply reduces the voltage input to R1, leaving the U1A/B amplifiers and Q1 still active.

When ON/OFF control is used, resistor R10 should be used with U1, to speed ON-OFF switching, and to allow the output of the circuit to settle to a nominal zero voltage. Components D3 and R11 also aid in speeding up the ON-OFF transition, by providing a dynamic discharge path for C2. OFF-ON transition time is less than 1ms, while the ON-OFF transition is longer, but under 10ms.
REFERENCES: LOW DROPOUT REFERENCES AND REGULATORS


EMI/RFI CONSIDERATIONS

Adolfo A. Garcia

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI hardened equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI hardened.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Elektrotechniker) in Germany. VDE regulations are more restrictive than the FCC’s with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and will require mandatory compliance in 1996. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on radiated emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to conducted interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Table 9.1 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.
Radiated Emission Limits for Commercial Computer Equipment

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Class A (at 3 m)</th>
<th>Class B (at 3 m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 - 88</td>
<td>300 µV/m</td>
<td>100 µV/m</td>
</tr>
<tr>
<td>88 - 216</td>
<td>500 µV/m</td>
<td>150 µV/m</td>
</tr>
<tr>
<td>216 - 1000</td>
<td>700 µV/m</td>
<td>200 µV/m</td>
</tr>
</tbody>
</table>

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Table 9.1

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) will require mandatory compliance in 1996 to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Table 9.1. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory, EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically hostile, all...
equipment manufacturers will be required to comply with all European Community EMC regulations by 1996.

**Automotive Equipment**

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on each of the active components used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

**EMC Regulations’ Impact on Design**

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

**Passive Components: Your Arsenal against EMI**

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To successfully use these components, the designer must understand their non-ideal behavior. For example, Figure 9.47 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.
ALL PASSIVE COMPONENTS EXHIBIT “NON IDEAL” BEHAVIOR

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Figure 9.47

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02ohm/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20nH/ft, it becomes inductive at frequencies above 160kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain, as illustrated in Figure 9.48. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of real components, a strategy can now be developed to find solutions to most EMI problems.
With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 9.49, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a source, a receptor or victim, and a path between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

Interfering signals reach the receptor by conduction (the circuit or system interconnections) or radiation (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the interconnects. Between 30MHz and 300MHz, the primary coupling mechanism is cable radiation and connector leakage. At frequencies greater than 300MHz, the primary mechanism is slot and board radiation. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.
When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 9.50. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system emission and can be either conducted or radiated. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

The second type of interference is circuit or system immunity. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is susceptibility, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is internal. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.
In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: frequency, amplitude, time, impedance, and distance.

The frequency of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI have shows that the time response of signals contains all the necessary information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

\[ f_{EMI} = \frac{1}{\pi \cdot t_{rise}} \]  
Eq. 9.1

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/µs and gain-bandwidth products greater than 500MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high
speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

**Radio Frequency Interference**

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument’s susceptibility to the applied RFI power density at the unit. In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus. For comparative purposes, Equation 9.2 can be used to convert electric-field intensity to power density and vice-versa:

\[
\text{\textbf{E} \left( \frac{\text{V}}{\text{m}} \right) = 61.4 \sqrt{\frac{\text{PT} \left( \text{mW} \right)}{\text{cm}^2}}} \quad \text{Eq. 9.2}
\]

where \( E \) = Electric Field Strength, in volts per meter, and \( PT \) = Transmitted power, in milliwatts per cm\(^2\).
From the standpoint of the source-path-receptor model, the strength of the electric field, $E$, surrounding the receptor is a function of transmitted power, antenna gain, and distance from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 9.3:

$$E \left( \frac{\text{V}}{\text{m}} \right) = 5.5 \left( \sqrt{\frac{P_T \cdot G_A}{d}} \right) \text{ Eq. 9.3}$$

where $E =$ Electric field intensity, in V/m; $P_T =$ Transmitted power, in mW/cm$^2$; $G_A =$ Antenna gain (numerical); and $d =$ distance from source, in meters.

For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 9.51, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.
RFI CAN CAUSE RECTIFICATION IN SENSITIVE ANALOG CIRCUITS

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 9.52). The three general points of RFI coupling are signal inputs, signal outputs, and power supplies. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1µF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

Figure 9.51

KEEPING RFI AWAY FROM ANALOG CIRCUITS

Decouple all voltage supplies to analog chip with high-frequency capacitors
Use high-frequency filters on all lines that leave the board
Use high-frequency filters on the voltage reference if it is not grounded

Figure 9.52
Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 9.53, real low-pass filters may exhibit leakage at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to leak when the applied signal frequency is 100 to 1000 higher than the filter’s cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.

A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 f3dB

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Figure 9.53

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into low-band, mid-band, and high-band, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of woofer-midrange-tweeter for RFI low-pass filter design illustrated in Figure 9.54. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as feed-through protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.
Another cause of filter failure is illustrated in Figure 9.55. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.

**NON-ZERO (INDUCTIVE AND/OR RESISTIVE) FILTER GROUND REDUCES EFFECTIVENESS**

In the first part of this discussion on RF immunity, circuit level techniques were discussed. In this next section, the second strategic concept for RF immunity will be discussed: *all cables behave as antennas*. As shown in Figure 9.56, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through
stray capacitance. If the length of the cable is considered *electrically long* (a concept to be explained later) at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the figure, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used. In applications where shielding is not used, filters on input/output signal and power lines work well. Small ferrites and capacitors should be used to filter high frequencies, provided that: (1) the capacitors have short leads and are tied directly to the chassis ground, and (2) the filters are physically located close to the connectors to prevent noise pickup.

"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA
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The key issues and techniques described in this section on solving RFI related problems are summarized in Figure 9.57. Some of the issues were not discussed in detail, but are equally important. For a complete treatment of this issue, the interested reader should consult References 1 and 2. The main thrust of this section was to provide the reader with a problem-solving strategy against RFI and to illustrate solutions to commonly encountered RFI problems.
Radio-Frequency Interference is a Serious Threat
- Equipment causes interference to nearby radio and television
- Equipment upset by nearby transmitters

RF-Failure Modes
- Digital circuits prime source of emissions
- Analog circuits more vulnerable to RF than digital circuits

Two Strategic Concepts
- Treat all cables as antennas
- Determine the most critical circuits

RF Circuit Protection
- Filters and multilayer boards
- Multistage filters often needed

RF Shielding
- Slots and seams cause the most problems

RF Cable Protection
- High-quality shields and connectors needed for RF protection

Figure 9.57

Solutions for Power-Line Disturbances

The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate transient power-line disturbances.

Figure 9.58 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOV) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.
POWER LINE DISTURBANCES CAN GENERATE EMI
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Commercial EMI filters, as illustrated in Figure 9.59, can be used to filter less
catastrophic transients or high-frequency interference. These EMI filters provide
both common-mode and differential mode filtering as in Figure 9.58. An optional
choke in the safety ground can provide additional protection against common-mode
noise. The value of this choke cannot be too large, however, because its resistance
may affect power-line fault clearing.

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER
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Transformers provide the best common-mode power line isolation. They provide good
protection at low frequencies (<1MHz), or for transients with rise and fall times
greater than 300ns. Most motor noise and lightning transients are in this range, so
isolation transformers work well for these types of disturbances. Although the
isolation between input and output is galvanic, isolation transformers do not provide
sufficient protection against extremely fast transients (<10ns) or those caused by
high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 9.60,
isolation transformers can be designed for various levels of differential- or common-
mode protection. For differential-mode noise rejection, the Faraday shield is
connected to the neutral, and for common-mode noise rejection, the shield is
connected to the safety ground.
Printed Circuit Board Design for EMI Protection

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system’s susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 9.61 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

A key point in minimizing noise problems in a design is to choose devices no faster than actually required by the application. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.
Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs and can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 9.62 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.
Once the system’s critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 9.63. These low-impedance planes form very high-frequency stripline transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.
Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance and if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 9.64 for a number of logic families.
LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches / ns

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**Figure 9.64**

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of $f_{\text{max}}$, then the equivalent risetime, $t_r$, can be calculated using the equation $t_r = 0.35/f_{\text{max}}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 9.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_0(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left[ \frac{5.98d}{0.89w + t} \right] \text{ Eq. 9.4}$$

where $\varepsilon_r$ = dielectric constant of printed circuit board material;  
$\dot{d}$ = thickness of the board between metal layers, in mils;  
$w$ = width of metal trace, in mils; and  
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 9.5:

$$t_{pd} (\text{ns/ ft}) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \text{ Eq. 9.5}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 ($\varepsilon_r=4.7$) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be
88ohms and 1.7ns/ft (7"/ns), respectively. Transmission lines can be effectively terminated in several ways depending on the application, as described in Section 2 of this book.

Figure 9.65 is a summary of techniques that should be applied to printed circuit board layouts to minimize the effects of electromagnetic interference, both emissions and immunity.

CIRCUIT BOARD DESIGN AND EMI
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“ALL EMI PROBLEMS BEGIN AND END AT A CURCUIT”

- Identify critical, sensitive circuits
- Where appropriate, choose ICs no faster than needed
- Consider and implement sound PCB design
- Spend time on the initial layout (by hand, if necessary)
- Power supply decoupling (digital and analog circuits)
- High-speed digital and high-accuracy analog don’t mix
- Beware of connectors for input / output circuits
- Test, evaluate, and correct early and often

Figure 9.65

A REVIEW OF SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1, 3, and 4 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (lambda) of the interference divided by 2pi, or lambda/2pi. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2pi yields a distance of
approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\text{ohms}$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377ohms. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377ohms.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the reflection of the incident wave off the shielding material. Second is the loss due to the absorption of the transmitted wave within the shielding material. Both concepts are illustrated in Figure 9.66. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

**REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS**

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![Figure 9.66](image-url)
Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

\[ R_{e}(dB) = 322 + 10\log_{10} \left( \frac{\sigma_r}{\mu_r f^3 r^2} \right) \]  
Eq. 9.6

where \( \sigma_r \) = relative conductivity of the shielding material, in Siemens per meter; 
\( \mu_r \) = relative permeability of the shielding material, in Henries per meter; 
\( f \) = frequency of the interference, and 
\( r \) = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

\[ R_{m}(dB) = 14.6 + 10\log_{10} \left( \frac{f r^2 \sigma_r}{\mu_r} \right) \]  
Eq. 9.7

and, for plane waves ( \( r > \lambda/2\pi \)), the reflection loss is given by:

\[ R_{pw}(dB) = 168 + 10\log_{10} \left( \frac{\sigma_r}{\mu_r f} \right) \]  
Eq. 9.8

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

\[ A(dB) = 3.34 t \sqrt{\sigma_r \mu_r f} \]  
Eq. 9.9

where \( t \) = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, \( Z_s \), increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate
shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Table 9.2.

**Impedance and Skin Depths for Various Shielding Materials**

| Material   | Conductivity $\sigma_r$ | Permeability $\mu_r$ | Shield Impedance $|Z_s|$ | Skin depth $\delta$ (inch) |
|------------|-------------------------|----------------------|---------------------------|---------------------------|
| Cu         | 1                       | 1                    | $3.68 \times 10^{-7} \cdot \sqrt{f}$ | $2.6 \frac{1}{\sqrt{f}}$ |
| Al         | 1                       | 0.61                 | $4.71 \times 10^{-7} \cdot \sqrt{f}$ | $3.3 \frac{1}{\sqrt{f}}$ |
| Steel      | 0.1                     | 1000                 | $3.68 \times 10^{-5} \cdot \sqrt{f}$ | $0.26 \frac{1}{\sqrt{f}}$ |
| $\mu$ Metal | 0.03                   | 20,000               | $3 \times 10^{-4} \cdot \sqrt{f}$ | $0.11 \frac{1}{\sqrt{f}}$ |

where $\sigma_0 = 5.82 \times 10^7 \text{ S/m}$
$\mu_0 = 4\pi \times 10^{-7} \text{ H/m}$
$\varepsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 9.67). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.
ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS

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Figure 9.67

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 9.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

\[
\text{Shielding Effectiveness (dB)} = 20 \log_{10} \left( \frac{\lambda}{2 \cdot L} \right) \quad \text{Eq. 9.10}
\]

where \( \lambda \) = wavelength of the interference and 
\( L \) = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.
General Points on Cables and Shields

Although covered in more detail later, the improper use of cables and their shields is a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 1, 2, 4, and 5. As illustrated in Figure 9.68, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

**LENGTH OF SHIELDED CABLES DETERMINES AN “ELECTRICALLY LONG” OR “ELECTRICALLY SHORT” APPLICATION**

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![Diagram](image)

**Figure 9.68**

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a low-impedance point. A generalized example of this mechanism is illustrated in Figure 9.69.
CONNECT THE SHIELD AT ONE POINT AT THE LOAD
TO PROTECT AGAINST LOW FREQUENCY (50/60Hz) THREATS
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Figure 9.69

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1Vrms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is electrically long, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01µF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.
System EMI problems often occur after the equipment has been designed and is operating in the field. More often than not, the original designer of the instrument has retired and is living in Tahiti, so the responsibility of repairing it belongs to someone else who may not be familiar with the product. Figure 9.70 summarizes the EMI problem solving techniques discussed in this section and should be useful in these situations.

**EMI TROUBLESHOOTING PHILOSOPHY**
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- **Diagnose before you fix**
- **Ask yourself:**
  - What are the symptoms?
  - What are the causes?
  - What are the constraints?
  - How will you know you have fixed it?
- **Use available models for EMI to identify source - path - victim**
- **Start at low frequency and work up to high frequency**
- **EMI doctor’s bag of tricks:**
  - Aluminum foil
  - Conductive tape
  - Bulk ferrites
  - Power line ferrites
  - Signal filters
  - Resistors, capacitors, inductors, ferrites
  - Physical separation

**Figure 9.70**
REFERENCES ON EMI/RFI


Sensors and Cable Shielding

John McDonald

The environments in which analog systems operate are often rich in sources of EMI. Common EMI noise sources include power lines, logic signals, switching power supplies, radio stations, electric lighting, and motors. Noise from these sources can easily couple into long analog signal paths, such as cables, which act as efficient antennas. Shielded cables protect signal conductors from electric field (E-field) interference by providing low impedance paths to ground at the offending frequencies. Aluminum foil, copper, and braided stainless steel are materials very commonly used for cable shields due to their low impedance properties.

Simply increasing the separation between the noise source and the cable will yield significant additional attenuation due to reduced coupling, but shielding is still required in most applications involving remote sensors.

Figure 9.71
WHY SHIELD CABLES?

There are two paths from an EMI source to a susceptible cable: capacitive (or E-field) and magnetic (or H-field) coupling (see Figure 9.73). Capacitive coupling occurs when parasitic capacitance exists between a noise source and the cable. The amount of parasitic capacitance is determined by the separation, shape, orientation, and the medium between the source and the cable.

Magnetic coupling occurs through parasitic mutual inductance when a magnetic field is coupled from one conductor to another as shown in Figure 9.73. Parasitic mutual inductance depends on the shape and relative orientation of the circuits in question, the magnetic properties of the medium, and is directly proportional to conductor loop area. Minimizing conductor loop area reduces magnetic coupling proportionally.

Shielded twisted pair cables offer further noise immunity to magnetic fields. Twisting the conductors together reduces the net loop area, which has the effect of canceling any magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero.
HOW DOES INTERFERENCE ENTER THE SYSTEM?

Figure 9.73

To study the shielding problem, a precision RTD (Resistance Temperature Detector) amplifier circuit was used as the basis for a series of experiments. A remote 100ohm RTD was connected to the bridge, bridge driver, and the bridge amplifier circuit (Figure 9.74) using 10 feet of a shielded twisted pair cable. The RTD is one element of a 4-element bridge (the three other resistor elements are located in the bridge and bridge driver circuit). The gain of the instrumentation amplifier was adjusted so that the sensitivity at the output was 10mV/°C, with a 5V full scale. Measurements were made at the output of the instrumentation amplifier with the shield grounded in various ways. The experiments were conducted in lab standard environment where a considerable amount of electronic equipment was in operation.

The first experiment was conducted with the shield ungrounded. As shown in Figure 9.74, shields left floating are not useful and offer no attenuation to EMI-induced noise, in fact, they act as antennas. Capacitive coupling is unaffected, because the floating shield provides a coupling path to the signal conductors. Most cables exhibit parasitic capacitances between 10-30pF/ft. Likewise, HF magnetically coupled noise is not attenuated because the floating cable shield does not alter either the geometry or the magnetic properties of the cable conductors. LF magnetic noise is not attenuated significantly, because most shield materials absorb very little magnetic energy.
To implement effective EMI/RFI shielding, the shield must be grounded. A grounded shield reduces the value of the impedance of the shield to ground (Z in Figure 9.73) to small values. Implementing this change will reduce the amplitude of the E-Field noise substantially.

Designers often ground both ends of a shield in an attempt to reduce shield impedance and gain further E-Field attenuation. Unfortunately, this approach can create a new set of potential problems. The AC and DC ground potentials are generally different at each end of the shield. Figure 9.75 illustrates how low-frequency ground loop current is created when both ends of a shield are grounded. This low frequency current flows through the large loop area of the shield and couples into the center conductors through the parasitic mutual inductance. If the twisted pairs are precisely balanced, the induced voltage will appear as a common-mode rather than a differential voltage. Unfortunately, the conductors may not be perfectly balanced, the sensor and excitation circuit may not be fully balanced, and the common mode rejection at the receiver may not be sufficient. There will therefore be some differential noise voltage developed between the conductors at the output end, which is amplified and appears at the final output of the instrumentation amplifier. With the shields of the experimental circuit grounded at both ends, the results are shown in Figure 9.76.
SIGNAL GROUND AND EARTH GROUND HAVE DIFFERENT POTENTIALS WHICH MAY INDUCE GROUND LOOP CURRENT

![Diagram of signal ground and earth ground](image)

Figure 9.75

GROUNDING BOTH ENDS OF A SHIELD PRODUCES LOW FREQUENCY GROUND LOOPS

![Diagram of grounding both ends of a shield](image)

Figure 9.76

Figure 9.77 illustrates a properly grounded system with good electric field shielding. Notice that the ground loop has been eliminated. The shield has a single point ground, located at the signal conditioning circuitry, and noise coupled into the shield is effectively shunted into the receiver ground and does not appear at the output of the instrumentation amplifier.
Figure 9.77 shows an example of a remotely located, ungrounded, passive sensor (EEG electrodes) which is connected to a high-gain, low power AD620 instrumentation amplifier through a shielded twisted pair cable. Note that the shield is properly grounded at the signal conditioning circuitry. The AD620 gain is $1000\times$, and the amplifier is operated on ±3V supplies. Notice the absence of 60Hz interference in the amplifier output.
Most high impedance sensors generate low-level current or voltage outputs, such as a photodiode responding to incident light. These low-level signals are especially susceptible to EMI, and often are of the same order of magnitude as the parasitic parameters of the cable and input amplifier.

Even properly shielded cables can degrade the signals by introducing parasitic capacitance that limits bandwidth, and leakage currents that limit sensitivity. An example is shown in Figure 9.79, where a high-impedance photodiode is connected to a preamp through a long shielded twisted pair cable. Not only will the cable capacitance limit bandwidth, but cable leakage current limits sensitivity. A preamplifier, located close to the high-impedance sensor, is recommended to amplify the signal and to minimize the effect of cable parasitics.
Figure 9.80 is an example of a high-impedance photodiode detector and pre-amplifier, driving a shielded twisted pair cable. Both the amplifier and the shield are grounded at a remote location. The shield is connected to the cable driver common, G1, ensuring that the signal and the shield at the driving end are both referenced to the same point. The capacitor on the receiving side of the cable shunts high frequency noise on the shield into ground G2 without introducing a low-frequency ground loop. This popular grounding scheme is known as hybrid grounding.

Figure 9.80

Figure 9.81 illustrates a balanced active line driver with a hybrid shield ground implementation. When a system’s operation calls for a wide frequency range, the hybrid grounding technique often provides the best choice (Reference 8). The capacitor at the receiving end shunts high-frequency noise on the shield into G2 without introducing a low-frequency ground loop. At the receiver, a common-mode choke can be used to help prevent RF pickup entering the receiver, and subsequent RFI rectification (see References 9 and 10). Care should be taken that the shields are grounded to the chassis entry points to prevent contamination of the signal ground (Reference 11).
HYBRID (LF AND HF) GROUNDING WITH ACTIVE DRIVER

Figure 9.81

To summarize this discussion, shield grounding techniques must take into account the type and the configuration of the sensor as well as the nature of the interference. When a low-impedance passive sensor is used, grounding the shield to the receiving end is the best choice. Active sensor shields should generally be grounded at the source (direct connection to source ground) and at the receiver (connect to receiver ground using a capacitor). This hybrid approach minimizes high-frequency interference and prevents low-frequency ground loops. Shielded twisted conductors offer additional protection against shield noise because the coupled noise occurs as a common-mode, and not a differential signal.

The best shield can be compromised by poor connection techniques. Shields often use “pig-tail” connections to make the connection to ground. A “pig-tail” connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

This section has highlighted the more common techniques used in cable shielding. There are other techniques which involve the use of driven shields, twin-shields, common-mode chokes, etc. References 1, 2, 5, 6, 7, and 8 provide an exhaustive study of the entire topic of noise reduction techniques including cable shielding.
SUMMARY OF CABLE SHIELDING TECHNIQUES

- Do not let the shield “float”
- Do not connect both ends of directly to ground
- No LF current should flow in the shield
- Use the *hybrid* approach for LF and HF electric field interference
- The shield includes the connector, therefore avoid using *pigtails* to connect shields to ground. Use *chassis ground* to prevent *signal ground* contamination
- Use Common-Mode chokes at receiver to enhance RF rejection
- Other techniques exist:
  - Driven Shields
  - Twin-Shields

Figure 9.82
REFERENCES: SENSORS AND CABLE SHIELDING


4. AD620 Instrumentation Amplifier, Data Sheet, Analog Devices, Inc.


GENERAL REFERENCES: HARDWARE DESIGN TECHNIQUES


2. **E.S.D. Prevention Manual**
   Available free from Analog Devices, Inc.


   AND

   Free from Analog Devices.

6. International EMI Emission Regulations
   Canada       CSA C108.8-M1983       FDR       VDE 0871/VDE 0875
   Japan        CISPR (VCCI)/PUB 22   USA       FCC-15 Part J

   Free from Analog Devices.


    Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.


